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Evaluation of Different Multilevel Inverter Topologies for Harmonics and Power Losses

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Abstract: ***With the emission norms becoming more stringent and escalating cost of hydrocarbon fuels automotive companies are developing Electric Vehicles (EV), Hybrid Electric Vehicles (HEVs), and Plug-in Hybrid Electric Vehicles (PHEV). All this vehicles need a traction motor and a power converter to drive the traction motor. The requirements for the power converters include high peak power, optimum consumption of energy, low output harmonics and inexpensive circuit. One of the promising technologies that can be made to meet these requirements is Multilevel Inverters (MLI). This paper discusses the three types MLI namely of diode clamped, cascaded H-bridge, and reduced switch multilevel inverters (MLI). This paper focuses on evaluation of harmonics and power losses in the above inverter topologies. Based on the simulation results obtained it is found that Total Harmonic Distortion (THD) of MLI is less compared to H-Bridge inverter where as power loss in H-Bridge inverter is less compared to MLI.***

Keywords: Multilevel inverter, Total Harmonic Distortion, Traction Motors.

I. INTRODUCTION

Power electronic converters which use semiconductor devices are becoming more and more popular for various industrial applications, especially dc/ac PWM inverters. This type of inverters have been extending their range of use in industry because they provide reduced energy consumption, better system efficiency, improved quality of product, good maintenance, and so on. At the same time the semiconductor devices used as switches have certain limitation especially at high power applications.

To overcome these limitations series and parallel connection of switches is often considered an effective solution. In addition, stepped waveform in the output of inverter has better harmonic spectrum than 2-level inverter and can be operated at switching frequencies. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations [1–3].

The principal function of MLI is to synthesize a desired ac voltage from several separate dc sources, which may be obtained from batteries, fuel cells, or solar cells [1].

The desired output voltage waveform can be synthesized from the multiple voltage levels. With an increasing number of dc sources, the inverter output voltage waveform approaches a nearly sinusoidal waveform. The small output voltage step results in high quality output voltage, reduction of voltage stresses on power switching devices, lower switching losses and higher efficiency.

A. The use of MLI to drive the main traction drives in electrical vehicles has the following advantages [2-4]:

1) They are suitable for large VA-rated motor drives, and traditional 230 V or 460 V motors can be used.
2) Higher efficiency is expected for these multilevel converter systems because higher voltages can be utilized and the switching frequency of the devices is at a minimum.
3) Low voltage switching devices can be used.
4) No electromagnetic interference (EMI) problem or common-mode voltage/current problem exists.
5) No charge unbalance problem results from either charge mode or drive mode.

The major drawback associated with MLI is the use of great number of power switches. With increase number of power switches there is considerable voltage drop across the power switches putting a limitation on the available output voltage and efficiency of the inverter. Thus it becomes imperative to study the performance these MLIs with respect to power loss in the converter circuits and advantages it provides in case of THD with increase use of power switches.

In this paper operating principle of three types of MLI namely diode clamped, cascaded and reduced switch is discussed. The power loss and THD of the MLI is discussed and compared with the results of standard H-Bridge inverter.

II. MULTILEVEL INVERTER TOPOLOGIES

A. Diode Clamped Multilevel Inverter

A five-level diode-clamped inverter is shown in Fig 1. Each of the three phases of the inverter shares a common dc bus, which has been subdivided by four capacitors into five levels. The voltage across each capacitor is V_{dc}, and the voltage stress across each switching device is limited to V_{dc} through the clamping diodes. Table 1 lists the output voltage levels possible for one phase of the inverter with the negative dc rail voltage V_0 as a reference. State condition 1 means the switch is on, and 0 means the switch is off. Each phase has five complementary switch pairs such that turning on one of the switches of the pair require that the other complementary switch be turned off. The complementary switch pairs for phase leg A are (S_4, S_8), (S_3, S_7), (S_2, S_6) and (S_1, S_5). For a Five-level inverter, a set of five switches is on at any given time.

TABLE 1. DIODE CLAMPED VOLTAGE LEVELS AND THEIR SWITCH STATES

Output V_{a0}	Switch States							
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$V_5=V_{dc}$	1	1	1	1	0	0	0	0
$V_4=3V_{dc}/4$	0	1	1	1	1	0	0	0
$V_3=V_{dc}/2$	0	0	1	1	1	1	0	0
$V_2=V_{dc}/4$	0	0	0	1	1	1	1	0
$V_1=0$	0	0	0	0	1	1	1	1

The configuration in Fig 1 can be modified by replacing each capacitor with batteries that can be used for EVs.

B. The main advantages and disadvantages of multilevel diode-clamped converters are as follows [1-3].

1) Advantages

a) All of the phases share a common dc bus, which minimizes the capacitance requirements of the converter.
b) The capacitors can be pre-charged as a group.
c) The control method is simple.
d) Inverter efficiency is high because all devices are switched at the fundamental frequency.

2) Disadvantages

a) Excessive clamping diodes are required when the number of levels is high.
b) It is difficult to control the real power flow of the individual converter in multi-converter systems.

c) Cascaded Multilevel Inverter

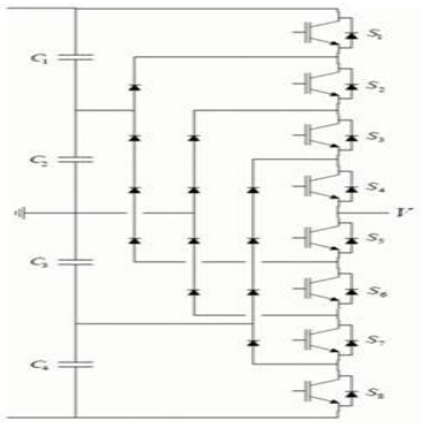

Fig 1. Diode Clamped Multilevel Inverter

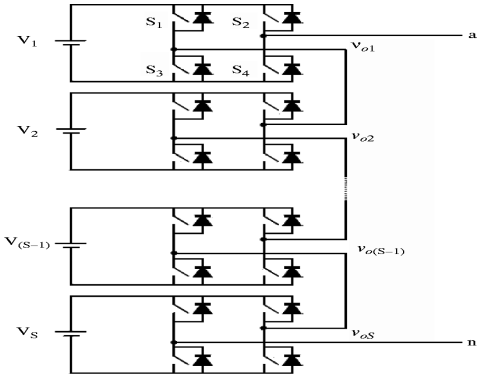

Fig 2. Single Phase Cascaded Multilevel Inverter

A single-phase structure of an m-level cascaded MLI is shown in Fig 2. It consists of separate dc source connected to a H-bridge inverter. Each inverter level can generate three different voltage outputs, +Vdc, 0, and -Vdc by connecting the dc source to the ac output by different combinations of the four switches, S1, S2, S3, and S4. To obtain +Vdc, switches S1 and S4 are turned on, whereas -Vdc can be obtained by turning on switches S2 and S3. By turning on S1 and S2 or S3 and S4, the output voltage is 0. The ac outputs of each of the different H-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate dc sources. The phase voltage $V_{an} = V_{o1} + V_{o2} + V_{o3} + V_{o4} + V_{o5}$.

C. The main advantages and disadvantages of multilevel cascaded H-bridge converters are as follows [8, 9].

1) Advantages

a) The number of possible output voltage levels is more than twice the number of dc sources (m = 2s + 1).

b) The series of H-bridges makes for optimized circuit layout and packaging, resulting in reduced cost.

c) Soft-switching techniques can be used to reduce switching losses and device stresses.

2) Disadvantages

a) Excessive clamping diodes are required when the number of levels is high.

It is difficult to control the real power flow of the individual converter in multi-converter systems.

D. Reduced Switch Multilevel inverter

A simple 5-level MLI configuration with reduced number of switches is shown in Fig 3. It consists of four switches S1 to S4 which generates stepped waveform based on given gate drive. When all the four switches i.e., S1 to S4 are off the output voltage is zero. Table 1 gives the switch state and output voltage level for each state. Switches S5,S6 and S7, S8 are made to conduct for π interval alternatively with overall time period of 2π.

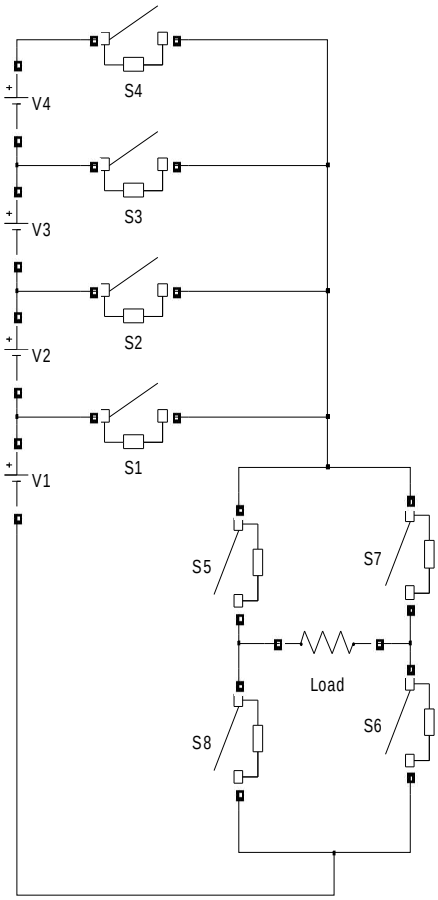

Fig 3. Reduced Switch Multilevel Inverter

Table 2. Switch states and output voltage levels

Switch Number	Switch State				Output Voltage
M1	1	0	0	0	V1
M2	0	1	0	0	V1+V2
M3	0	0	1	0	V1+V2+V3
M4	0	0	0	1	V1+V2+V3+V4

Switch state – 1 indicates the switch is on and switch state – 0 indicates the switch is off.

E. The main advantages and disadvantages of Reduced Switch Multilevel converters are as follows.

1) Advantages

a) As the number of voltage levels increases the number of conducting devices remains the same.

b) All of the phases share a common dc bus.

c) The control method is simple.

d) Inverter efficiency is high because all devices are switched at the fundamental frequency.

2) Disadvantages

a) As the number of voltage levels increases the voltage stress on the device also increases.

b) It needs separate DC source for each level hence limiting its application.

III. SWITCHING METHODOLOGY

The switching angles for switches are calculated in such ways that lower dominant harmonics are eliminated. For this purpose Fourier analysis need to be done to determine the frequency spectra of the output waveform.

The Fourier series of n-step output waveform is given by

$$f(t) = \frac{KV_{dc}}{\pi}\sum_{n=1}^{\infty}\left[\sum_{i=1}^{h}\cos(h\theta_i)\frac{\sin(h\omega t)}{h}\right] \qquad (1)$$

where, V_{dc}:Voltage of voltage sources for each cell that is unity, θ_i:the switching angle, h:the harmonic order, K:Number of voltage levels.

For eliminating 3rd, 5th, and 7th harmonics following equation are used which is obtained from equation (1).

$$h_1 = \frac{3V_{dc}}{\pi}(\cos(\theta_1) + (\cos(\theta_2) + (\cos(\theta_3) \qquad (2)$$

$$h_3 = \frac{3V_{dc}}{\pi}(\cos(3\theta_1) + (\cos(3\theta_2) + (\cos(3\theta_3) \qquad (3)$$

$$h_5 = \frac{3V_{dc}}{\pi}(\cos(5\theta_1) + (\cos(5\theta_2) + (\cos(5\theta_3) \qquad (4)$$

$$h_7 = \frac{3V_{dc}}{\pi}(\cos(7\theta_1) + (\cos(7\theta_2) + (\cos(7\theta_3) \qquad (5)$$

Equations (2) to (5) are for the harmonics that should be eliminated, so (3) to (5) should be equated to zero for eliminating the 3rd, 5th and 7th harmonics. The resulting equations are:

$$\frac{\pi}{4} = \frac{3V_{dc}}{\pi}(\cos(\theta_1) + (\cos(\theta_2) + (\cos(\theta_3) \qquad (6)$$

$$0 = \frac{3V_{dc}}{\pi}(\cos(3\theta_1) + (\cos(3\theta_2) + (\cos(3\theta_3) \qquad (7)$$

$$0 = \frac{3V_{dc}}{\pi}(\cos(5\theta_1) + (\cos(5\theta_2) + (\cos(5\theta_3) \qquad (8)$$

$$0 = \frac{3V_{dc}}{\pi}(\cos(7\theta_1) + (\cos(7\theta_2) + (\cos(7\theta_3) \qquad (9)$$

These equations (6) to (7) are nonlinear transcendental equations that can be solved by an iterative method such as the Newton-Raphson method to obtain the switching angles.

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IV. MOSFET LOSS COMPUTATION MODEL

The metal-oxide semiconductor field-effect transistor (MOSFET) is a semiconductor device consisting of three terminals namely drain, source and gate. Gate is the control terminal. MOSFET conducts when (g < 0) and does not conduct when (g = 0). The MOSFET is connected in parallel with an internal diode that turns on when the MOSFET is reverse biased (Vds < 0) and no gate signal is applied (g=0). The model is simulated by an ideal switch controlled by a logical signal (g > 0 or g = 0), with a diode connected in parallel. Figure 3 gives MOSFET model, R_{on} is internal resistance of MOSFET when it is conducting. R_d is the internal diode resistance of MOSFET when it not conducting and V_f is the forward voltage drop of internal diode. The drain to source voltage, V_{ds} of MOSFET is defined as

A. $V_{ds} = R_{on} * I$ when MOSFET is on

B. $V_{ds} = R_d * I - V_f$ when is MOSFET is off

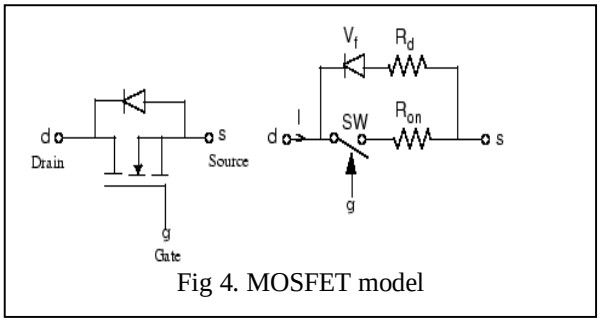

Fig 4. MOSFET model

For computing losses in MOSFET current through it and voltage across it is measured and multiplied and mean for one time period is taken, which gives the total loss taking place in the MOSFET.

V. MLI POWER LOSS ANALYSIS

In this section Power loss analysis on three different types of MLIs namely Diode clamped, Cascaded, Reduced switch and PWM H-Bridge inverter is discussed. The inverters should give RMS output voltage of 230V single phase, frequency of operation is 50Hz, and number of levels in case of MLIs is seven for a purely resistive load of 10KWs. Figure 5 gives the plot of efficiency of different types of inverter. It is observed from plot that PWM-Bridge inverter has the efficiency of 96%, Reduced switch MLI is 94% and cascaded and Diode clamped MLI has efficiency of around 90%. Figure 6 gives the plot of power losses in the different types of inverter circuits.

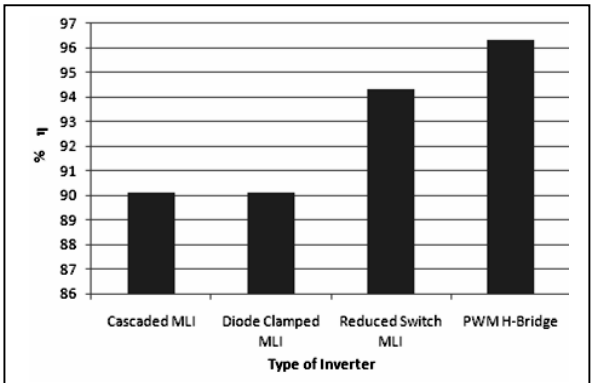

Fig 5. Efficiency of Different types of Inverters

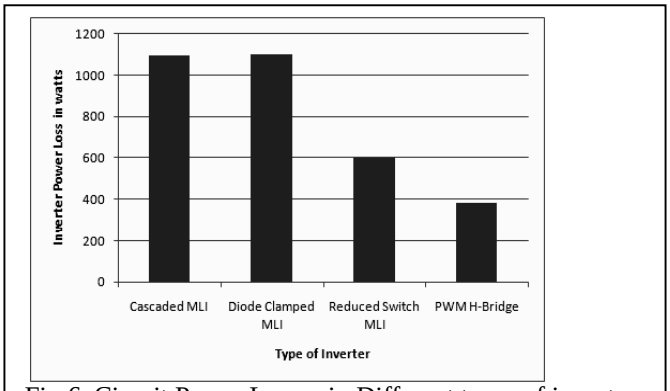

Fig 6. Circuit Power Losses in Different types of inverters

From the plot it is observed that Cascaded and Diode clamped MLI have circuit power loss of 1100 watts where as PWM H-Bridge inverter has circuit power loss of around 380 watts and that of reduced switch MLI has circuit power loss of 600 watts. The increased power loss in Cascaded and Diode clamped MLI can be attributed to the fact that the conducting devices are more. In case of the PWM H-Bridge inverter the number of conducting devices is less and Reduced switch MLI it is one device more than the PWM H-Bridge inverter. This is one of the reason for reduced efficiency in case of Cascaded and Diode clamped MLI as can be observed in figure 5.

VI. MLI HARMONIC ANALYSIS

The output waveform for 7-level inverters is shown in figure 7. The output waveforms obtained for diode clamped, cascaded and reduced switch MLIs are same and is shown in figure 7 and figure 8 gives the output waveforms for PWM H-Bridge inverter.

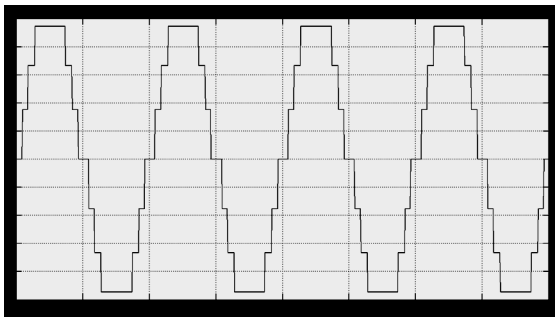

Fig 7. Multilevel inverter output waveform.

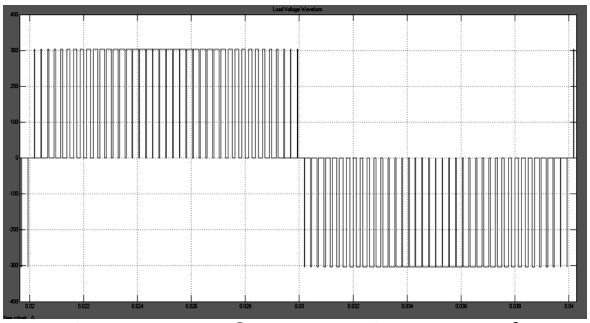

Fig 8. PWM H-Bridge Inverter Output Waveform

The FFT analysis of the waveform is shown in Figure 9. It is seen that 3rd, 5th, and 7th components are considerably reduced with the use MLI and THD is found to be 12.55% as shown in figure 9. THD in case of PWM H-Bridge Inverter is 64.36% has can be seen in figure 10.

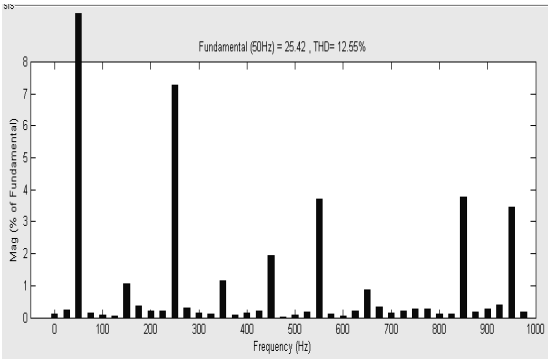

Fig 9. Frequency spectrum of MLI

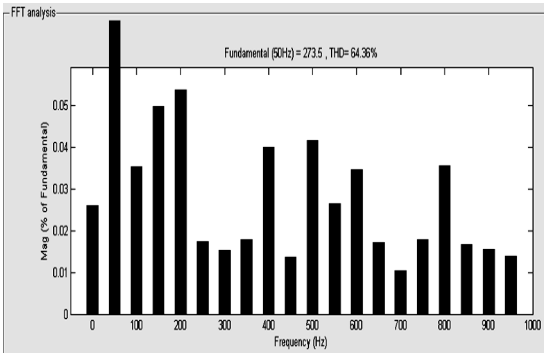

Fig 10. Frequency spectrum of H-Bridge Inverter

VII. CONCLUSIONS

In this paper power loss and harmonic analysis of three different types of MLI is carried out and compared with the 2-level inverter. It is observed that the efficiency of two level inverter with sinusoidal pulse width modulation is highest but THD is very poor. Reduction of the power loss and improved harmonic spectrum in comparison other topology is the main advantage of the reduced switch MLI. The proposed topology can be a good solution for applications that require high power quality, or applications that have considerable numbers of dc voltage sources like electric vehicles.

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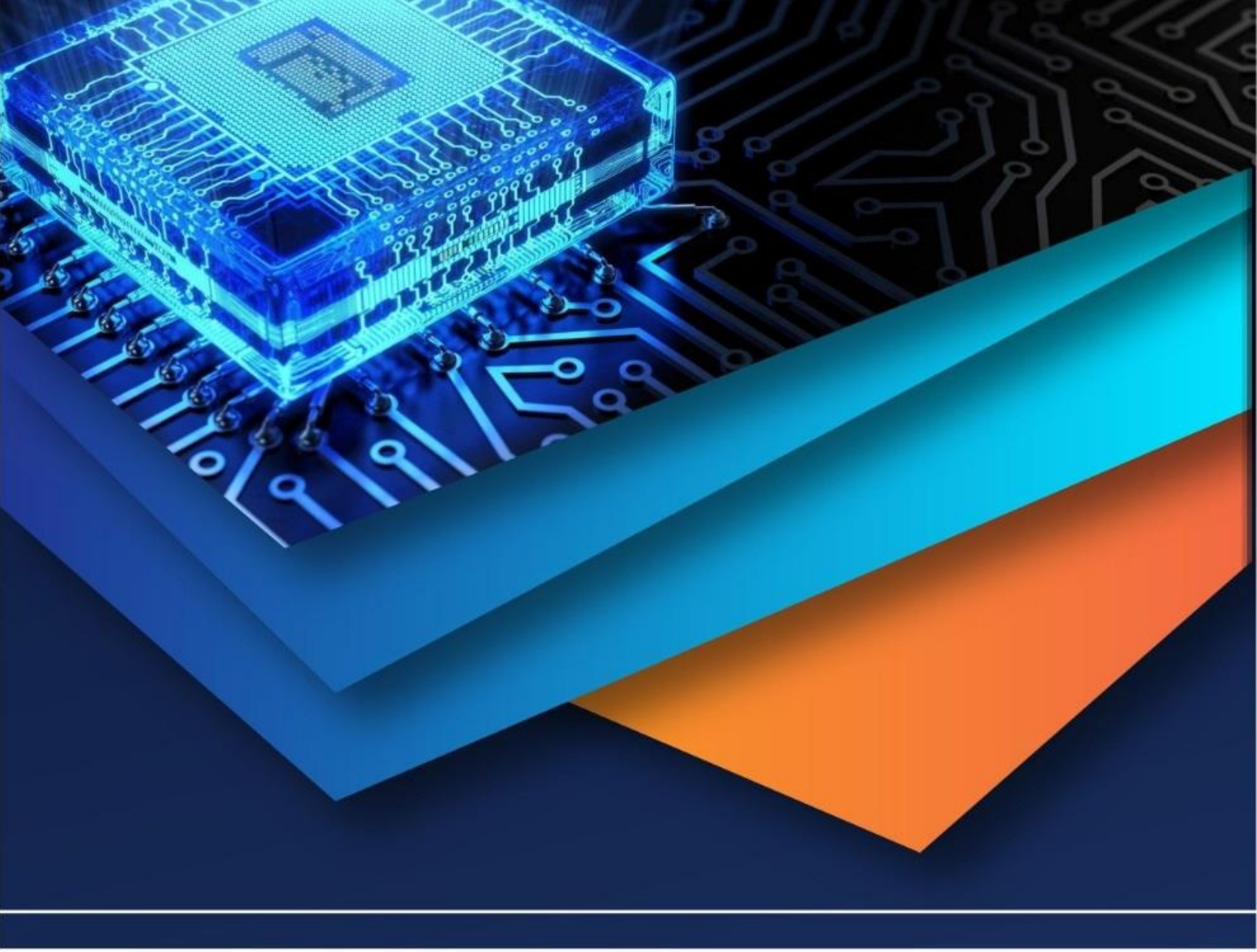

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