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Hyper-Threading Technology in Microprocessor

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Abstract- Hyper-Threading Technology is a form of simultaneous multithreading technology. Architecturally, a processor with Hyper-Threading Technology consists of two logical processors per core, each of which has its own processor architectural state. Each logical processor can be individually halted, interrupted or directed to execute a specified thread, independently from the other logical processor sharing the same physical core. In this paper, we will study about how Hyper threading Technology works and how it is useful in increasing the performance of microprocessors. We will also study about the impact of Hyper-Threading on Processor Resource Utilization in Multitasking.

Keywords- Simultaneous Multithreading Technology (SMT), Hyper-Threading Technology (HT), Processor Resource Utilization, Multitasking

I. INTRODUCTION

Before the introduction of hyper-threading, only one instruction stream at a time could be executed by a single CPU by maintaining a single instruction pointer. And the processor is allowed to execute multiple threads by switching between the threads. Later the simultaneous multithreading technology (SMT) was developed where a single processor could execute multiple threads simultaneously without switching. Intel Pentium 4 architectures adopted SMT with their trade mark called Hyper-Threading technology(HT technology).A single processor will appear as multiple logical processors with HT technology. So operating systems can schedule multiple threads to these logical processors in the way how threads can be scheduled on multiprocessor systems. Although HT technology maximizes the performance of a single processor by effective utilization of the processor resources, there is a limiting factor as the logical processors share most of the basic resources like cache, FPU and integer math unit of the single physical processor. And as the computer industry has also identified that the future performance improvements could not come from making a single core faster by making it complex, it must come largely by increasing the number of cores on a single chip, the later development in the processor architecture called the multi-core architecture has evolved. By integrating more than one processor on a single chip, multi-core processors improve the performance of parallel applications with less communication cost among the cores. The new generation Intel „core iX „ series processors combined the architectural features of both multi-core and Hyper-threading technologies to make each core on the die more faster. Though these architectures are expected to bring significant execution speedups for the applications [7], not all the applications may get the performance benefits from these architectures as with any hardware feature. If the application needs to get the benefit from these new processors, it should be a well written multithreaded application.

II. HYPER-THREADING ON A SINGLE-CORE

Hyper-Threading allows a single core processor to execute two threads by adding a "virtual" thread alongside the physical thread. From the architectural point of view, a hyper threaded processor contains two logical processors. Each logical processor has its own processor architectural state which consists of all the processor registers like data, Segment, control ,debug and other model specific registers to avoid the context switch between the two threads [13]. Each processor also has independent instruction streams , own APIC(advanced programmable interrupt controller) and they share the execution resources consisting of execution engine, the caches, the system bus and the firmware of the processor core . Each logical processor handles the interrupts sent to it on its own as it has its own APIC. By presenting itself to the operating system as two identical virtual processors, a hyper-threading processor will handle the work load generated by a CPU-intensive operation effectively because of the two logical processors handling the tasks at the same time.

III.HYPER-THREADING ON DUAL-CORE

Being its own set of execution units, a core is different from a logical processor and in hyper threaded Dual-Core, each core constitutes hyper-threading technology, enabling two threads to run simultaneously on each core with a little hardware overhead . So, in a dual-core HT Technology enabled system, one physical processor chip can have two cores and four logical processors. The architectural register state is duplicated on all the four logical processors and all of them share the physical execution resources. Figure 1 shows the block diagram of a hyper threaded dual-core processor. From the software point of view all the

cores are functionally equivalent and four separate threads can simultaneously run on the four logical cores which is good for multi-threading applications. From a micro architecture perspective, this means that instructions from all the logical processors will persist and execute simultaneously on shared execution resources. In a computer system with hyperthreaded dual-core processor , the performance monitor shows the usage of all the four logical processors.

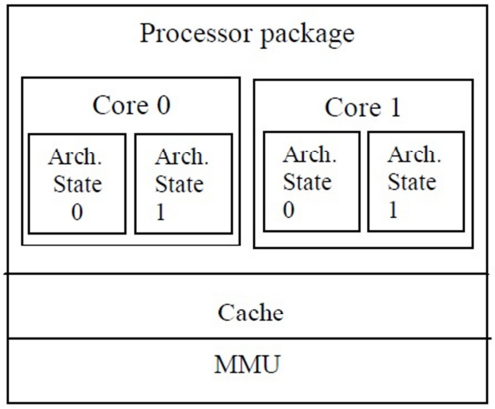

Fig 1: Dual core processor with Hyper-Threading

IV. RELATED WORK.

There was only a little research done on identifying the effect of HT technology on the performance of applications. HT performance evaluation using OpenMP threaded matrix matrix multiplication and a bench mark of 256-particle molecular dynamics on a dual processor –server with HT was conducted by Boisseau et al). Characterization of Java application performance using Pentium 4 processors with HT was done by Haung et al. Utilization of Pentium 4 performance counters in the performance of garbage collection in HT mode was studied by Blackburn et al. Saini et al., studied the impact of HT on processor resource utilization . They have also investigated how the scientific application performance in HT mode was affected because of shared resources and the utilization of these resources was compared between single threaded(ST) and HT modes. They have conducted the experiments on four NASA applications and investigated that HT technology improved the processor resource utilization more but this may not result in overall application performance gain. Gasmi et al., proposed MTFASTFDS, a multi-threaded parallel algorithm on a hyper-threading multi core processor for mining functional dependencies. They have shown that their parallel algorithm scales very well with the number of cores available. Tian et al., conducted the performance study on Hyper-Threading technology (HT) enabled Intel single processor and multi-processor systems by parallelizing two multimedia applications with OpenMP pragmas. They have presented the threaded code generation and optimization techniques and concluded that multithreaded code with OpenMP pragmas yields more speedup on a HT-enabled dual-CPU compared to HT-enabled single-CPU.

V. CONCLUSIONS

Though the computer hardware industry is introducing new processor architectures, a software application can take the performance gains from these architectures only when it is properly coded. Especially the architectures like multi-core and hyper threading technologies can give the performance benefit to the application only when the application is properly written to run with multiple threads. In this paper the performance results of parallelizing the popular data mining algorithm called apriori using OpenMP threads on a hyper threaded Intel Corei3 processor were presented and the results were compared with the results obtained a non-hyper threaded Intel Pentium Dual Core processor . The performance of the algorithm was compared on these architectures with two different I/O retrieval techniques - conventional I/O technique using fread() and a special I/O technique using mmap(). Our results proved that the efficiency and speed up of our parallel implementation were more with a hyper threaded processor compared to non-hyper threaded processor with both fread() and mmap() for all the datasets taken and at all the support counts considered.

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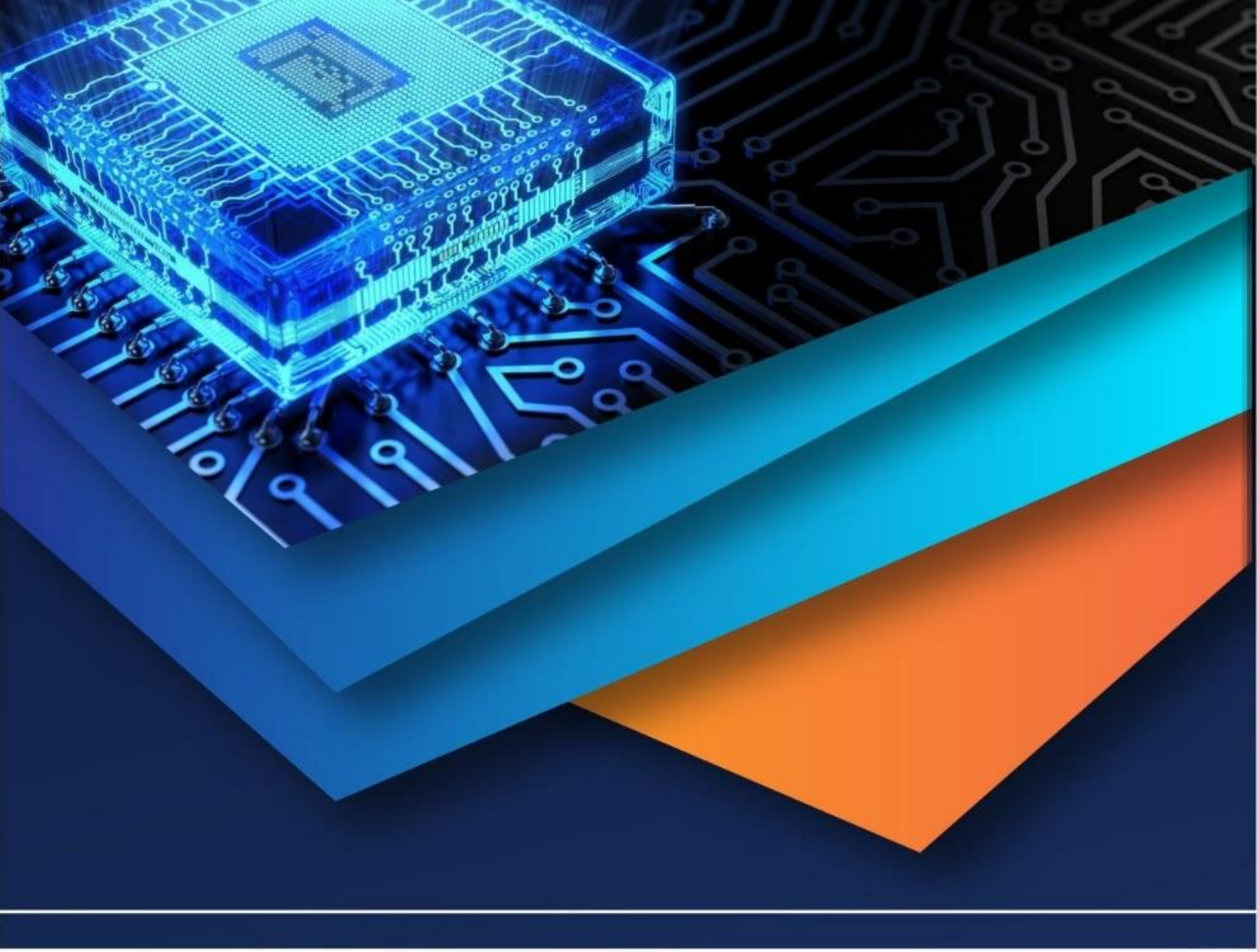

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