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128-Bit Area-Efficient Carry Select Adder

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Abstract—Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. The structure of the CSLA, suggests that there is scope for reducing the area in the CSLA. This work presents a simple and efficient gate-level modification to significantly reduce the area of the CSLA. This method uses first, the implementation of adder and then excess one adder. Based on this modification 128-bit square-root CSLA (SQRT CSLA) architecture has presented and compared with the regular SQRT CSLA architecture. For both modified and regular SQRT CSLA adders, the theoretical calculations for delay and area are tabulated. Experimentally delay and area comparisons for both regular and modified SQRT CSLA are done. The simulation is performed using Modelsim and synthesis is carried on Xilinx ISE12.2

Index Terms—Area-efficient, CSLA, low power

I. INTRODUCTION

Design of area- and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position.

The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum[2].However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input and ,then the final sum and carry are selected by the multiplexers (mux). The basic idea of this work is to use Binary to Excess-1 Converter (BEC) instead of RCA with in the regular CSLA to achieve lower area and power consumption [3]–[4]. The main advantage of this BEC logic comes from the lesser number of logic gates than the *n*-bit Full Adder (FA) structure. The details of the BEC logic are discussed in Section III.

This paper is structured as follows: Section II deals with the delay and area evaluation methodology of the basic adder blocks. Section III presents the detailed structure and the function of the BEC logic. The SQRT CSLA has been chosen for comparison with the proposed design as it has a more balanced delay, and requires lower power and area [5], [6]. The delay and area evaluation methodology of the regular and modified SQRT CSLA are presented in Sections IV and V, respectively. Results are analysed in Section VI. Finally, the work is concluded in Section VII.

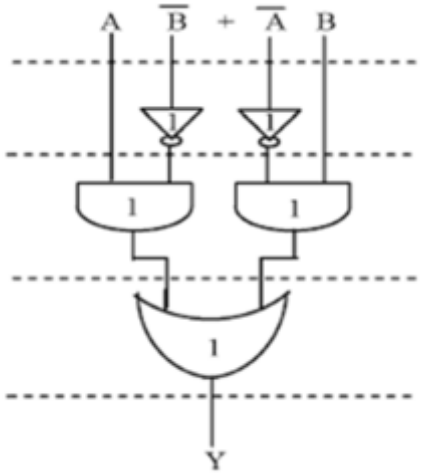

Fig: 1. Delay and Area evaluation of an XOR gate.

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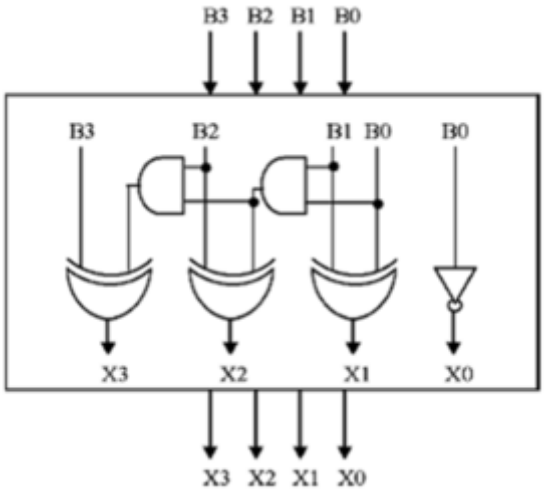

Fig: 2. 4-b BEC.

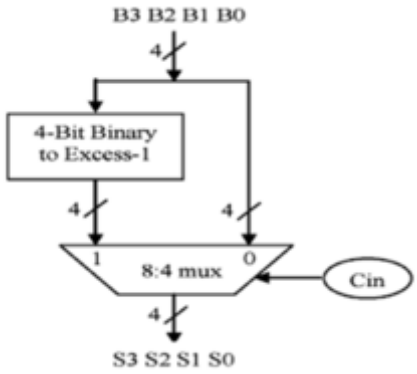

Fig: 3. 4-b BEC with 8:4 mux.

II. DELAY AND AREA EVALUATION METHODOLOGY OF THE BASIC ADDER BLOCKS

The AND, OR, and Inverter (AOI) implementation of an XOR gate is shown in Fig. 1. The gates between the dotted lines are performing the operations in parallel and the numeric representation of each gate indicates the delay contributed by that gate. The delay and area evaluation methodology considers all gates to be made up of AND, OR, and Inverter, each having delay equal to 1 unit and area equal to 1 unit. We then add up the number of gates in the longest path of a logic block that contributes to the maximum delay. The area evaluation is done by counting the total number of AOI gates required for each logic block. Based on this approach, the CSLA adder blocks of 2:1 mux, Half Adder (HA), and FA are evaluated and listed in Table I.

TABLE I
DELAY AND AREA COUNT OF THE BASIC BLOCKS OF CSLA

Adder blocks	Delay	Area
XOR	3	5
2:1 Mux	3	4
Half adder	3	6
Full adder	6	13

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TABLE II
FUNCTION TABLE OF THE 4-b BEC

B[3:0]	X[3:0]
0000	0001
0001	0010
⋮	⋮
1110	1111
1111	0000

III. BINARY TO EXCESS-1 CONVERTER (BEC)

As stated in section II the main idea of this work is to use BEC instead of the RCA with in order to reduce the area and power consumption of the regular CSLA. To replace the *n*-bit RCA, an *n*-bit BEC is required. A structure and the function table of a 4-b BEC are shown in Fig. 2. and Table II, respectively.

Fig: 3. illustrates how the basic function of the CSLA is obtained by using the 4-bit BEC together with the mux. One input of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another input of the mux is the BEC output. This produces the two possible partial results in parallel and the mux is used to select either the BEC output or the direct inputs according to the control signal Cin. The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed. The Boolean expressions of the 4-bit BEC is listed as (note the functional symbols NOT, & AND. XOR)

IV. DELAY AND AREA EVALUATION METHODOLOGY OF REGULAR 128-B SQRT CSLA

The structure of the 128-b regular SQRT CSLA is shown in Fig. 4. It has five groups of different size RCA. The delay and area evaluation of last group is shown in Fig. 5. in which the

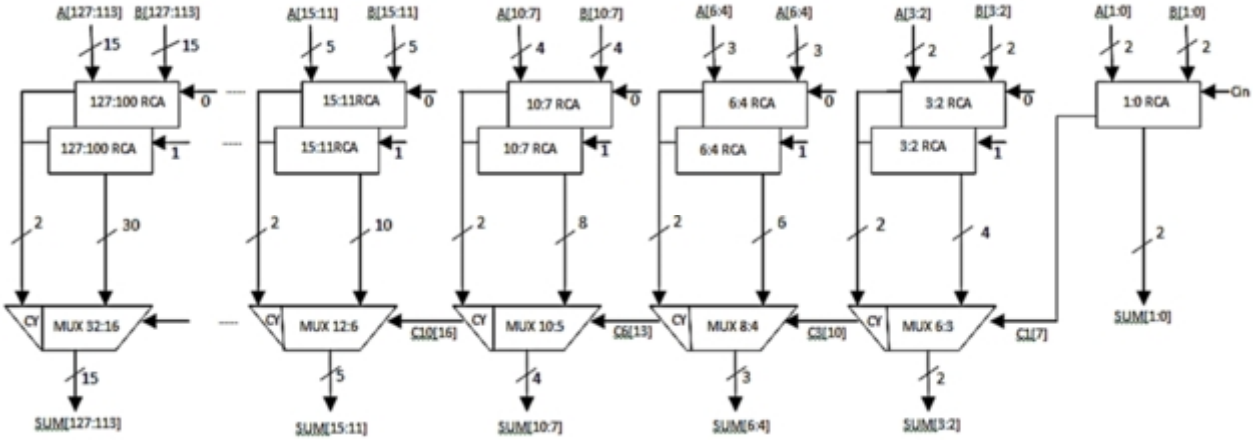

Fig.4. Regular 128-b SQRT CSLA

numerals within [ ] specify the delay values, e.g,
10 gate delays. The steps leading to the evaluation are as follows:

1) The group15 has fifteen sets of 28-b RCA. Based on the consideration of delay values of Table I, the arrival time of selection input $C112[time(t) = 46]$ of 6:3 mux is earlier than $S114[t = 8]$ and later than $S113[t = 6]$.Thus, $sum114[t = 52]$ is summation of $S3$ and $Mux[t = 3]$ and $sum113[t = 49]$ is summation of $C112$ and mux.

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Fig: 5. Delay and area evaluation of regular SQRT CSLA of group 15

2) The one set of 28-b RCA in group15 has 14 FA for cin=1 and the other set has 1 FA and 1 HA for cin=0 .Based on the area count of Table I, the total number of gate counts in group15 is determined as follows:

Gate count =447(FA+HA+Mux)

FA=337(29*13)

HA=6(1*6)

Mux=64(16*4)

Table III:
Delay and Area Count of Regular SQRT CSLA Groups

Group	Delay	Area
Group2	11	57
Group3	13	87
Group4	16	117
Group5	19	147
Group6	23	237
Group7	25	237
Group8	28	237
Group9	31	357
Group10	34	357
Group11	37	357
Group12	40	357
Group13	43	357
Group14	46	387
Group15	49	447

3) Similarly, the estimated maximum delay calculations for group2-group5[11-19] and area calculations for group2-group5[57-147] are studied [1].For the other groups in regular SQRT CSLA are evaluated and listed in Table III.

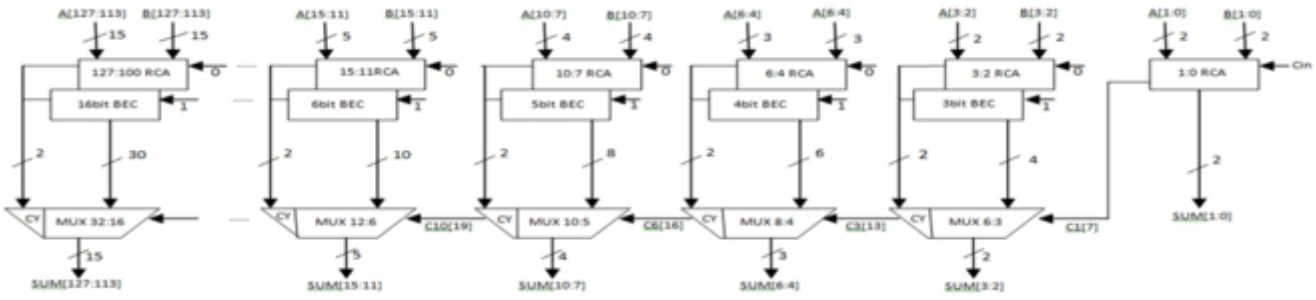

Fig: 6. Modified 128-bit SQRT CSLA

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V. DELAY AND AREA EVALUATION METHODOLOGY OF MODIFIED 128-B SQRT CSLA

The structure of the proposed 128-b SQRT CSLA using BEC for RCA with $C_{in} = 1$ to optimize the area and power is shown in Fig. 6. We again split the structure into five groups. The delay and area estimation of each group are shown in Fig. 7. The steps leading to the evaluation are given here.

1) The group15 has one 28-b RCA which has 1 FA and 1 HA for $C_{in} = 0$. Instead of another 28-b RCA with $C_{in} = 1$ a 16-b BEC is used which adds one to the output from 28-b RCA. Based on the consideration of delay values of Table I, the arrival time of selection input $C112[time(t) = 46]$ of 6:3 mux is earlier than the $S114[t = 8]$ and $Cout[t = 36]$ and later than the $S113[t = 6]$. Thus, the sum3 and final *Cout* (output from mux) are depending on *S114* and mux and partial *Cout* (input to mux) and mux, respectively. The sum2 depends on *C112* and mux.

2) For the remaining group's the arrival time of mux selection input is always greater than the arrival time of data inputs from the BEC's. Thus, the delay of the remaining groups depends on the arrival time of mux selection input and the mux delay.

3) The area count of group15 is determined as follows:

Gate count =342(FA+HA+MUX+BEC)

FA=182(14*13)
HA=6(1*6)
AND=14
NOT=1
XOR=75(15*5)
MUX=64(16*4)

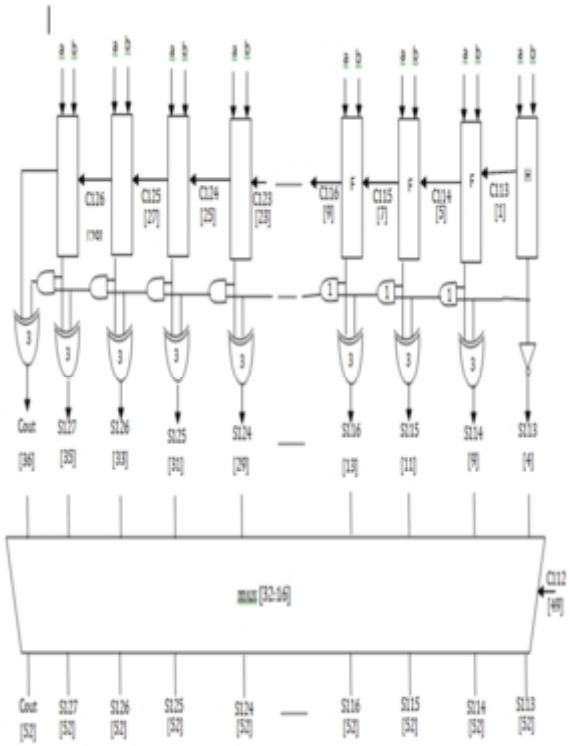

Fig: 7. Delay and area evaluation of Modified SQRT CSLA Of group 15

4) Similarly, the estimated maximum delay calculations for group2-group5 (13-22) and area calculations for group2-group (43-112) are studied [1].For the other groups of the modified SQRT CSLA are evaluated and listed in Table IV.

Comparing Tables III and IV, it is clearly understood that the proposed modified SQRT CSLA saves 882 gate areas than the regular SQRT CSLA, with only 40 increases in gate delays. To further evaluate the performance.

Table IV:

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Delay and Area Count of Modified SQRT CSLA Groups

Group	Delay	Area
Group2	13	43
Group3	16	66
Group4	19	89
Group5	22	112
Group6	25	181
Group7	28	181
Group8	31	181
Group9	34	273
Group10	37	273
Group11	40	273
Group12	43	273
Group13	46	273
Group14	49	296
Group15	52	342

VI. RESULTS

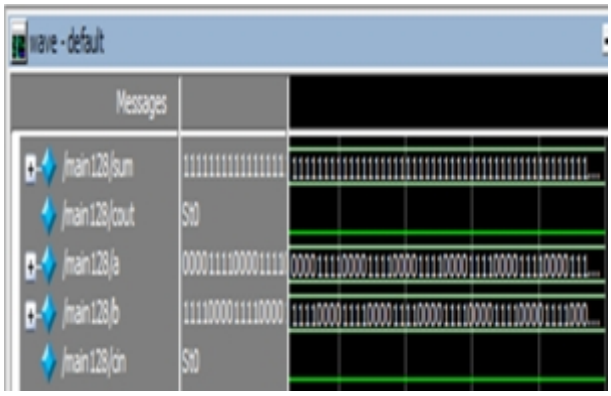

Fig: 8. Simulated Results for 128-b regular SQRT CSLA

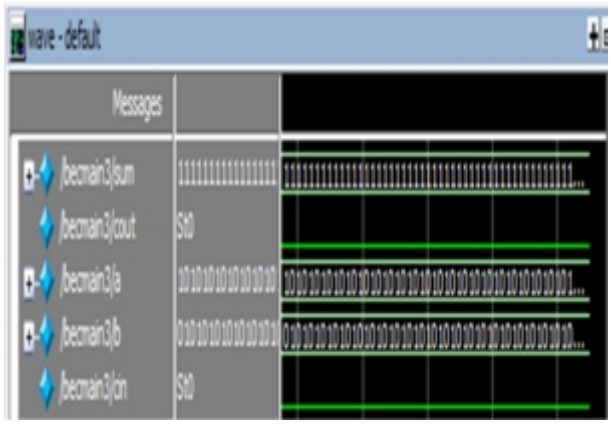

Fig: 9. Simulated Results for 128-b modified SQRT CSLA

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Table V:
Summary Result for 128-b Regular SQRT CSLA

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	251	4656	5%
Number of 4 input LUTs	438	9312	4%
Number of bonded IOBs	386	232	166%

Table VI:
Summary Result for 128-b Modified SQRT CSLA

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	295	46560	0%
Number of fully used LUT-FF pairs	0	295	0%
Number of bonded IOBs	386	240	160%

VII. CONCLUSION

A simple approach is presented in this paper to reduce the area of SQRT CSLA architecture. The reduced number of gates of this work offers the great advantage in the reduction of area. The modified CSLA architecture is simple and efficient architecture for VLSI hardware implementation in the aspect of low area. The results show that the modified SQRT CSLA has a slightly larger delay (24.276ns) than the regular SQRT CSLA (17.446ns).

VIII. FUTURE SCOPE

Area delay product of regular 128-b SQRT CSLA and modified 128-b SQRT CSLA can be experimentally performed.

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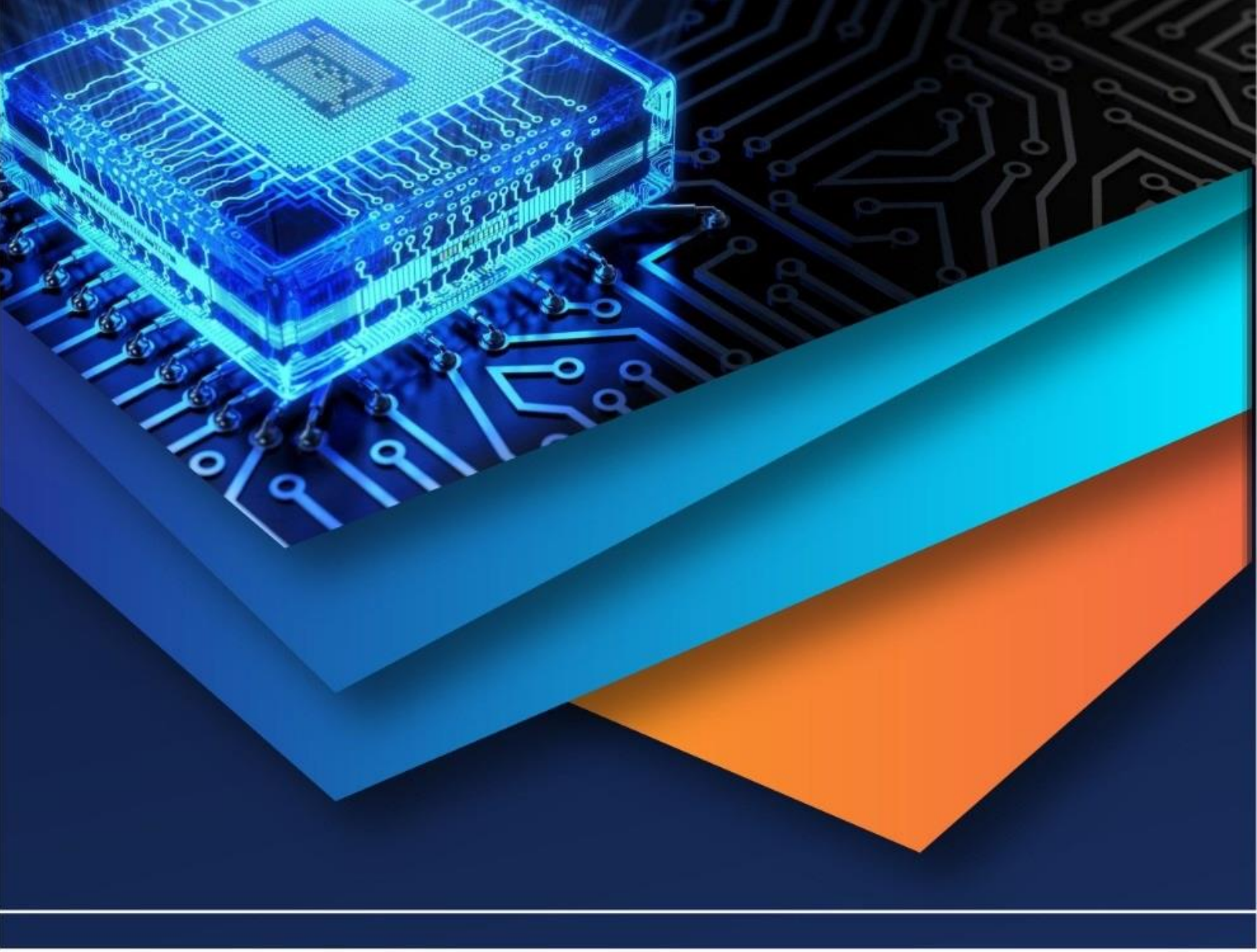

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