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Design of an Asynchronous 1 Bit Charge Sharing Digital to Analog Converter for a Level Crossing ADC

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***Abstract:** This paper presents the design of a charge sharing 1 bit DAC with pseudo resistors suitable for an asynchronous level crossing ADC. Dummy NMOS devices are added to the 1 bit DAC for reducing the charge accumulation and clock feed through giving a 81.26 % increase in SFDR for 5 kHz input frequency compared to the 1 bit DAC with only pseudo resistors. The asynchronous control logic for the DAC is designed digitally and optimized for lower power consumption. The DAC and its control logic has been designed using 180nm technology in cadence using a supply voltage of 0.8 V and consumes an average power of 2.323 nW.*

***Keyword:** Digital to Analog Converters (DAC), Analog to Digital Converters (ADC), Asynchronous, Level crossing, pseudo resistors*

I. INTRODUCTION

Asynchronous ADC architectures are emerging as an excellent alternative for replacing synchronous ADCs in various applications such as portable and implantable biomedical signal sensing devices, remote environmental monitors and sensors, military applications, magnetic disk reader, optical disk readers and wireless applications such as audio devices and cellular telephones. The advantages of asynchronous circuits compared to their synchronous counter parts are higher speed, lower power consumption, and smaller area, immunity to metastable behaviour, less clock skew and low susceptibility to electromagnetic interference.

Level crossings ADCs are asynchronous ADCs that generate output samples only when the input signal crosses a threshold level [1]. Level crossing ADCs offers lower sampling rate, power consumption and area than synchronous ADCs. Level crossing ADC has been mainly used in embedded sensing systems, such as environmental sensors (temperature, pressure sensors), implantable biomedical applications, hearing aids and ultrasound applications [2]-[7], [10],[11].

This paper presents the design of a charge sharing 1 bit DAC with pseudo resistors and additional dummy NMOS devices for a level crossing ADC. A digital DAC logic using gates and latches for the control of the 1 bit DAC asynchronously is also designed in this paper.

In this paper, section II discusses previous literatures on DAC used in level crossing ADCs. Section III gives the circuit implementation followed by results and discussion in section IV. Section V gives the conclusion of the paper.

II. PREVIOUS LITERATURE

Level crossing ADC generates output samples whenever the input signal crosses a threshold level and the time between the level crossing samples are quantized and encoded in uniform steps. Level crossing ADC architectures in previous literature can be generally classified into two types: LC ADC using feedback DAC [2], [3],[5] and LC ADC with flash ADC like architecture [4]. A general architecture of LC ADC using feedback DAC consists of feedback DAC, comparators, counter and timer as shown in the figure 1. The feedback loop with DAC keeps the comparison window of the comparators around the input signal. The up/down counter functions as a digital integrator and the timer records the time between two samples. The DAC and comparators power consumption dominates the overall power consumption. The benefits of the DAC are rail to rail input swing, decreased settling time, decreased leakage and decreased output drift.

N-bit DACs were previously used in all level crossing ADC implementation. They were implemented using resistor string DACs and capacitive DACs. Resistor string DAC used in [8] was used to generate the varying comparison window boundary signals for the varying input signal. The use of resistor string DAC simplified the design and prevents the glitches in the reference signals. A capacitive DAC structure based on charge sharing principle was used in [9] which generate the varying comparison interval. A hybrid switched-capacitor/resistor-string architecture was used for implementing DAC in [10][12]. The 2 DACs used in this architecture create the threshold levels which bound the input signal from above and below. The resolution of the DAC is increased

by 2 bits with respect to the quantizer resolution and this allows the calibration of comparator offset below 1 LSB. The additional benefits of the DAC are rail to rail input swing, decreased settling time, decreased leakage and decreased output drift. But, the resistor string DACs and capacitive DACs consumes large power and area. In [11], a 1 bit DAC with 2 branch structure was proposed. The settling time of the DAC is relaxed by using three branched architecture [2]. The 1 bit DAC offers lower power consumption, lower area, higher linearity, lower cost as most of the processing takes place in digital domain.

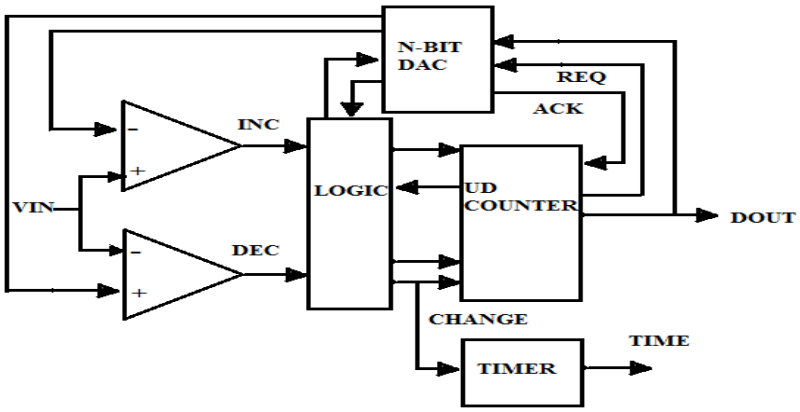

Fig. 1. General LC ADC architecture using feedback DAC

III. CIRCUIT IMPLEMENTATION

This section discusses the implementation of asynchronous LC ADC using feedback DAC. The block diagram of the LC ADC for which the 1 bit DAC was designed is shown in figure 2. The 1 bit DAC fixes the comparison window of the LC ADC by injecting offset into the input. The 1 bit DAC tracks the input signal V_{IN} .When there is a level crossing, the DAC performs subtraction or addition on the tracked input and gives $V_{ON.}$ $V_{H,}$ V_L and V_M are the reference voltages such that difference between V_H and V_L is 2LSB and V_M is given by V_H+ V_L/2.The lower comparator detects the varying direction of signal by comparing output of DAC with V_M. The upper comparator compares V_{ON} with V_H or V_L as determined by the MUX.

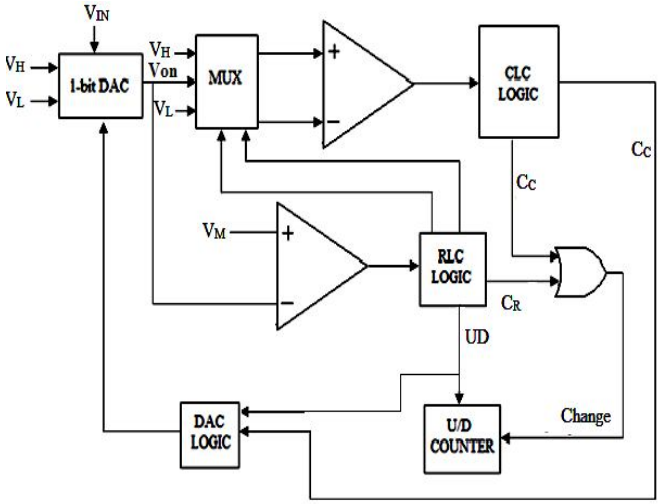

Fig. 2. The LC ADC architecture [2]

A 1 bit DAC used to fix the comparison window with offset injection to the input is shown in figure 3. Fixing the comparison window will lower the power consumption and reduce the design complexity of level crossing ADC. The 1 bit DAC consists of three branches with the middle branch for tracking. The left and right branches of 1 bit DAC are used for positive and negative offset injection. The DAC logic designed digitally as shown in figure 4 generates the required control signals for 1 bit DAC with CC and UD as input. The control signals for the 1-bit DAC are shown in figure 5.

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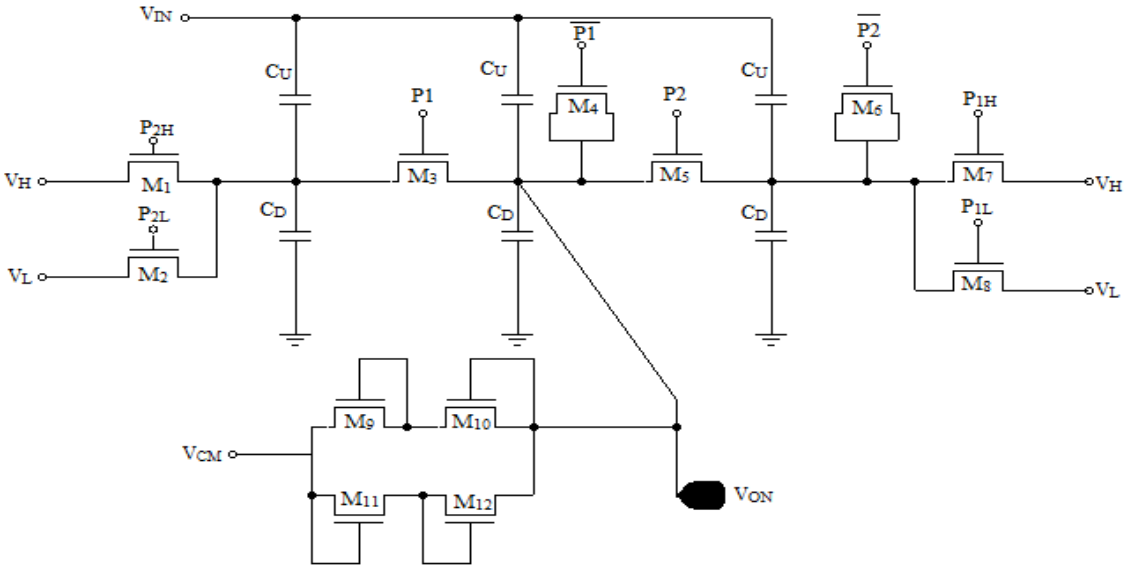

Fig. 3 Circuit digram of 1-bit DAC

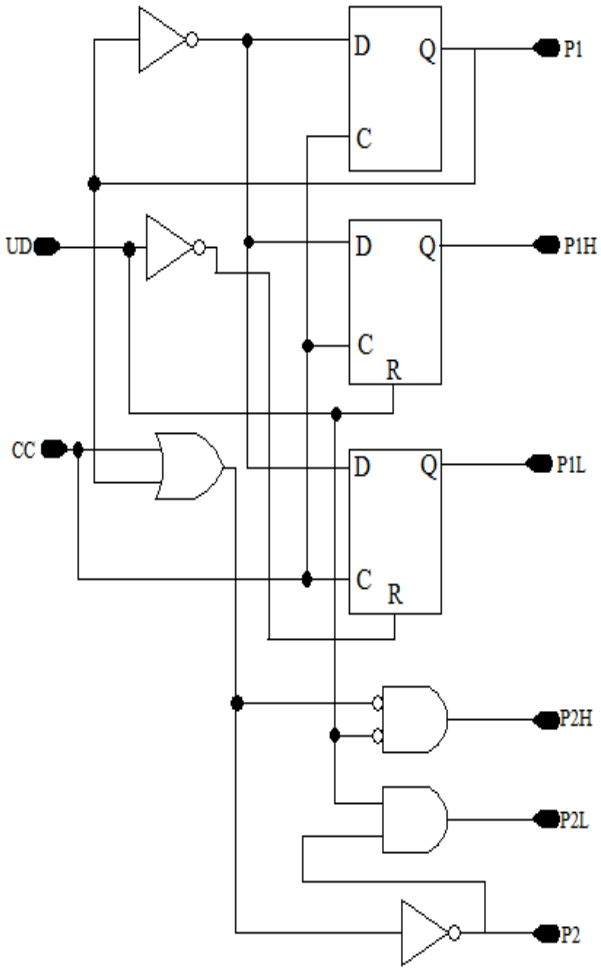

Fig. 4 The DAC logic circuit diagram

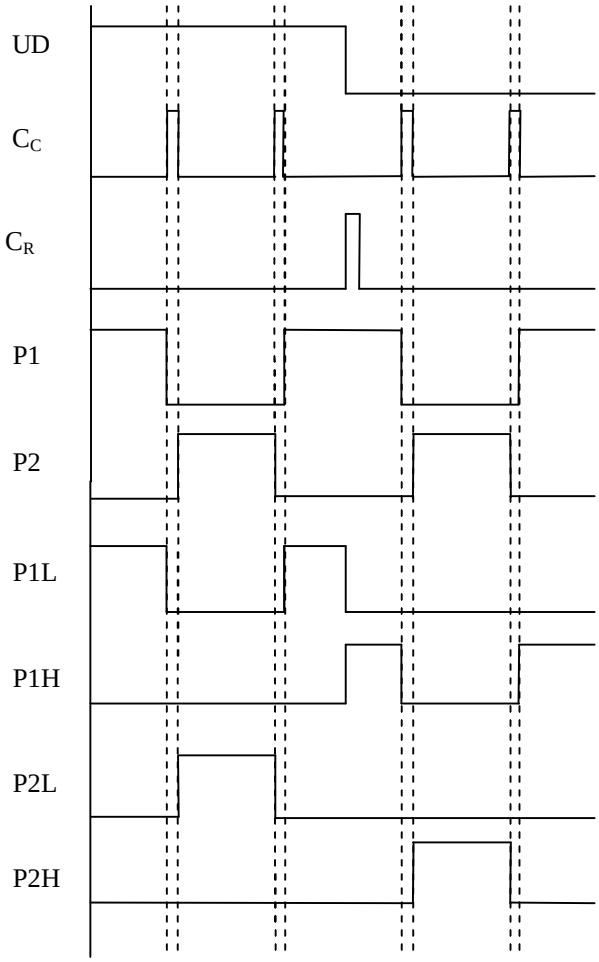

Fig. 5 The DAC logic control signals

When the output of the DAC, V_{ON} stays within the comparison window between V_M and V_H, the left and right branches are connected to V_L. When V_{ON} crosses V_H, CLC logic gives a high C_C. When C_C pulse is high, DAC logic gives a low P_1 and P_{1L}.When P_1 is low, the left offset injection branch is disconnected from the tracking branch. Then P_2 and P_{2L} go high which connects the right offset injection branch to the tracking branch and discharges the left offset injection branch. The charge is shared between the right offset injection branch and tracking branch and thus V_{ON} decreases by 1 LSB.

When V_{ON} stays within the comparison window between V_L and V_M, the left and right branches are connected to V_H. The CLC logic gives a high C_C and the DAC logic gives a low P_1 and P_{1H}, when V_{ON} crosses V_L. So the left offset injection branch is disconnected from the tracking branch. Then P_2 and P_{2H} go high which connects the right offset injection branch to the tracking branch and charges the left offset injection branch. The charge on right offset injection branch connected to V_H when V_{ON} was between V_L and V_M is added to charge on tracking branch and increases V_{ON} by 1 LSB.

The switches of the 1 bit DAC are constructed using NMOS switches. A pseudoresistor comprising M_9, M_{10}, M_{11} and M_{12} is used to prevent unwanted accumulation of charge resulting from any mismatch in capacitors during offset injection. It is also used to fix the DC common mode voltage at the output node when the input signal does not vary. The dummy devices M_4 and M_6 are added to the 1 bit DAC for further reducing the charge accumulation and clock feed through. When M_3 is off, M_4 is on and the channel charge deposited by M_3 on C_D is absorbed by M_4.Similarily M_6 reduce charge accumulation by M_5.

IV. RESULTS AND DISCUSSION

A 1 bit DAC was implemented in cadence virtuoso using 180 nm technology. A supply voltage of 0.8 V has been used for both analog and digital supply. An input voltage of $800mV_{PP}$ ranging from 5 Hz to 5 kHz is given to the DAC. The difference between the reference voltages, V_H and V_L is widened to 2 LSB. A value of 16mV is chosen as 1 LSB in this design. C_U is the unit capacitor

and C_D is chosen 16 times larger and so 16/17 of the input variations fall on the upper plate of C_D. Switches should be made as small as possible and capacitors should be made as large as possible. A value of 200fF is chosen for C_U and value of 3.2pF is chosen for C_D for our targeted resolution.

The 1 bit DAC offers several advantages such as lower power consumption, lower area, higher linearity and lower cost as most of the processing takes place in digital domain. Also the input voltage range is not limited and so the input signal swing is higher. The input supply can exceed supply voltage as the tracked input voltage is increased or decreased by 1 LSB as soon as it reaches the fixed comparator level. The power consumption of the array is much lower than conventional architectures and consumes a power of only 2.32nW.

The output V_{on} of the 1 bit DAC is shown in figure 6.The layout of the DAC is shown in figure 7. The capacitor array formed by C_U and C_D dominates the area of the 1 bit DAC as shown in the layout.

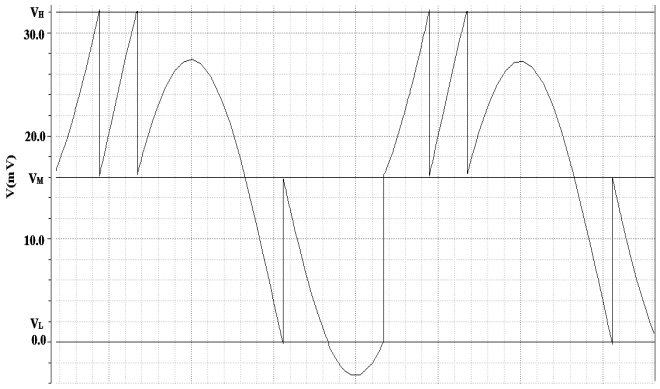

Fig. 6 The output of DAC

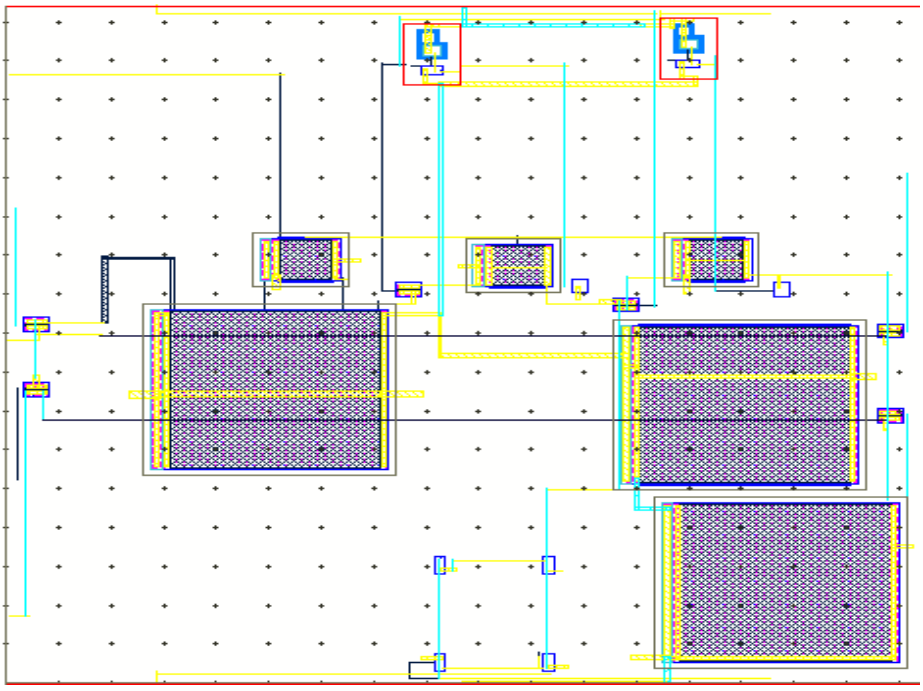

Fig. 7 The Layout of DAC

The FFT plot of the 1 bit DAC with pseudoresistors and dummy devices is shown in figure 8 and the FFT plot of the 1 bit DAC with pseudoresistors and without dummy devices is shown in figure 9 for an input frequency of 5 kHz and sampling frequency of 13.3 kHz. Addition of dummy device gives a increase of 81.26 % in SFDR for 5 kHz input frequency compared to the design without dummy device. Figure 10 shows the SNR of 1 bit DAC as function of sampling frequency.

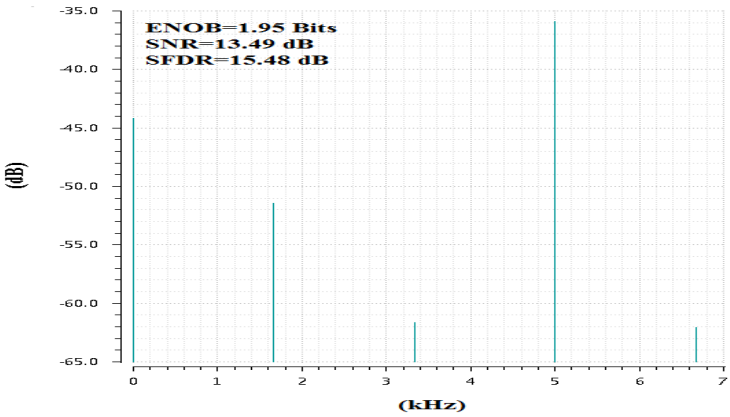

Fig. 8 The FFT plot of 1 bit DAC with pseudoresistors and dummy devices

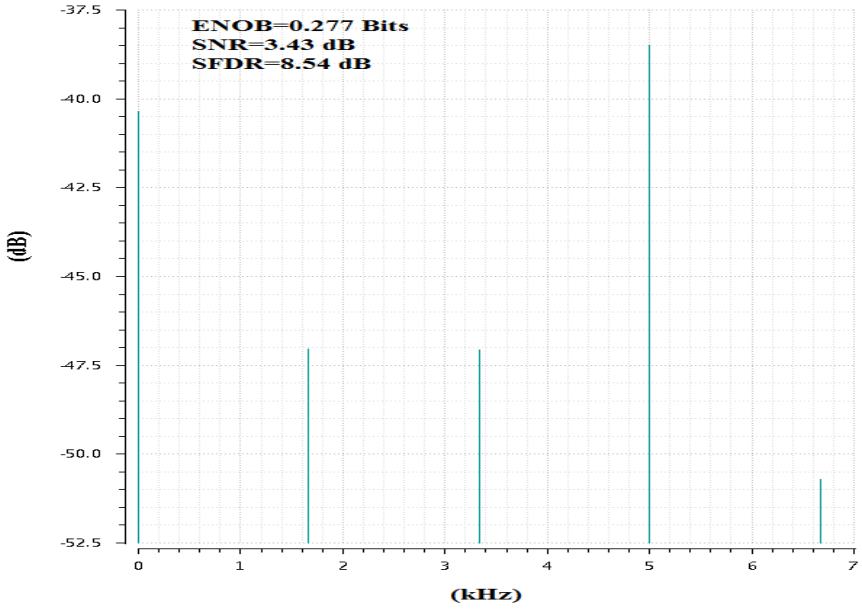

Fig. 9 The FFT plot of 1 bit DAC with only pseudoresistors

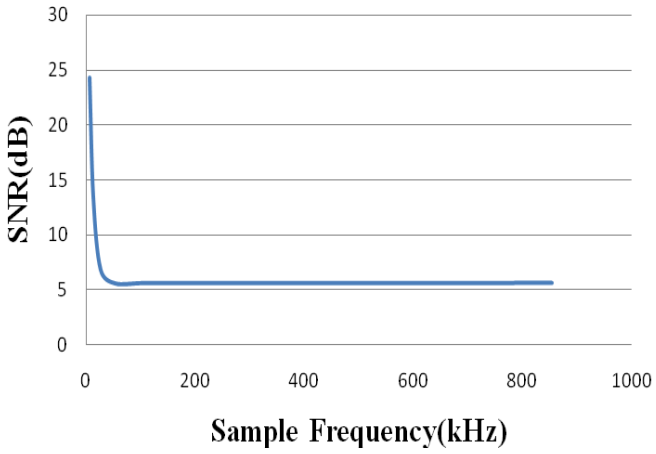

Fig. 10 SNR as function of sample frequency

V. CONCLUSION

A 1 bit DAC suitable for level crossing ADC has been designed and simulated in cadence using 180 nm technology. The DAC with 3 branches for tracking and positive or negative offset injection has improved settling time and accuracy with pseudoresistors and dummy NMOS devices to reduce charge accumulation and clock feedthrough. The DAC logic to generate the control signals has been designed digitally and carefully scaled to reduce the power consumption and area.

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