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# Performance Enhancement of Reversible Binary to Gray Code Converter Circuit using Feynman gate

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***Abstract:*** ***In the field of engineering design and development, nanometer technology implementation minimizes the power consumption of logic circuits and makes it energy efficient. Reversible logic circuits design is one of the promising trending engineering developments that have importance due to less dissipation of heat and low power consumption. In digital systems, code converter circuits is used for enhancing security of data, reducing the complexity of arithmetic operations and thereby reducing the hardware required, dropping the level of switching activity leading to more speed of operation and power saving etc. Also, for the efficient and faster implementation we need to optimize the quantum cost and garbage outputs for final implementation. Normally delay has been very least concerned in the optimization in the design implementation. In this proposed work, we have presented the novel design of the reversible Binary to gray converter that is based on the optimization based on the delay, quantum cost and garbage outputs. The synthesis is done on Xilinx 14.1 tool and X power analyzer has been used for the validation of the power consumption.***

***Keywords: Reversible logic circuits, Quantum cost, Garbage outputs, Delay reduction, Optimization.***

## I. INTRODUCTION

The major concern in miniaturization of the chips is that it dissipates more heat and thus power is wasted. In researches, it is shown that the actual energy required for the computation is very less than the actual power dissipated. Reversible logic circuits design is one of the promising trending engineering developments that have importance due to less dissipation of heat and low power consumption. Earlier, Landauer (1961) showed that every bit of information loss will generate KTln2 Joules of heat energy, where K is Boltzmann's constant and T is the operating Temperature. Later Bennett (1973) proved that the energy loss in a circuit can be eliminated by using reversible gates for the designing of circuits. Code converters are combinational circuits and considered as important part of the digital design. These circuits find its application improving the security of data, decreasing the complexity of arithmetic operations and reduce the hardware requirement. Reversible logic circuits have the same number of inputs and outputs, and have one-to-one mapping between vectors of inputs and outputs; thus the vector of input states can be always reconstructed from the vector of output states [1].Consequently, a computation is reversible, if it is always possible to uniquely recover the input, given the output.

Synthesis of reversible logic circuits is significantly more complicated than traditional irreversible logic circuits because in a reversible logic circuit, we are not allowed to use fan-out and feedback. In digital systems code conversion is a widely used process for reasons such as enhancing security of data, reducing the complexity of arithmetic operations and thereby reducing the hardware required, dropping the level of switching activity leading to more speed of operation and power saving etc.In this proposed work, we have presented the novel design of the reversible Binary to gray converter that is based on the optimization based on the delay , quantum cost and garbage outputs.

## II. REVRSIBLE LOGIC GATES

Reversible gates are circuits in which number of input is equal to number of output and therefore it is one to one mapping between the vector input and output. It is defined as the number of input to be maintained constant at either 0 or 1 in order to synthesize the given logical function. Some of the important parameters of reversible logic gates are-

*A.* Reversible Gates- The number of reversible gates used to realize the function and should be as minimum as possible so as to reduce delay, quantum cost and area
*B.* Quantum Cost: This refers to the cost of the circuit in terms of reversible gates used and should be minimum to reduce the circuit cost.
*C.* Garbage Output: This refers to the no. of outputs which are not used and therefore it should be as small as possible.
*D.* Constant Input: This refers to the no. of inputs to be maintained constant at either logic 0 or logic 1 and should be minimum.

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*E.* Delay: The delay is the propagation delay of the critical path where, critical path is the path to the output which has the maximum delay and so it should be minimum.

*F.* Fan-ut: Fan-out is not allowed in reversible logic circuits

Reversible computation in a system can be performed only when the system comprises of reversible gates. A circuit/gate is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one-to-one correspondence between its input and output assignments.

The reversible circuits form the basic building block of quantum computers.

NOT GATE NOT gate is a 1×1 gate with quantum cost of zero. It is only reversible gate among the conventional logic gate.

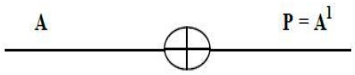


Fig. 1 NOT Gate

CNOT GATE (FEYNMAN GATE): It is 2×2 reversible gate having one quantum cost [12]. This is a gate having mapping (A, B) to (P=A, Q=A ⊕B) where A, B are inputs and P, Q are outputs.


Fig. 2 Feynman Gate

PERES GATE: It is a 3×3 Peres gate with the minimum cost 4. Peres gate is a three input and three output 3×3 gate with the mapping (A,B,C) to (P=A, Q=A ⊕B, R=A.B ⊕ C ), where A,B,C are the inputs and P,Q,R are the output.

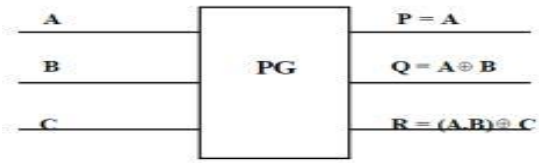


Fig. 3 Peres Gate

TOFFOLI GATE: Toffoli gate is one of the most popular reversible gates and it has quantum cost of 5. This is a 3×3 reversible gate with two of its outputs are as input with the mapping (A, B, C) to (P=A, Q= B, R=AB ⊕C) where A, B, C are inputs and P, Q, R are outputs respectively.

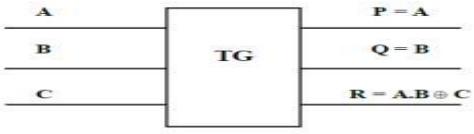


Fig. 4 Toffoli Gate

FREDKIN GATE: Fredkin gate has 5 quantum cost and it is a 3×3 reversible gate. It maps (A, B, C) to (P=A, Q= A'B +AC, R=AB + A'C), where A, B, C are the inputs and P, Q, R are the outputs.

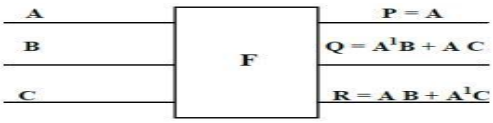


Fig. 5 Fredkin Gate

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TR GATE: TR gate are also reversible gate having 6 quantum cost therefore it is realize in a different implementation with quantum cost is equal to 6 or less than 6. It has three input and three output mapping as (P=A, Q=A ⊕B, R= (A ⊕ B') C), where the A, B, C are the inputs and P, Q, R are the outputs, respectively

.

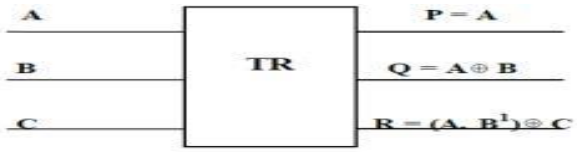


Fig.6 TR Gate

NG GATE:NG GATE has less quantum cost, it is a 3x3 gate and its logic circuit and its quantum implementation is as shown in the figure. It has inputs A, B, C and outputs are P, Q, R then A reversible logic gate is an n-input n- output logic device with one- to-one mapping. . NG gate is a reversible gate which is mostly used in quantum computers, low power CMOS technology, etc. Reversible NG gate has three input and three outputs, it is a gate which has quantum cost less, power consumption less, etc

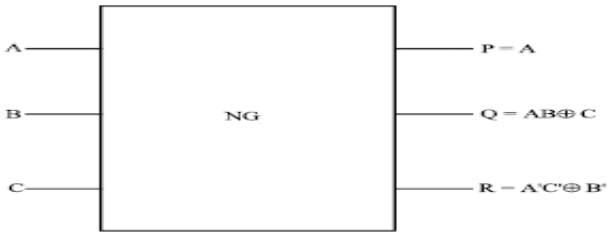


Fig.7 NG Gate

BJN GATE: It is a 3x3 gate and its logic circuit and its quantum implementation is as shown in the figure. It has quantum cost five.

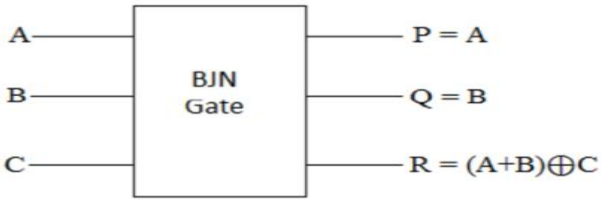


Fig.8 BJN Gate

MCL GATE: MCL Reversible logic gate is an n-output logic n-output device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. The MCL gate is a 3x3 gate which maps the inputs A, B, C to P=(B+C)', Q=(A+B)', R=A. MCL gate has 3-inputs and 3-outputs. It is a reversible MCL gate which has constant inputs and constant outputs. MCL gate has power consumption less and it is used in many fields like nano technology, CMOS technology, communication, etc.

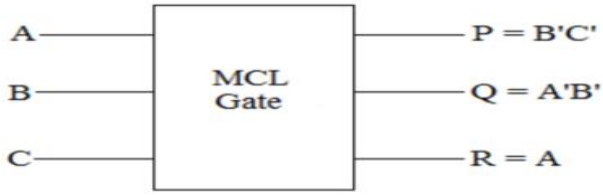


Fig.9 MCL Gate

SCL GATE: It is a 4x4 gate and its logic circuit is as shown in figure. It has 4-inputs and 4-outputs where inputs are A, B, C and D and outputs are P, Q, R and S then P=A, Q=B, R=C and S=A (B+C) ⊕D .SCL gate is not much important than remaining reversible logic gates Reversible logic gate are now presently used more than logic gates because its quantum cost is less, power consumption

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is less. SCL gate has 4-inputs in this 3-outputs are same as input but remaining only 1-input is different it is the combination of A, B and C. These reversible logic gates are mostly used in quantum computing, CMOS technology, nanotechnology, etc.

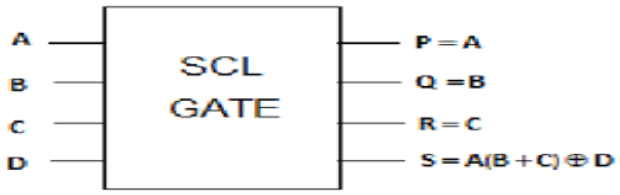


Fig.10 SCL gate

## III. PROPOSED DESIGN

Design constraints for reversible logic circuits [13]:

*A.* Reversible logic gates do not allow fan-outs.
*B.* Reversible logic circuits should have minimumquantum cost.
*C.* The design can be optimized so as to produceminimum number of garbage outputs.
*D.* The reversible logic circuits must use minimum number of constant inputs.
*E.* The reversible logic circuits must use a minimumlogic depth or gate levels

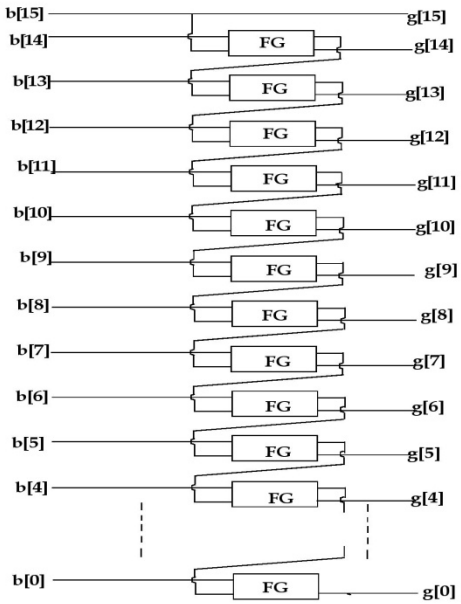


Fig.11 Block diagram of Reversible Binary to gray converter using Feynman Gate

Binary to Gray code converters used to reduce switching activity by achieving single bit transition between logical sequences.

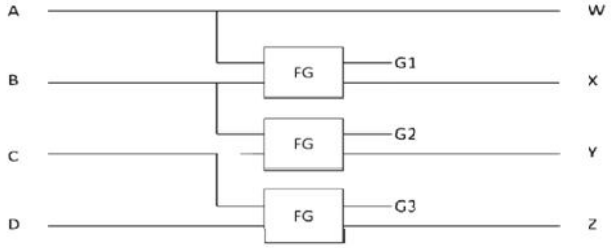


Fig 12Circuit Diagram of Reversible Binary to Gray Code Converter

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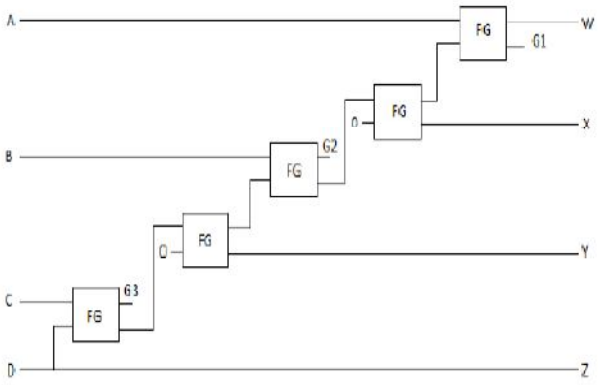


Fig 13 Circuit Diagram of Reversible Gray to Binary Code Converter

If Input vector is I(D,C,B,A) then the output vector o(Z,Y,X,W). The circuit is constructed with the help of Feynman Gate (FG) gate and Table 1 shows the truth table of FG gate and figure 12 and figure 13 shows the circuit diagram of reversible Binary to Gray code converter & Gray to Binary code converter. Feynman Gate (FG) can be used as a copying gate. Since a fan-out is not allowed in reversible logic, this gate is useful for duplication of the required outputs. [13]

| A | B | P | Q |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 |

Table. 1 Truth table of Feynman Gate

## IV. RESULTS & DISCUSSION

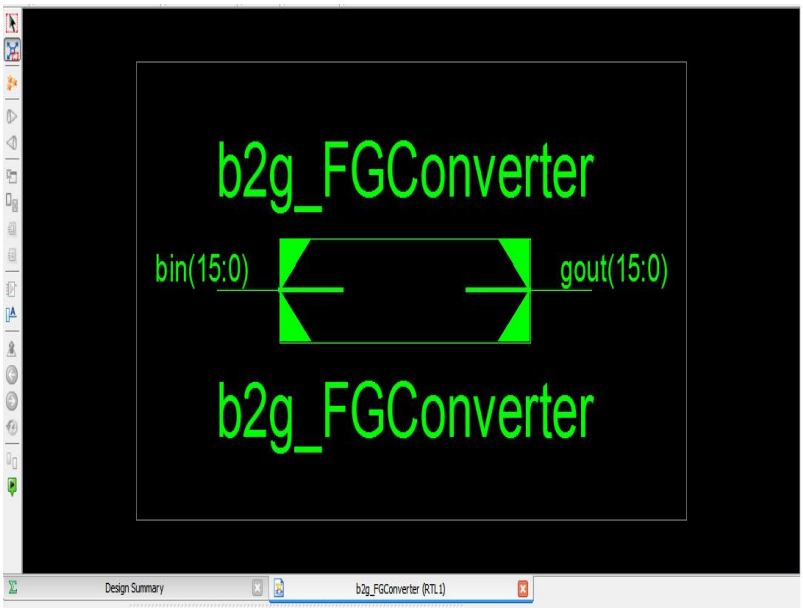


Fig.14 Technology view of the proposed design

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The figure 14 presents the technology view of the proposed design. The functional block design of the proposed design consists of the 16-bit logical input in binary format and the output 16-bit gray converted output.


Fig.15 Simulation results of the proposed design

Figure 15, presents the simulation results of the proposed design. The input is the 16-bit binary sequence and output is converted gray code. In the simulation results:

*A. Case- 1:*

1) *Input:* Din = 0000000000000001
2) *Output:* Dout = 0000000000000010

*B. Case- 2:*

1) *Input:* Din = 0000000000000011
2) *Output:* Dout = 0000000000000100


Fig. 16Detailed RTL block diagram of the proposed design

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Figure 16, presents the detailed block diagrammatic representation of the proposed design. The designed architecture consists of the basic element modified FG-gate used for the implementation of the proposed converter design.
The Synthesis report and delay report has been presented as shown in Figure 17 and Figure 18.

```
=========================================================================
*                     Synthesis Options Summary                         *
=========================================================================
---- Source Parameters
Input File Name                    : "b2g_FGConverter.prj"
Input Format                       : mixed
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "b2g_FGConverter"
Output Format                      : NGC
Target Device                      : xc3s100e-5-vq100


==
=========================================================================



=========================================================================
*                            Final Report                               *
=========================================================================
Final Results
RTL Top Level Output File Name     : b2g_FGConverter.ngr
Top Level Output File Name         : b2g_FGConverter
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 32

Cell Usage :
# BELS                             : 15
#      LUT2                        : 15
# IO Buffers                       : 32
#      IBUF                        : 16
#      OBUF                        : 16
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s100evq100-5

 Number of Slices:                        9  out of    960     0%
 Number of 4 input LUTs:                 15  out of   1920     0%
 Number of IOs:                          32
 Number of bonded IOBs:                  32  out of     66    48%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------


=========================================================================


Timing Summary:
---------------
Speed Grade: -5

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
```

Figure 17 Synthesis Report

```
   Maximum combinational path delay: 5.776ns

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 31 / 16
-------------------------------------------------------------------------
Delay:               5.776ns (Levels of Logic = 3)
  Source:            bin<15> (PAD)
  Destination:       gout<14> (PAD)

  Data Path: bin<15> to gout<14>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             2   1.106   0.532  bin_15_IBUF (gout_15_OBUF)
     LUT2:I0->O            1   0.612   0.357  X1/Mxor_Q_Result1 (gout_14_OBUF)
     OBUF:I->O                 3.169          gout_14_OBUF (gout<14>)
    ----------------------------------------
    Total                     5.776ns (4.887ns logic, 0.889ns route)
                                      (84.6% logic, 15.4% route)

=========================================================================



-->

Total memory usage is 251716 kilobytes
```

Fig 18 Delay Report of Proposed design

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Similarly Power Report of proposed design is shown in Figure 19.

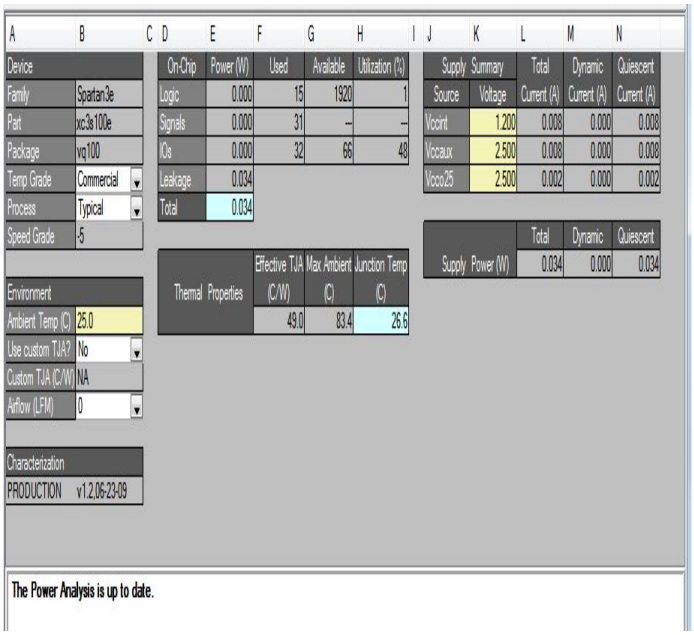


Fig 19 Power Report of proposed design

## V. APPLICATIONS OF REVERSIBLE GATES

Reversible computing may have applications in computer security and transaction processing, but the main long-term benefit will be felt very well in those areas which require high energy efficiency, speed and performance .it include the area like

*A.* Low power CMOS.
*B.* Quantum computer.
*C.* Nanotechnology.
*D.* Optical computing.
*E.* DNA computing.
*F.* Computer graphics.
*G.* Communication.
*H.* Design of low power arithmetic and data path for digital signal processing (DSP).
*I.* Field Programmable Gate Arrays (FPGAs) in CMOS technology.

## VI.CONCLUSION

In this proposed work, we have presented the novel design of the reversible Binary to gray converter that is based on the modified FG gate based on the delay and energy efficiency. The simulation results show the RTL synthesis of the structure of the converter.
Thus, we found our proposed design to be efficient for the power, and quantum cost due to use of the reversible gates. It reduces the power consumption and the quantum cost of the circuit. Similarly, the GDI technique has been studied and found to be reducing the number of transistors and thus reducing the delay.

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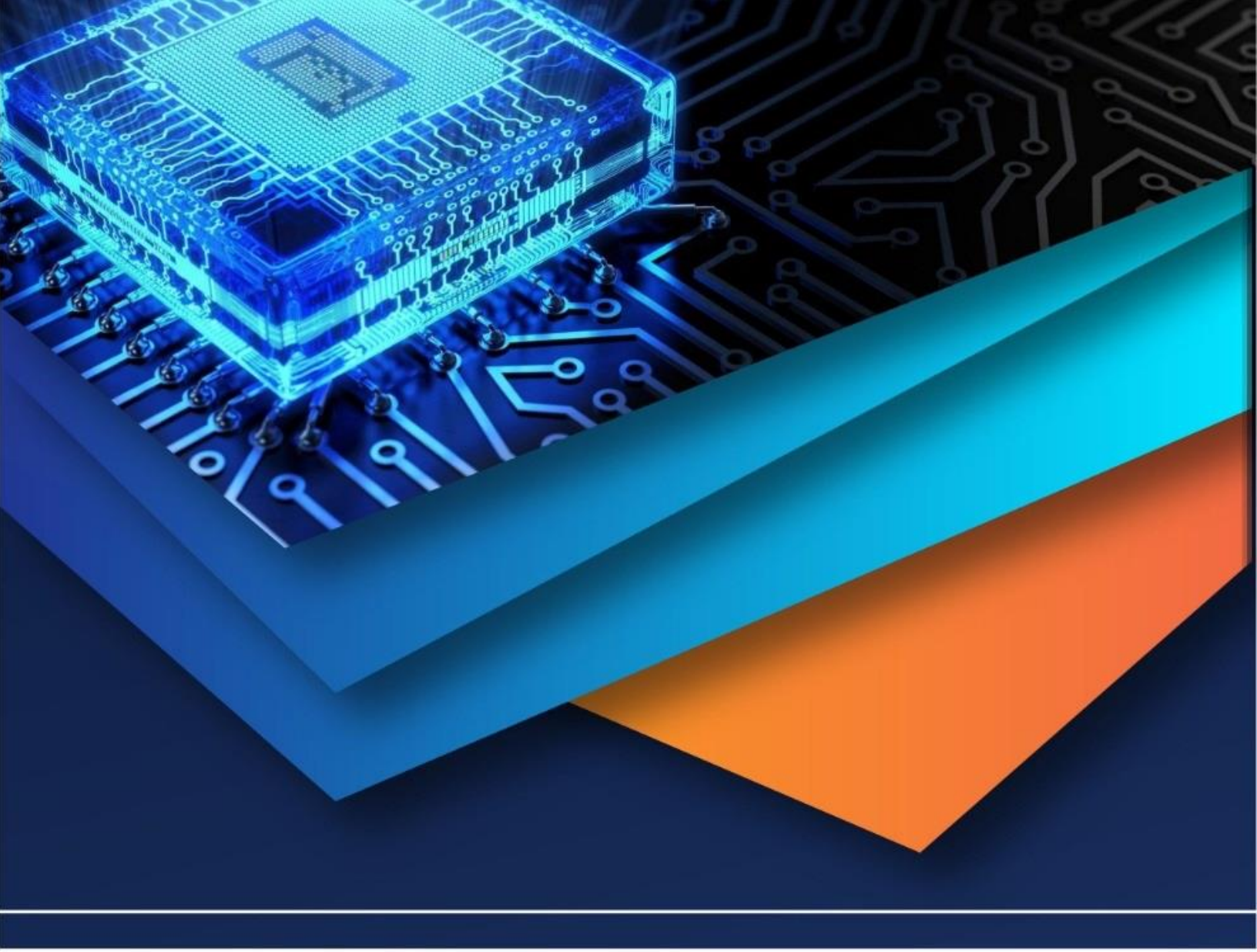

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