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An ASIC level Implementation of Modified CSA to Optimize Low Power and High Speed Using Brent Kung Adder

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Abstract: ***Adder is used to perform the Addition of two numbers. Adder is also forms the integral part of ALU. Different algorithms in digital signal processing such as FIR and IIR and also employed using adder. The most important constraint is speed. The important constraints in VLSI design areas are low power, high speed and data logic design. In carry select adder the possible values of input carry are 0 and 1. The architecture of CSA are design by Brent Kung adder in order to reduce the power and delay of adder. In proposed model a modification is done by using 16-bit inputs instead of 32-bit inputs to improve the speed and reduce the power. Here using D-latch block, initially when en=1, the output of the Brent Kung adder is fed as input to the D-latch and the output of the D-latch follows the input and given as an input to the multiplexer. when the en=1, the last sate of the D-latch input is trapped and held in the latch and therefore the output from the Brent Kung adder is directly given as a input to the multiplexer without any delay. Here the 32-bit CSA adder using Brent Kung adder of the physical design is designed.***
Keywords: Adders, delays, power demand, optimization, digital signal processing

I. INTRODUCTION

The Proposed design is mainly implemented to achieve Low-Power and high speed design implementation. Here in the Proposed Design System we go for 32-bit input is given to the blocks of Brent Kung adder. The circuit operating speed is increased and it takes less power compared to existing method. In this Proposed project, There is a huge scope in this project as it is applicable for real-time use and is more efficient multipliers are used ie, DSP to execute various algorithms like FFT,FIR and IIR with ease. By this ultimately, we achieved Low-Power and delay consumption. Here in the Proposed Design System we go for 32-bit Brent Kung adder is used in this system. Hear existing system is 16-bit circuit so calling by two time's 16-bit circuit, therefore 32-bit proposed system is formed. The main aim of the project is used for low power and high speed Purpose ie., the carry select adder operation is to improve low power and high speed of the circuit by using BK Adder. The proposed design 180-nm technology used in cadence tool.

II. RELATED WORK

When the Modified Brent Kung CSA is simulated and synthesized, the area and power is less in the modified CSLA but the delay is slightly increased. So we can improve the above structure in terms of less delay and higher speed by replacing the BEC with a D-Latch. Thus an improved Carry Select Adder with D-Latch. Here the Binary to Excess-1 Converter is replaced with a D-Latch. Initially when en=1, the output of the Brent Kung adder is fed as input to the D-Latch and the output of the D-latch follows the input and given as an input to the multiplexer. When en=0, the last state of the D input is trapped and held in the latch and therefore the output from the BK adder is directly given as an input to the multiplexer without any delay. Now the multiplexer selects the sum bit according to the input carry which is the selection bit and the inputs of the multiplexer are the outputs obtained when en=1 and 0.
Carry select adder algorithm doesn't well if the input bit length is more. Thus, if we use Brent Kung adder at greater bit length and Brent Kung adder at lesser bit length then we can compensate the limitations of the algorithm at a greater efficient. Thus, the Multiplier becomes more efficient and delay will reduce to greater extent. By designing the whole processor architecture, we can reduce the Power and Delay at lower efficient. The circuit operating speed is increased and it takes less power compared to existing method.

III.PROPOSEDMETHOD

The Proposed design is mainly implemented to achieve Low-Power and high speed design implementation. Here in the Proposed Design System we go for 32-bit Brent Kung adder is used in this system. Hear existing system is 16-bit circuit so calling by two

time's 16-bit circuit, therefore 32-bit proposed system is formed. It is finest algorithm for binary multiplications in terms of area and delay. However, when input bits increase, delay will also increase and the partial products are summered in a ripple fashion. Suppose for an 8-bit multiplication, we require 14 adders which are added in a ripple fashion. If we try to compensate the delay, then it will cause the increases in area. Thus, carry select adder algorithm doesn't well if the input bit length is more. Thus, if we use Brent Kung adder at greater bit length and carry select adder using Brent Kung adder algorithm at lesser bit length then we can compensate the limitations of the algorithm at a greater efficient. As a result, the Multiplier becomes more efficient and delay will reduce to greater extent. By designing the whole circuit architecture, we can reduce the Power and increase the speed at lower efficient. Hence Low-Power and less delay is being achieved.

The Processor architecture contains mainly BK Adder, D-latch, multiplexer. Here the different blocks in Brent Kung adder there are 4 types are used in this. 2-bitBK Adder, 3-bit BK Adder, 4-bit BK Adder and 5-bit BK Adder and also same thing in D-latch Circuit. The inputs are given to the blocks of BK Adder 32-bits like [0-31] bits. Here the basic diagram is 16-bit input so we calling two times. The Cin input is initial ZERO the outputs of the 2-bit BK Adder contains two outputs one is given to the input of MUX 6:3 and other one is SUM [1:0]. The 2-bit BK Adder contains 3 inputs A, B and en pin. The out puts of the 2-bit BK Adder contains 2 outputs sum and carry these outputs are given to the inputs of the 2-bit D-latch block and also enable pin

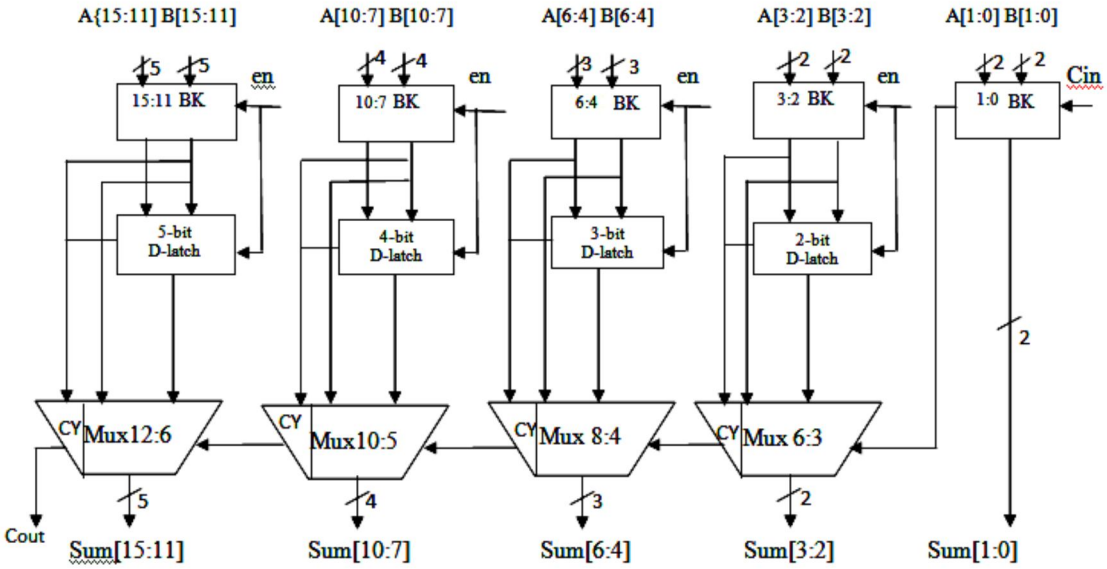

Fig: Block Diagram of 16-bit Brent Kung carry select adder

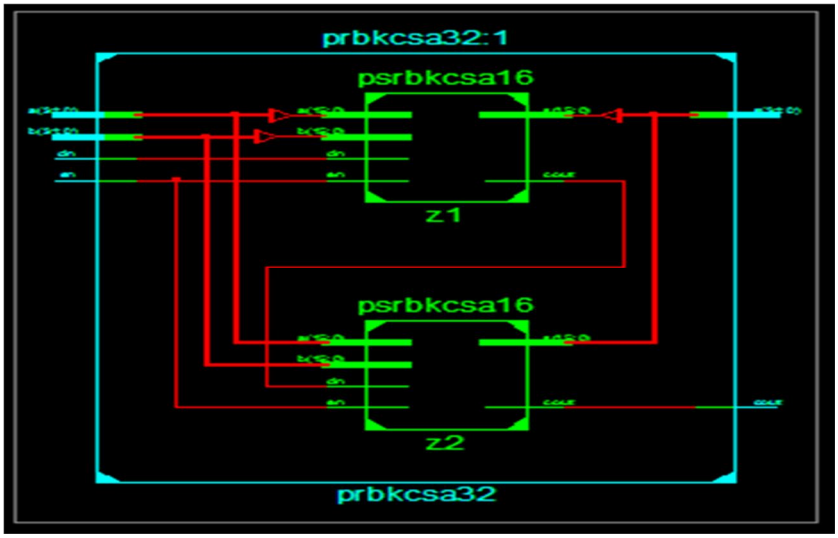

Fig: Block diagram of 32-bit Brent Kung carry select adder

Is connected to this block. The D-latch operation is done and outputs are given to the input of MUX 6:3. Multiplexer operation is done it gives an outputs carry and SUM [3:2]. Same thing the operation is done up to SUM [15:11].

Latch is an electronic device that can be used to store one bit of information. The D latch is used to capture, or 'latch' the logic level which is present on the Data line when the clock input is high. If the data on the D line changes state while the clock pulse is high, then the output, Q, follows the input, D. When the CLK input falls to logic 0, the last state of the D input is trapped and held in the latch. Fig. 12 shows the logic diagram of D-Latch

IV. RESULT AND DISCUSSION

A. Simulation waveform of Native Compiler code of proposed Result

In extension, we have designed by 32-bit carry select adder using Brent Kung adder which is the fastest and more efficient adder. The output for simulation is designed below:

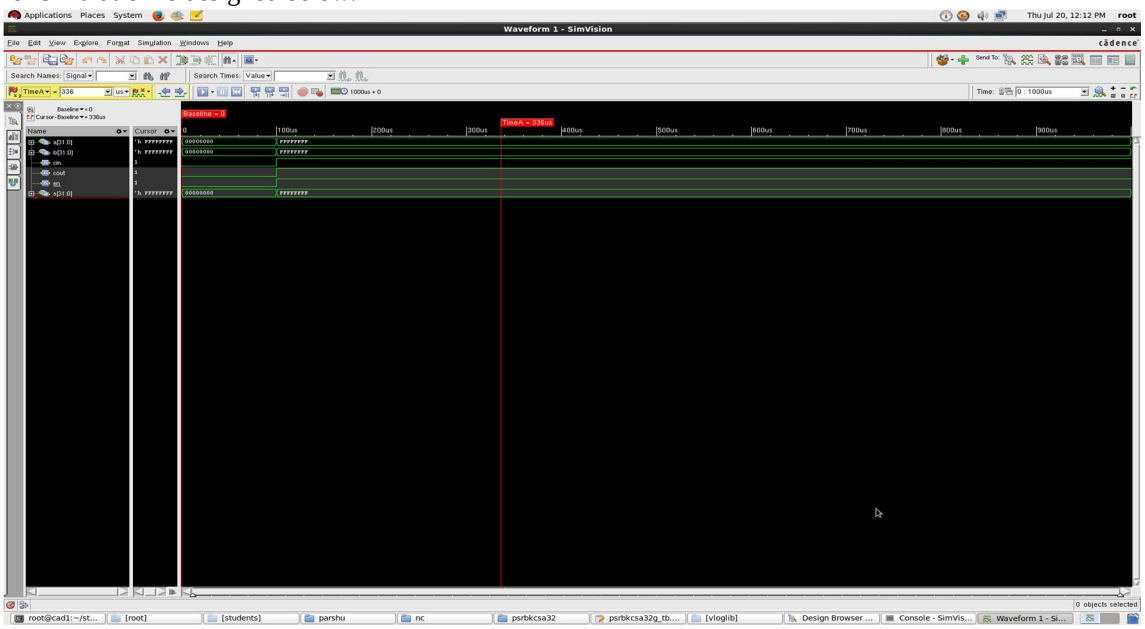

Fig: proposed Result of NC

B. Schematic Diagram of Proposed Result

After finishing the Native code simulation, we have to check the schematic. So for that we should use the RTL compiler.

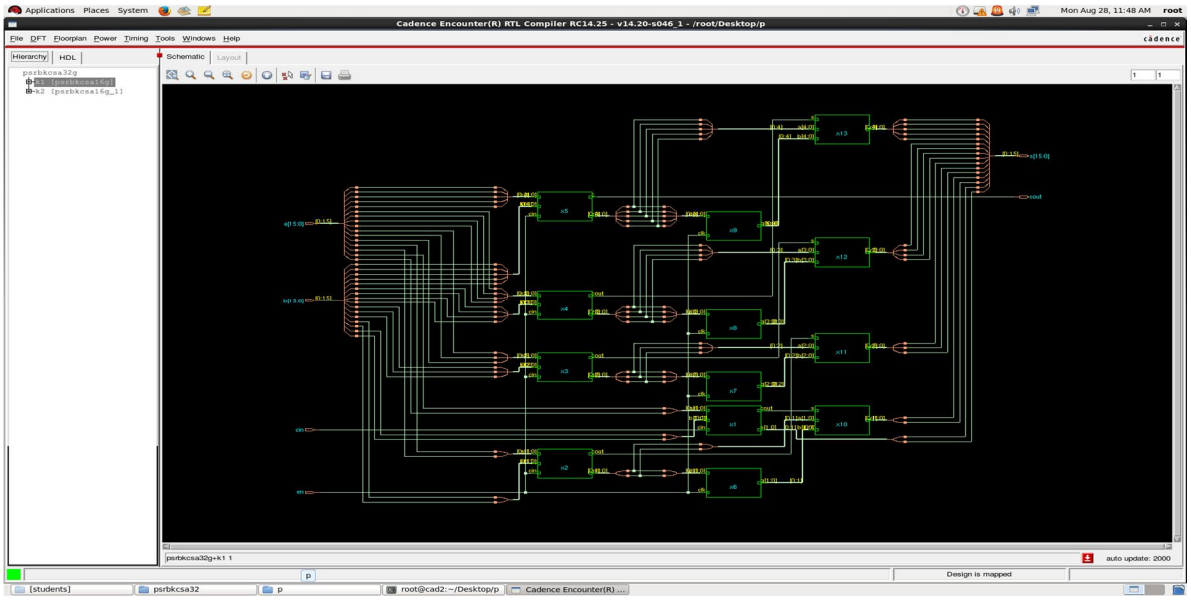

Fig: Schematic result of proposed

The above figure is proposed of 32-bit CSA RTL synthesis. It can shows the sub blocks of the RTL compiler Register-transfer-level abstraction is used in hardware description languages (HDLs) like Verilog and VHDL to create high-level representations of a circuit, from which lower-level representations and ultimately actual wiring can be derived. Design at the RTL level is typical practice in modern digital design

C. Physical Design

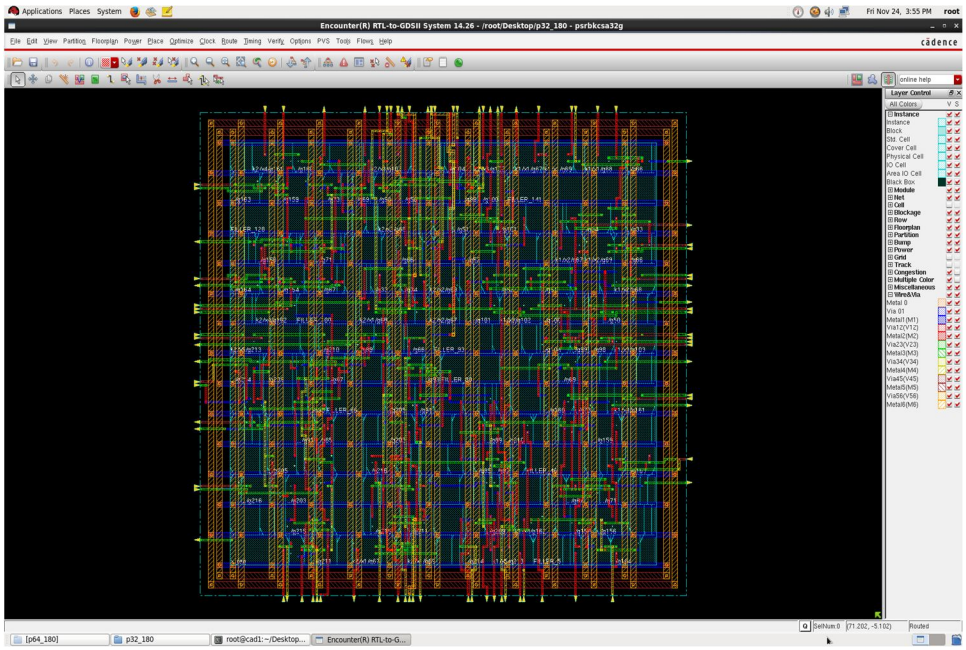

Fig.1: Physical Design for 32-bit Brent kung carry select adder

Floor plan describes about size of cell or (die). It creates the boundary and core area, for placement of standard cells. It is also a process of positioning blocks or macros on the die. . In-placement optimization re-optimizes the logic based on VR. It mainly functions for cell sizing, cell moving, cell bypassing, net splitting, gate duplication, buffer insertion, area recovery. Clock tree synthesis is a process of balancing clock skew and minimizing insertion delay in order to meet timing, power requirements and other constraints. Timing analysis for back end it requires a knowledge of all clock related constraints that is provided at front end. If there are CEL views of sub-blocks and the Flatten Hierarchical Cells option is selected, the power analysis will give down into the CEL views, even if there is a white box or gray box. Clock Gating is a power reduction technique, as clock is a highly toggling signal. It consumes more power, When a portion of design not using the clock, Clock passing to that particular portion is stopped by using clock gating technique.

TABLE I
PERFORMANCE COMPARISON AT 180nm TECHNOLOGY

S.No.	Project Paper	Existed	Proposed
1	POWER(nw)	2987015.977	1454357.173
2	DELAY(PS)	3189	93

III.CONCLUSION

This paper proposed the ASIC implementation of the carry select adder using Brent Kung adder. Power and Delay are the two constituent factors in the VLSI design that limits the performance of the circuit. This work proposes a simple technique to reduce the power and delay. In this work a Proposed Brent Kung adder using Carry Select Adder is proposed which is designed using single Brent kung adder and D-latch instead of using single Brent kung adder for Cin=O and Cin=l in order to reduce the delay and power consumption of the circuit. So these adders can be used in multipliers, in DSP to execute various algorithms like FFT, FIR and IIR with ease.

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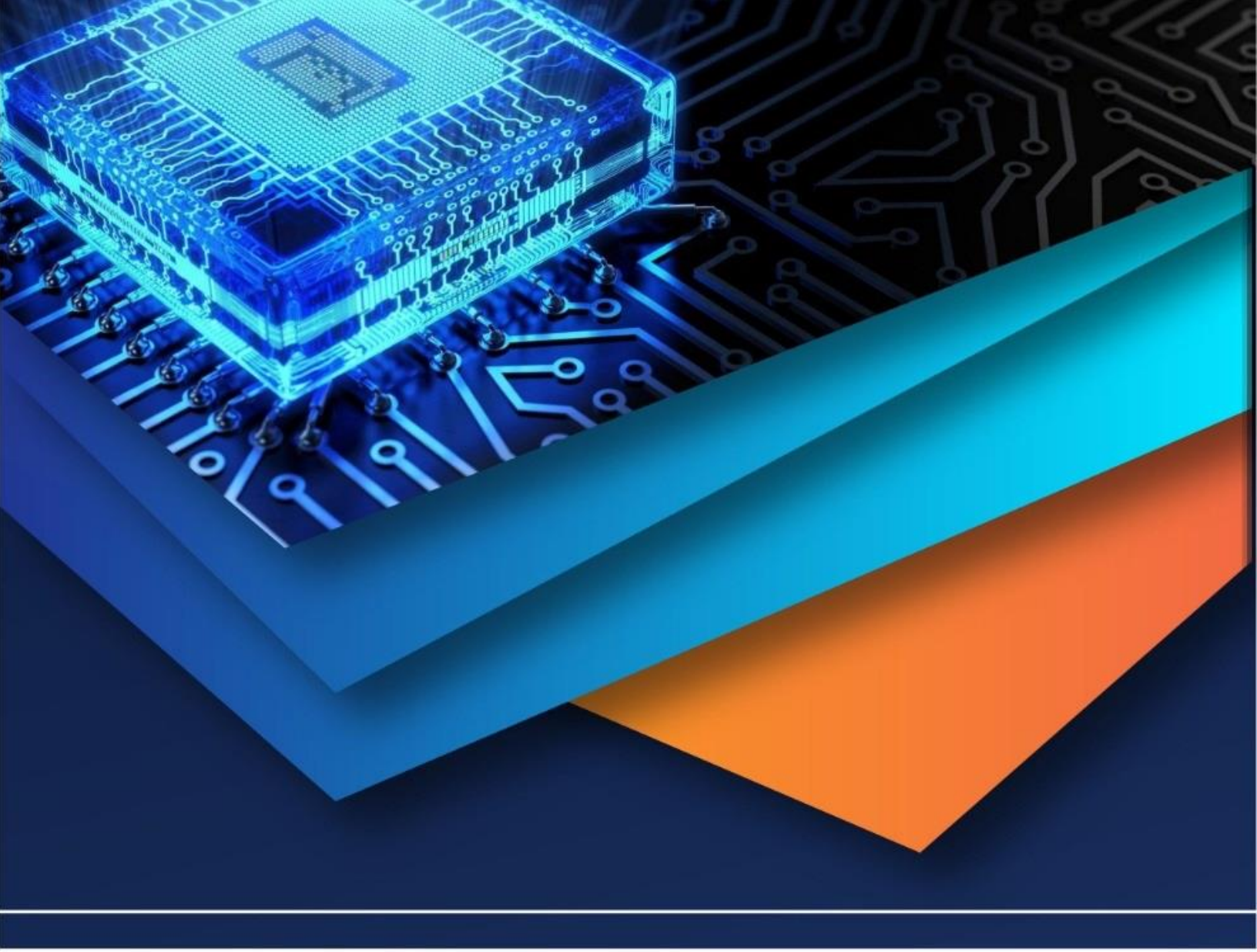

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