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Designing of Digital Front-End Structure for ECG Acquisition System

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***Abstract:** This article grants a design of digital front end structure for electrocardiogram (ECG) acquisition system utilized to diminish the energy dissipation. ECG utilizes to know the heart disorder of patient in medical field and the electrical actions generated by the heart muscles is demonstrated on ECG, then it transmits the pulsating electrical wave towards the skin. ECGs are utilized to estimate the heart speed and to check the rhythm for the heart diseases. The proposed structure of ECG is companionable with digital complementary metal oxide semiconductor (CMOS) and that can be performed with the supply voltage of 0.4V. To cancel the direct current (DC) offset on the circuit, a digital feedback loop engaged. In this design, the voltage to time converter (VTC), time mode processing and time to digital converter (TDC) are considered to convert the analog portion to digital portion. The design is implemented in 0.18µm CMOS process in cadence tool.*
***Keywords:** ECG, energy, mod-counter, De-mux, control logic, DCC circuit, Op-amp.*

I. Introduction

Now-a-days, the applications of biomedical devices have tremendous change due to the development of integrated circuits (ICs). Data acquisition is method to calculate sampling signals at substantial conditions and also changes that samples to digital values which is managed by the personal computer, the process of data acquisition systems(DAS) is used to transform the analog signals in to digital signals. Decrease the supply voltage for digital circuits is the most instantaneous and hypnotic manner to reach low power dissipation, Electrocardiogram (ECG) is a depictive recording of electrical activity of the heart over time. In this document, we are propose an better front-end structure for particularly low energy digital circuits. In this design general consist of energy, mod-counter, de-mux, control logic are used which are in digital and the analog signal is translates into digital by using time and digital mode, its also eliminates the dc-offset, interferences. The devices seek close to engineering and medicine, and its merge the circuit design for the resolving skill with a biological science to protect from the healthiness trouble. Our proposed system reaches a energy reduction of nW at MHz and utilize clock frequency.

II. Literature Review

At the point when the heart does not work appropriately, a artificial cardiac device is expected to perfect the heart's contraction. Be much functionality at maximum power spending plan requires less power per work. In this approach, the power utilization of the front-end, (sense speaker), of the pacemaker must be decreased. The outline of a ultra-low-control sensor interface is an extremely difficult duty because of the way that the intracerdiac electro-gram, ECG, is an exceptionally powerless signal (1-5mV) at low frequencies (50mHz-100Hz). A lot of research has been devoted to looking for approaches to understand the previously mentioned challenges. A MOS bipolar pseudo-resistor used to channel such low frequencies was reported. These outlines required a high supply voltage and demolish generally huge power, yet result in moderately high Noise Efficiency Factor (NEF). A 1V 2.3 µW biomedical signal securing, where an samples and hold circuit has been implanted into the output phase of the OTA to decrease the power. Be that as it may, a high ADC clock rate is required to limit the mistake caused by the switching of the output phase. The integrated circuit perform variety of function that supports by implanted medical devices, such as sensing and a communication between electronic equipment and human being. To diminish the power utilization much further, in the present paper, another design for a sensor interface circuit for pacemakers joins ultra-low-control task with low noise by operate a non-direct current-mode ADC.

An instrumentation (or instrumentation) amplifier is a kind of differential amplifier that have be furnished with input support speakers, which remove with the requirement for input impedance coordinating and in this approach make the amplifier especially appropriate for use in estimation and test. Extra attributes incorporate low DC balance, low drift, low disturbances, high open-loop increase, high basic mode dismissal proportion, and high info impedances. Instrumentation amplifier are utilized where awesome

precision and security of the circuit both tiny and extended haul are required. These circuits find across the board use in almost every therapeutic gadget, both for the preferences already specified and for the way that instrumentation amplifiers are additionally accuracy pick up gadgets. Instrumentation amps don't require outer feedback resistors, rather it has trimmed laser resistors which is embedded on Integrate circuit Itself, utilizing just a solitary external gain up setting resistor to design the amplification factor, disposing of resistor bungles. This enables the gadget to have its increase set to a correct number, in view of the necessities of the circuit. Most biomedical sensors are high impedance and produce small signal, for example, pulse sensors, ultrasound transducers, enraptured and non-spellbound terminals, and radiation thermometry transducers. Application cases transducers, mechanical process control, direct position detecting, and bio-potential securing frameworks. Principle centre is around the plan of incorporated instrumentation for medicinal impedance imaging utilizing bio-impedance estimations. Bio-impedance imaging is otherwise called electrical impedance tomography which is far superior than the other imaging systems. It has advantage over different techniques for example, noise free, radiation less, profoundly convenient, and economical. In a bio-impedance imaging framework a differential altering current is connected through a couple of surface electrode to the body tissue and coming about voltages are grabbed by another terminal which is additionally amplified and handled. Amplifier has its need of high input impedance to stay away from the piece of delivered current into the circuit, which would cause mistaken deficiencies. Subsequently IA is required. The primary spotlight is on to identify the microvolt (µvolts) differential signal of the body tissue within the sight of mill volts (mv) mode signal at working frequency of few Hz to MHz.

III. EXISTING SYSTEM

Biomedical signal securing frameworks [3] more often than not subsist of a low-noise amplifier (LNA), a band-pass filter, a sample and hold, and a analog to digital converter (ADC) is appeared in Fig.2.Typically, analogy portion takes more amount of power and region contrasted with the digital structure. This digital improved approach can expands the extensibility of the framework in removing the undesirable interferences.

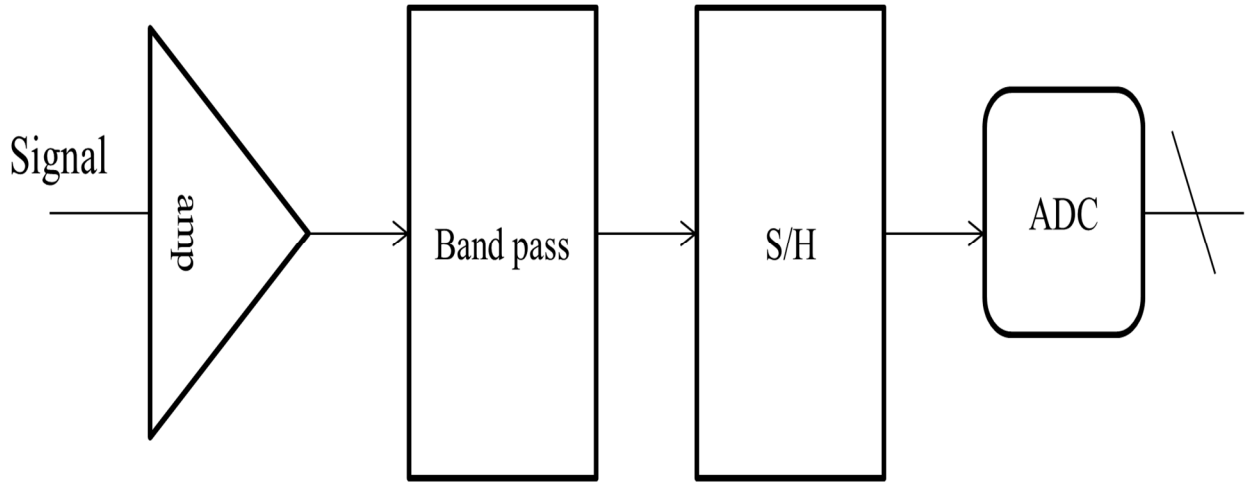

Fig.1 Biomedical signal acquisition system.

IV. PROPOSED SYSTEM

A modern power-capable ECG system that uses a complete digital structure is proposed. In the framework, DCC, Demux, active electrode, mod-counter, op-amplifier and control logic is implemented in the 0.18µ CMOS technology to calculate its performance. The supply voltage is 0.4 V, and the circuits are planned to run in the sub- threshold region to reduce the power dissipation. The following part of system is challenges and it is discuss in below part.

A. Proposed System Block Diagram:

The analog signal Vsin is given as input to active electrode it reaches to switching circuit. Form VTC, voltage is converted to time by VTCp and VTCn then its feed back to control logic, which transformed into digital part and acts as input to front-end, which eliminates interference and offset in circuit, Acontrol logic to connect with feedback and 2x1multiplexer is design to connect the mod-counter and it operates by external clock, reaches to de-mux which consist of 5 inputs and (0-31) outputs, finally goes to DCCp and DCCn which generates the current to input .Now a digital signal is established at the output of tdp and tdn.

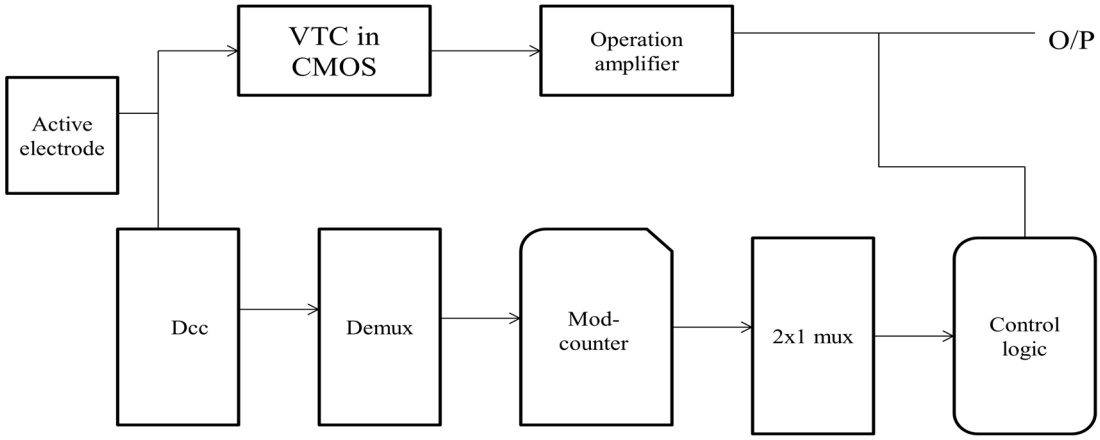

Fig.2Proposed system block diagram

B. Active Electrode

Active electrode are becoming more popular. The electrodes which translates high impedance source to low impedance source of output and its also save the time for researcher. Whereas tiny electrode were set on specified point to produces the output on ECG. By using electrodes their will be no skin problem and it is low costs, safer. In this design electrodes are used in CMOS innovation.

C. Digital to Current Converter

The complete digital structure has ´2´Direct current control portion are utilized. In this portion the charge are produces a current depends on 0-31 bits at the output of Demux ,The DCC design in which produces the gate voltage is necessary for generation of reference current in top circuit. The current generate by transistor from Mp0 to Mp31 and Mn0-Mn31 exceeds through a transistor of Mp and Mn to produces ´2´ voltage input of PMOS and input NMOS. Then the voltage are applied to PMOS and NMOS of voltage time converter and NMOS of the voltage to time converter portion. The produces a current that is proportional its digital input and reduces(or) raises. Thee voltage are connected to the PMOS of voltage to time converter and NMOS voltage to time converter portion and expands the input voltage of PMOS in VTC and NMOS of VTC and every LSB of DCC corresponding to much or less than 3mv and this voltage is added(or) subtracted of every step in a system.

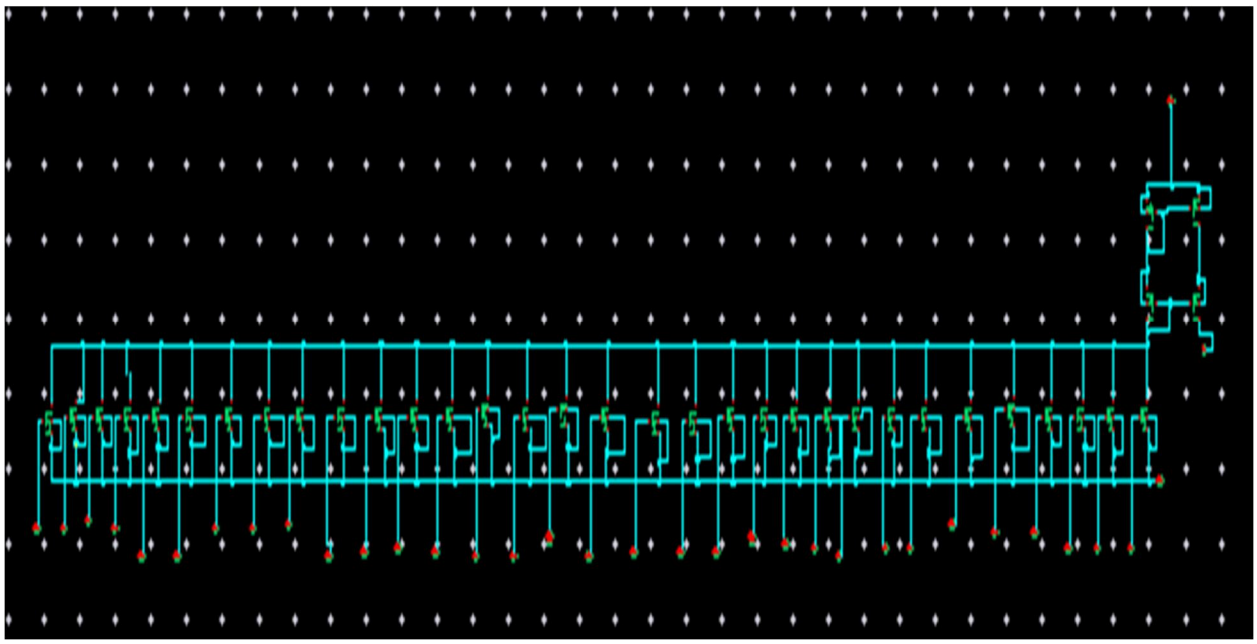

Fig.3 Diagram of the current DCCp.

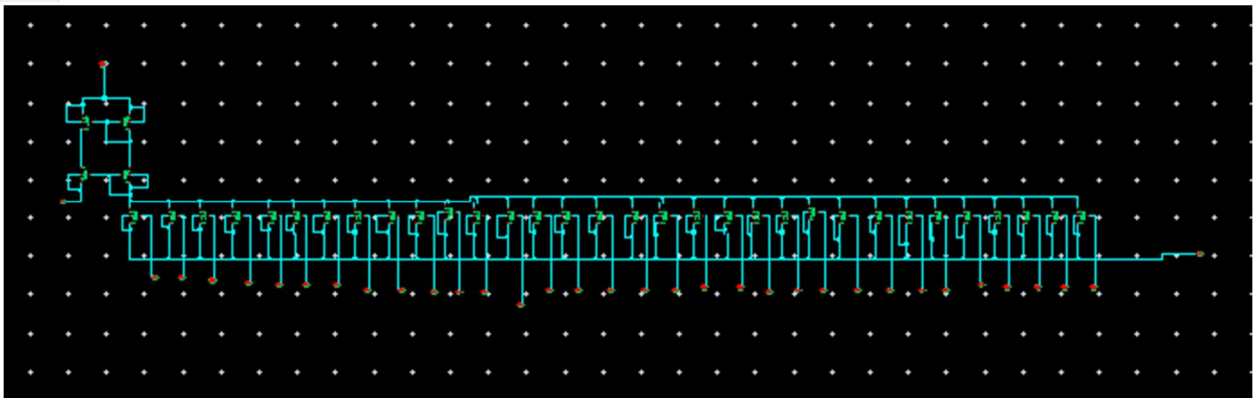

Fig.4 Diagram of the current DCCn.

To recognize the behavior of the DCC, assume that the offset at the input increases (decreases) dominated to a rise (fall) in *V*inp and *V*inn. As a outcome, the delay of the VTC*p* block enlarge (or)reduce and that the VTC*n* diminish (or)raise. As can be seen, at the beginning, the offset cancellation circuit is in term and setting the output of the DC signal is reliable.

D. Demux(0-31)

The demux have 5inputs and 32 outputs. The ability of a de-multiplexer is to opposite to the capacity of the multiplexer and the alternate way types of the multiplexer. A few multiplexers perform both multiplexing and de-multiplexing tasks. In the vast scale-advanced frameworks, a solitary line is required to bear on at least two computerized signals – and, obviously! At once, one flag can be set on the one line. However, what is required is a gadget that will enable us to choose; and, the flag we wish to put on a typical line, such a circuit is alluded to as multiplexer A demultiplexer (or demux) is a gadget that takes a solitary info line and courses it to one of a few advanced output lines. A demultiplexer has a only input and much data output lines n select lines, and it is data distributor.. A multiplexer is additionally called an information selector. Then again, a demux is a gadget taking a solitary info signal and choosing one of numerous information output lines, which is associated with the single information. A multiplexer is regularly utilized with a corresponding demultiplexer on the less than desirable end. *M*ultiplexers.

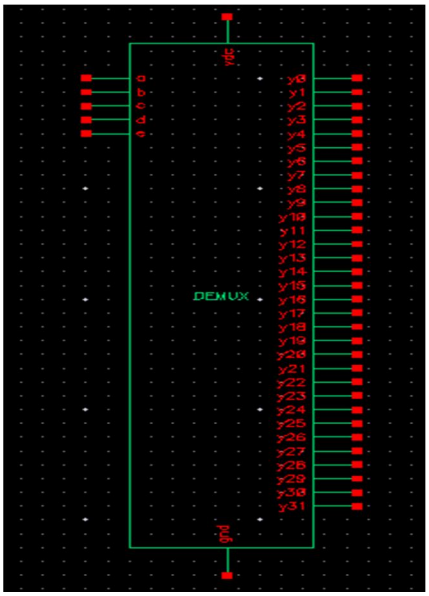

Fig.5 Diagram of Demux

E. JK flip-flop

Generally 1-bit digital portion of memory circuit is also know as a flip-flop and which is design by logic gates and it store the information in state. A flip flop is an bi-directional multivibrator.The design has to change the state by signal applied to control inputs by single (or)additional and also store element in sequential logic and also JK flip flop is manly used in the digital part of system.

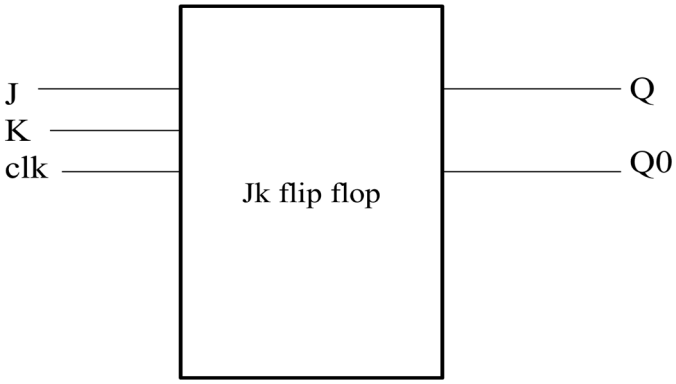

Fig.6 Diagram of JK flip-flop

In JK latch, which is in off condition that will be a no memory, when a logic1 is applied to “SET” then Q output goes high and Q0 goes low. Accordingly the feedback process, The output of Q will remain logic “1” when the input goes logic “0” . This is how the latch creates as a memory device. Whereas logic“1” is applied to Reset line and drives and become low and respectively Q0 will be high, when two inputs are logic“0” the latch remains in it previously Reset(or)set condition. When two inputs are in logic“1” at once there is a problem in it and simultaneously produces a high Q state and low Q state in SR-latch. This generates a race state inside the circuit. Where as a JK flip-flop “2” inputs are in logic“1” there is no problem in this state. So it obtain a toggled process.

F. Mod-Counter

The activity of a counter is to count by propelling the substance of the counter by one count with each clock heartbeat. Counters which propel their sequence of numbers or states when actuated by a clock input are said to work in a "count up" mode. In like manner, counters which diminish their arrangement of numbers or states when actuated by a clock input are said to work in a "count down" mode. Counters that work in both the UP and DOWN modes, are called bidirectional. Counters are sequential logic gadgets that are enacted or activated by an outside planning heartbeat or clock flag. A *counter* can be developed to work with clock and without clock. With synchronous counters, every one of the information bits change synchronously with the utilization of a clock signal.

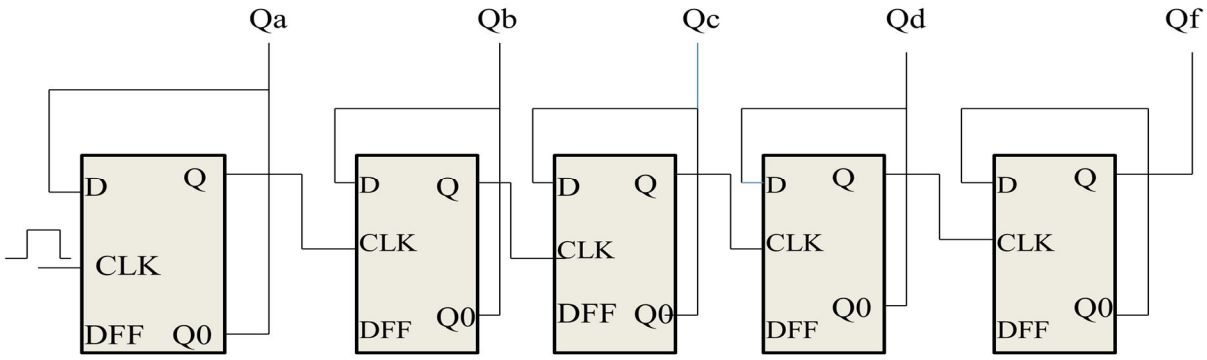

Fig.7 Diagram of counter

G. Simulation results

Though a synchronous counter circuit is autonomous of the input clock so the information bits change state at various circumstances in a one after other. The inputs are active electrodes which are in CMOS innovation and it will supply the voltage to VTC and a current comes from the 2 DCC circuits, which is feedback manner to the switching circuit and external clock is available which comes from the mod-counter and it’s also set the values that is low. And Direct current control circuit which will reduces the dc offset in circuit and sin wave given as input it consist of DC voltage and AC magnitude and amplitude are given in the input, used to reduces the power and have a little depends on temperature coefficients. These two stage common gate terminal is taken as input which is fed to the DCCs architecture and whose output is set to the Mod-counter. The proposed is executed in 0.18µm CMOS technology at 0.4v supply voltage. The simulated power dissipation is 11nw.

Fig.8 Output waveform of block diagram with dc offset cancellation

V. CONCLUSIONS

In the expectation of the upcoming dominance of digital CMOS innovation, a complete digital structure for an ECG acquisition method was designed. In this system, active electrode, Demuxs, Op-amplifier, DCC and mod-counter circuits were implemented. The system has low power dissipation, and less complexity. This digital structure is simulated in 0.18µm in CMOS innovation at 0.4 V supply voltage. The power dissipation has been simulated in this structure is 11nw.In upcoming, digital structure can be change to agree an offset voltage bigger than ±300 mV. In arrange to do this, the resolution of the DCC circuit and de-multiplexer should be enlarge to 64 bits.

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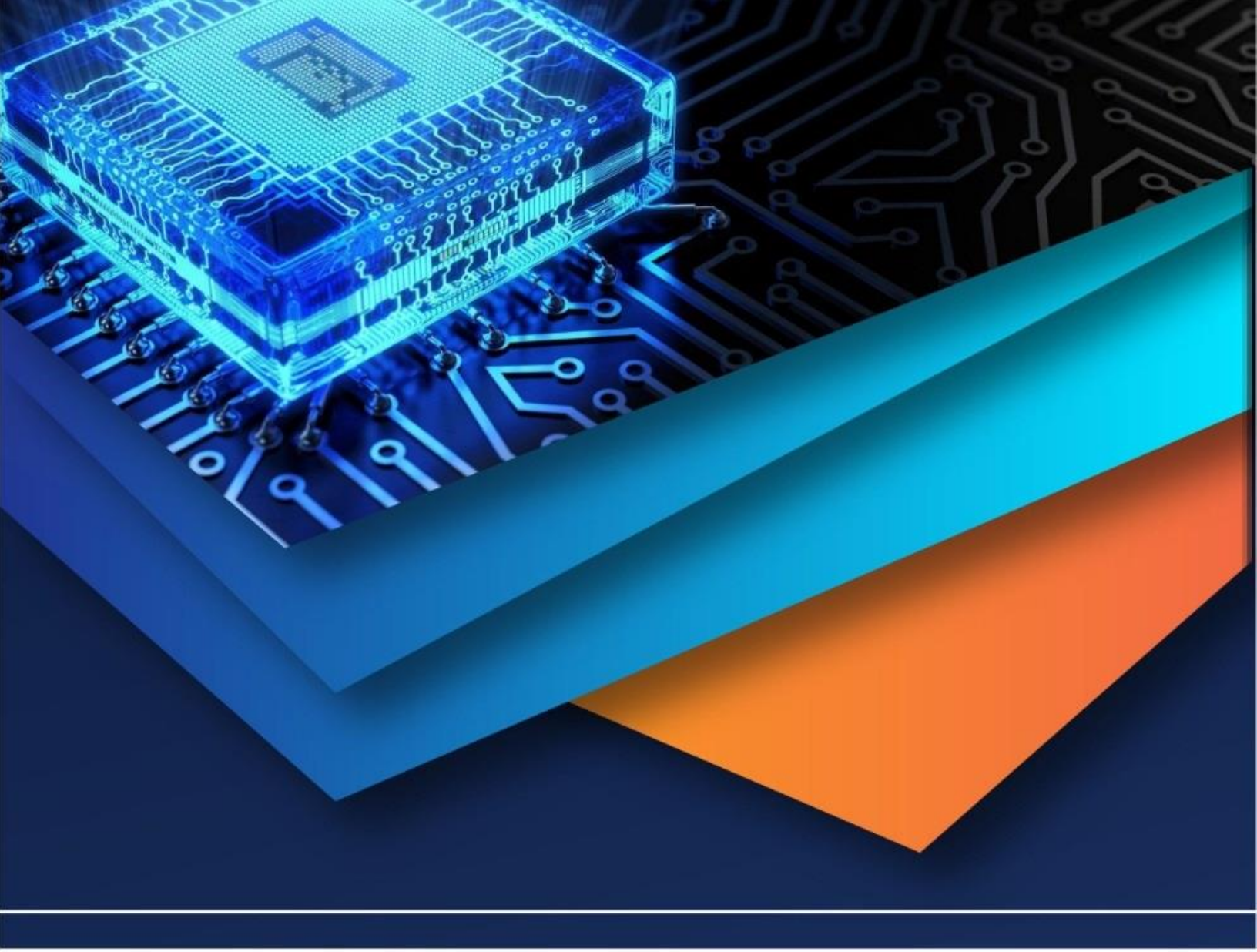

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