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# Enhanced Adiabatic Paradigm for Ultra Low Power and High Speed Switching

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***Abstract:*** ***With the continuous rising expedition for miniaturization of VLSI technology, one of the key hubs of the research has been shifted in the direction of ultra low power paradigms. Over past few years, adiabatic paradigms have been premeditated and found to be effectual in realising LPVD's. This paper succinct some of the adiabatic logic families such as ECRL, PFAL and exploits an enhanced adiabatic logic know as Enhanced Diode Connected DC Biased Positive Feedback Adiabatic Logic (EDCDB-PFAL). A few useful constructs, such as Boolean logic gates and binary full adder are successfully modelled and verified by using proposed technique. The flexibility and simplicity of modelling, simulation and verification show the usefulness and applicability of EDCDB-PFAL for low power paradigms. This paper aims at evaluating the efficacy of proposed adiabatic logic circuit, in terms of power, delay and leakage current over conventional logic families and are examined using Tanner EDA Tool with 250nm technology.***

***Keywords: Low power, Adiabatic switching, ECRL, PFAL, EDCDB-PFAL.***

## I. INTRODUCTION

Due to the advancements in VLSI technology over the years, transistors size has reached to minuscule size that concerns the designers with the increasing power dissipation [1]. The most significant types of power dissipation are Static and Dynamic power dissipation. The static power dissipation is due to internal leakages in a device during off state, whilst dynamic power dissipation is due to energy loss during charging and discharging of the output node capacitance of a transistor when keying takes place. To achieve low power various paradigms has been implemented over conventional logic such as sub threshold logic, multi threshold logic and adiabatic logic [2,3]. Adiabatic logic has been widely used as a low - power tool. The word adiabatic comes from thermodynamics that depicts a method where no energy acquaintances with the milieu and hence no dissipation of energy loss takes place. In the recent years, several adiabatic or energy recovery logic (ERL) paradigms have been exploited and have attained significant power savings compared to conventional circuits [1,3-5]. Due to keying of circuits with output voltage swing causes energy transfer from power supply to the output node and to the ground causing more energy transfer in CMOS conventional techniques. Thus to increase the energy efficiency of the circuits and to achieve low power, adiabatic logic families are used that offers reduced power dissipation, recycling the energy drawn from the supply($V_{DD}$), fast switching speed and less noise. In adiabatic paradigms, the charge flows back to the $V_{DD}$ rather than flowing from the output node capacitance of a transistor to the ground making it to reuse achieving low power [4,5]. This paper delineates as follows: section 2 presents the overview of convention logic and explicates briefly about the adiabatic design methodology. Section 3 elucidates briefly about the proposed Enhanced Diode Connected DC Biased Positive Feedback Adiabatic Logic (EDCDB-PFAL) to attain better performance of the circuit and also the implementation of EDCDB-PFAL full adder is shown. Whilst in section 4, the simulated results of a full adder is evaluated with respect to traditional CMOS logic, ECRL and PFAL designs in terms of power consumption, leakage current and propagation delay and finally concludes in section5.

## II. LITERATURE SURVEY

### A. *Conventional switching*

The major sources of power dissipation in conventional CMOS circuits is due to the switching activity of MOSFETs as the gate voltage alters from high to low inducing spike/glitch. The power consumption becomes a decisive issue when the circuit is in active and power-down modes respectively. The total power consumption of a CMOS circuit is given by[3]

$$P_{total} = P_{dynamic} + P_{static}$$

In CMOS paradigms, switching power dissipation, shown in fig.1 occurs due to charge-up and charge-down/discharging of charge in the node capacitance (CL) i.e. when energy is haggard from the power supply (VDD), the output node potential of a CMOS logic circuit charges up and makes a logic transition. During charge-up phase, the output node voltage characteristically makes a full transition from 0 to VDD and dissipates half of the energy drawn from the VDD as heat in the conducting pull-up network whilst in

conducting pull-down network the output node voltage drops to 0 from VDD and no heat is dissipated during power down mode.So the total power consumed during switching of the output node is given by

$Ps/w = 0.5(\alpha C_L V_{DD}^2 f_{clk})$

Where $CL(i) = \sum_j C_{in}j + C_{wire} + C_{par(i)}$

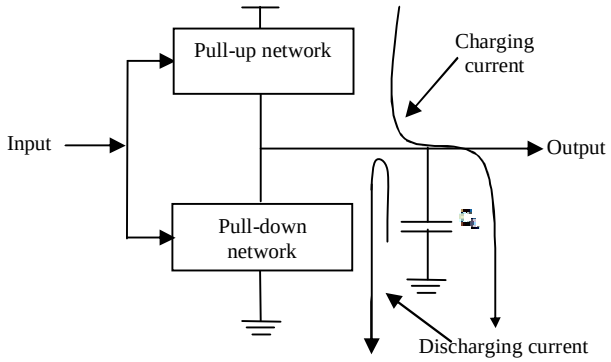


Fig. 1 Switching power dissipation

*B. Adiabatic Switching*

The principle behind adiabatic keying [5,6] is that, the switching should be adequately slow so that no heat is emanated significantly. This dawdling switching is attained when a DC power source is replaced with an AC power clock (pck) that can be attained by an oscillator, a resonance LC driver, a clock generator etc[7]. since the charging current source corresponds to a linear voltage ramp then it delivers the charge Q = CVdd during time period T and the channel resistance R is given by-

P= I2RT = (RC/T)VDD2 From the above equation, as T increases linearly, power dissipation decreases linearly. Similarly if T is made adequately larger than RC, the dissipation will be nearly zero achieving low power adiabatic switching. Thus the designing of adiabatic paradigms is mounting, and proves to be the best in analysis with conventional designs[8].

Adiabatic switching consists of four phases (i.e Wait, Evaluate, Hold and Recovery), with a phase difference of one quarter of a complete period shown in fig. 2.


Fig. 2 Four Phased Power Clock (pck)

In the WAIT phase the pck stays at '0' value, maintaining the output at low state, the evaluation logic generates pre-evaluated results. Since the pck is at low state, the pre-evaluated inputs will not affect the state of the gate[8]. In the EVALUATE phase the supply switches up from '0' to VDD gradually, and the outputs will be evaluated based on the results of pre-evaluation logic. In the HOLD phase, pck will be at high level providing a constant input for the next stage in pipelining of adiabatic paradigms and maintains a valid output for the entire phase. In the RECOVERY phase, power supply switches down to '0' state and the energy of the circuit is recovered and transferred back to power source instead of dissipating energy[7-10].

*1) Efficient Charge Recovery Logic (ECRL)*

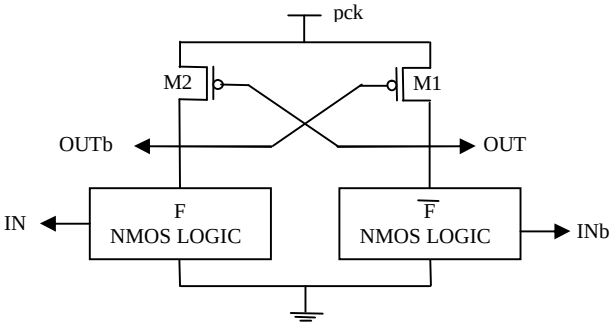


Fig. 3 Efficient Charge Recovery Logic (ECRL)

The Efficient Charge Recovery Logic (ECRL) circuit (shown in Fig. 3) exploits two PMOS transistors in cross-coupled fashion and two NMOS transistors in the functional blocks. An AC power clock (pck) is used instead of a constant DC supply[8]. Consider IN at high level and INb at low level. During the beginning of a cycle, when pck rises from 0 to VDD , OUT remains at 0 level because the high level at IN turns the F - NMOS block high. OUTb follows pck through M1. Now when pck reaches to VDD, the outputs hold valid state. During the hold phase these outputs remain stable and can be used as inputs for the next stages of evaluation[9]. In the next phase of recovery, power clock switches down to 0 level and the power from the output nodes can be returned back to power clock so as to recover the delivered power. The downsides of ECRL logic is the due to coupling effects, since the two outputs are driven by the PMOS latch that may interfere with each other at the output[11,12].

*2) Positive Feedback Adiabatic Logic (PFAL)*

The Positive Feedback Adiabatic Logic (PFAL) shown in fig. 4, achieves low power compared to other logics. It consists of two PMOS transistors and two NMOS transistors in cross coupled fashion[11-14]. The NMOS logic functional blocks are connected in parallel with the PMOS pull up transistors, forming a transmission gates. The fact that the functional blocks are in parallel with the pull up transistors the equivalent resistance is smaller during the charging process of capacitance[1,8,10].

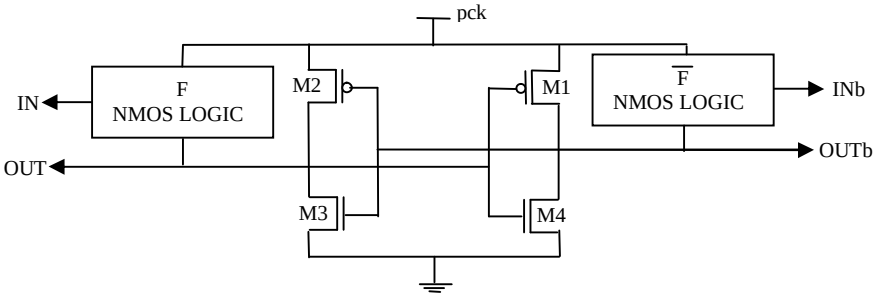


Fig. 4 Positive Feedback Adiabatic Logic (PFAL)

## III. PROPOSED ENHANCED DIODE CONNECTED DC BIASED POSITIVE FEEDBACK

*A. Enhanced Diode Connected DC Biased Positive Feedback*

The proposed EDCDB-PFAL circuit is shown in fig. 5. The design is similar to the PFAL logic design with the latch consists of two PMOS transistors, two NMOS transistors, two NMOS logic functional blocks connected in parallel with the latch forming a transmission gates. From fig 5 M5 transistor acts as a diode and a DC voltage source is connected in between the pull-down MOS transistors and the ground. The NMOS diode acts as an active load which provides high impedance path to the pck in order to control the discharging rate at the output nodes. The DC source incorporates the advantage of level-shifting technique to reduce leakage currents, provides faster switching and to achieve low power[11,13].

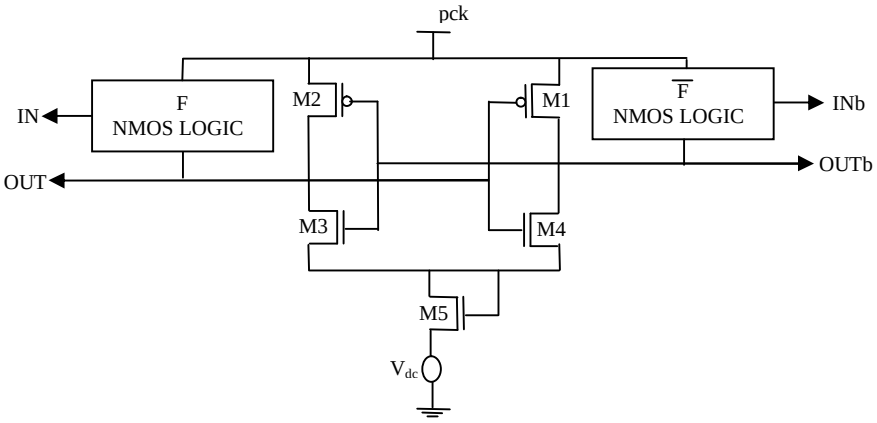


Fig. 5 Diode Connected DC Biased Positive Feedback

## IV. IMPLEMENTATION OF EDCDB-PFAL FULL ADDER

In this paper, we present a gate level implementation of MUX based full adder shown in fig. 6 using EDCDB-PFAL approach. The sum of the inputs 'A' and 'B' is written to output Sum, S and generates a carry, C. To evaluate a valid sum and carry the EDCDB-PFAL full adder exploits four switching phases. To implement full adder 2:1 MUXs are used as it generate one of the several input data and forwards to the output. Due to this required data is attained at the output reducing the unwanted switching activity in the circuit.

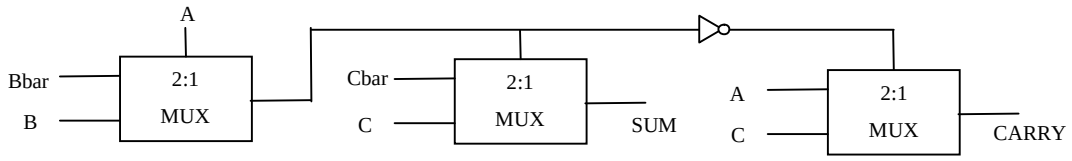


Fig. 6 EDCDB-PFAL implementation of MUX based Full Adder

## V. EXPERIMENTAL RESULTS AND DISCUSSIONS

In this work, EDCDB-PFAL mux based full adder is designed and simulated to evaluate the average power, leakage current and propagation delay. The proposed EDCDB-PFAL adder is evaluated with traditional CMOS, ECRL and PFAL designs. To scrutinize the performance of proposed EDCDB-PFAL paradigms to other conventional designs, we have carried out simulation on Tanner EDA with 250nm technology. The evaluated results are tabulate and the waveforms are collected.

### *A. Simulation results for proposed EDCDB-PFAL 2:1MUX*

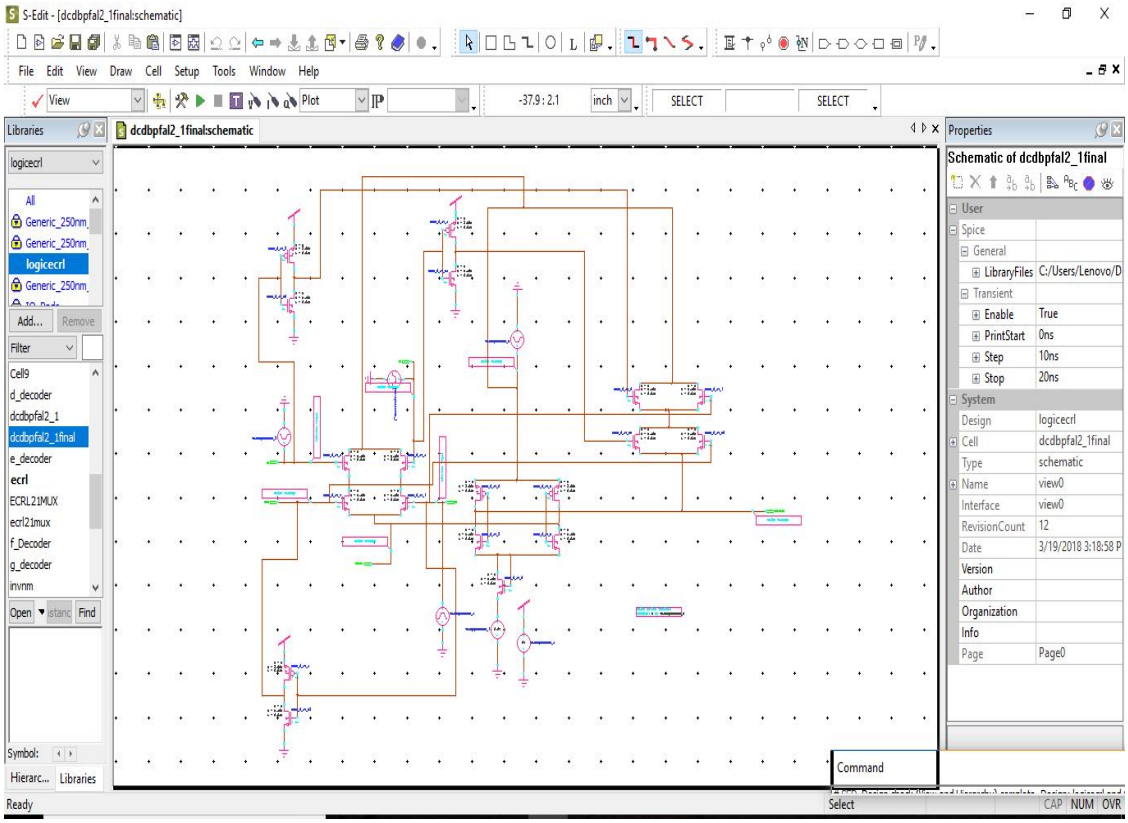


Fig. 7 Gate level implementation of 2:1 MUX

This paper proposes the design and analysis of 2:1MUX using EDCDB-PFAL paradigm, shown in fig. 7 and the simulation result of 2:1MUX is shown in fig. 8.

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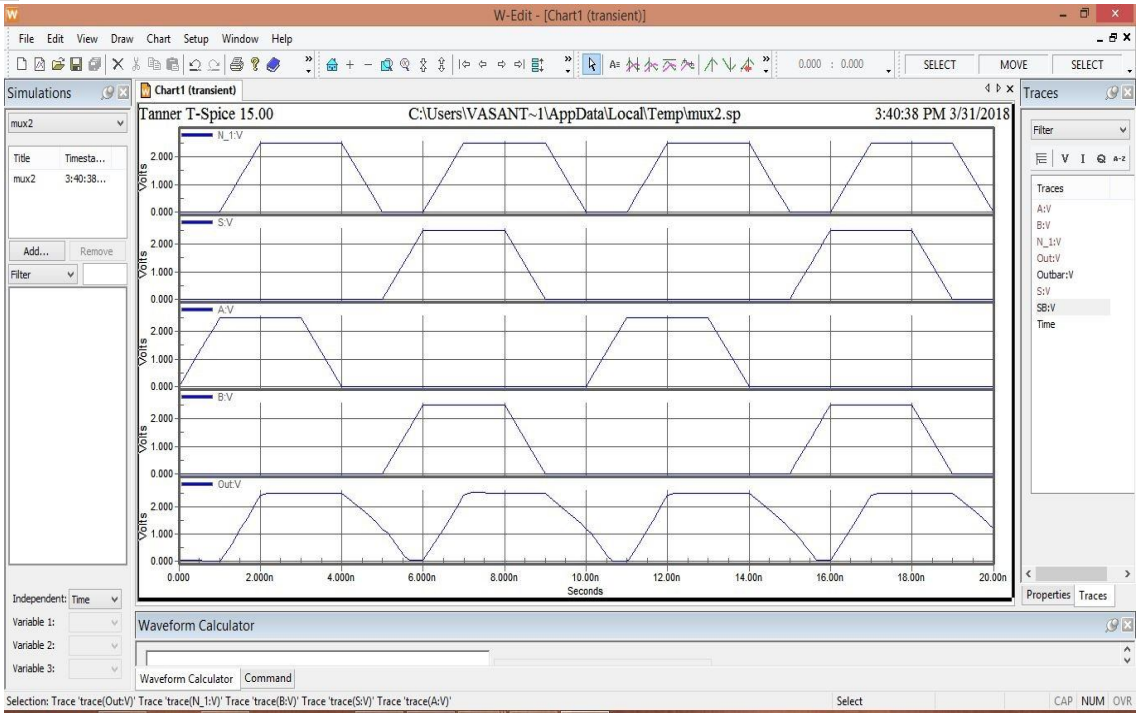


Fig. 8 Output Waveforms for 2:1 MUX

## VI. SIMULATION RESULTS FOR PROPOSED EDCDB-PFAL FULL ADDER

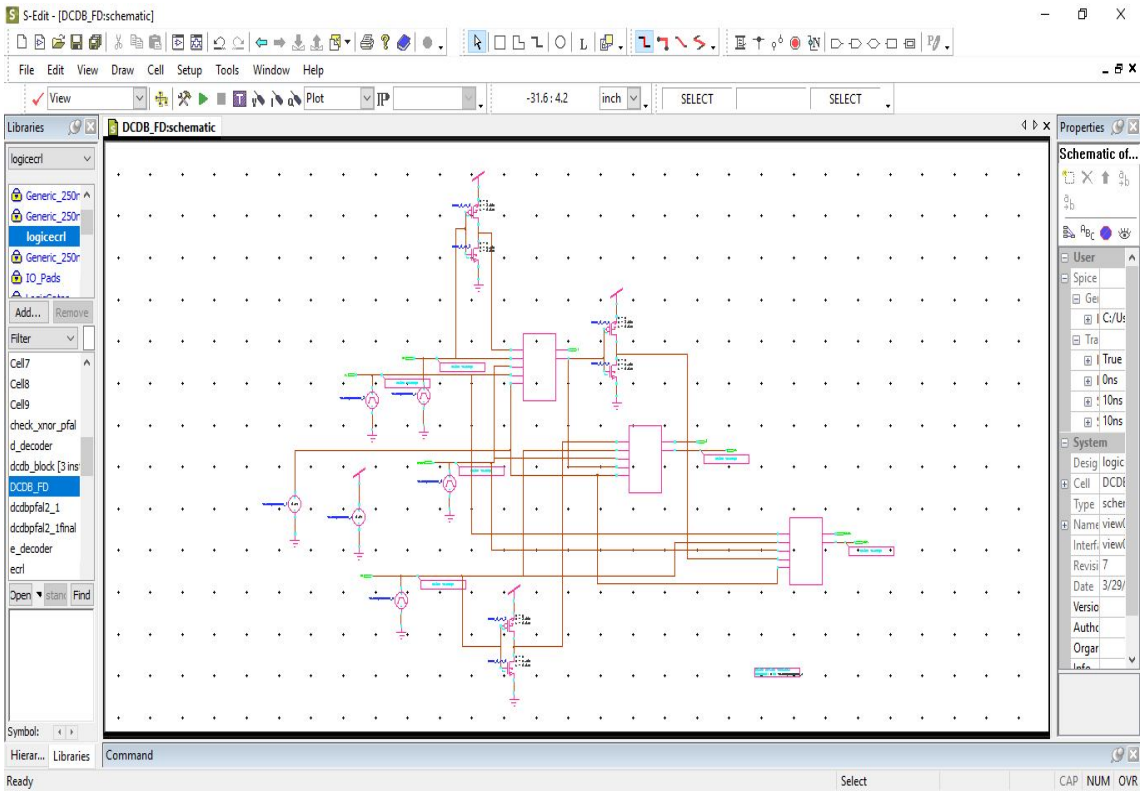


Fig.9 Gate level implementation of Full Adder

The simulation for proposed enhanced DCDB-PFAL full adder has been performed using Tanner tool. Fig. 9 shows the Full Adder compilation with zero errors and zero warnings while fig. 10 shows output waveform of Full adder which verifies the truth table.

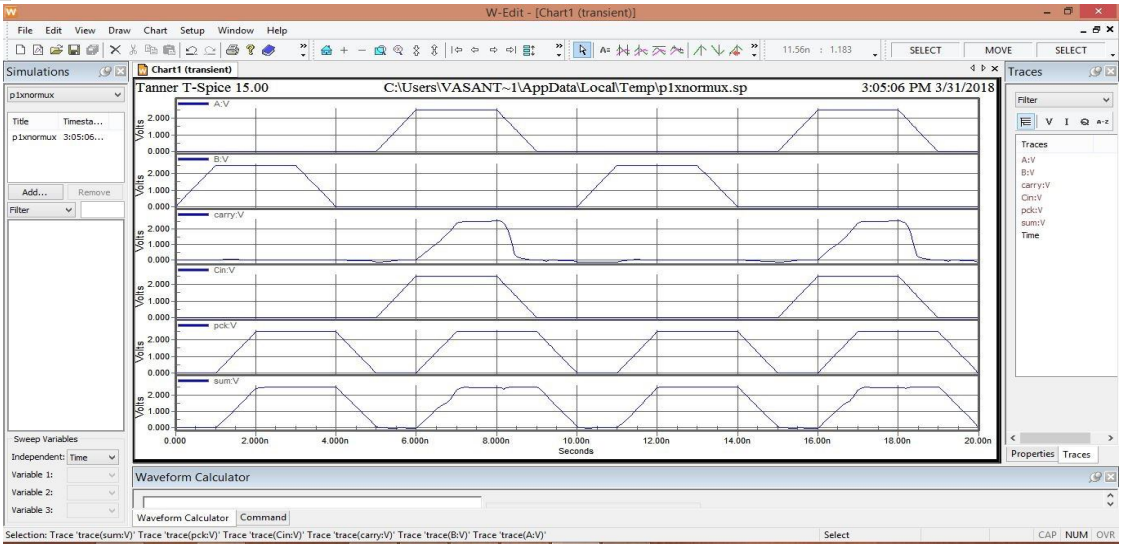


Fig. 10 Output Waveforms for Full Adder

*A. Evaluated Results*

Power, leakage current and delay are the key parameters of any experimental design. Table 1 shows the average power, leakage current and delay for CMOS, ECRL, PFAL and EDCDB-PFAL paradigms. The tabulate results show that the paradigms based on EDCDB-PFAL principle confers higher performance when compared to conventional approaches proving the proposed enhanced logic is an attractive solution for low power and ultra low power requirements.

TABLE I
EVALUATED RESULTS

| Logic Family | Average Power(nW) | Delay(ns) | Leakage Current(µA) |
|---|---|---|---|
| CMOS | 110.27 | 12.03 | 159.30 |
| ECRL | 833 | 8.9 | 113.12 |
| PFAL | 713.3 | 8 | 55.10 |
| EDCDB-PFAL | 512 | 4.07 | 115.34 |

*B. Graphical Analysis*

Graphical represetation of all the logic families are compared and showed in fig.11. Among all the log families the propsed EDCDB-PFAL adiabatic design offers low power an fast switching speed.

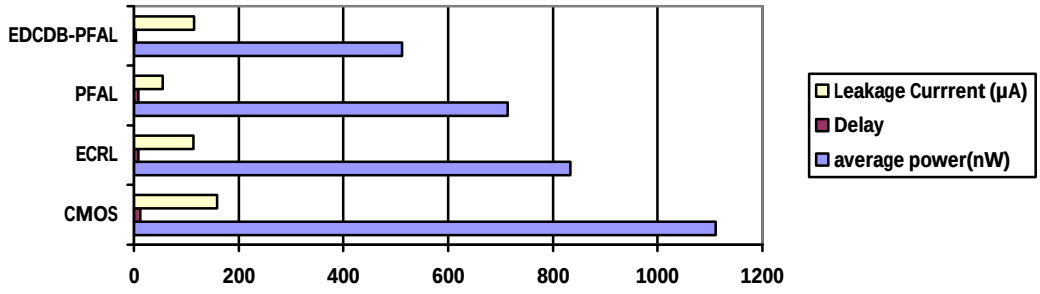


Fig. 11 Graphical analysis for EDCDB-PFAL Full Adder

## IV. CONCLUSION AND FUTURE SCOPE

To reduce the downsides in traditional architectures, we incorporate adiabatic logic for ultra-low power operations known as EDCDB-PFAL. Potential benefits of the proposed technique include reduced leakage currents, power, delay and less susceptible to

parameter variations. Upon comparison, it was found that the proposed adiabatic technique vastly outperforms traditional logic families in all aspects and drastically outperforms in terms of power and can operate faster. Whilst this work presents root to existing predicament and has opened the door for new research projects. For future work, we will further scrutinize the performance of the circuit to achieve ultra low-power design and to overcome sub-threshold leakage overheads compared to conventional designs.

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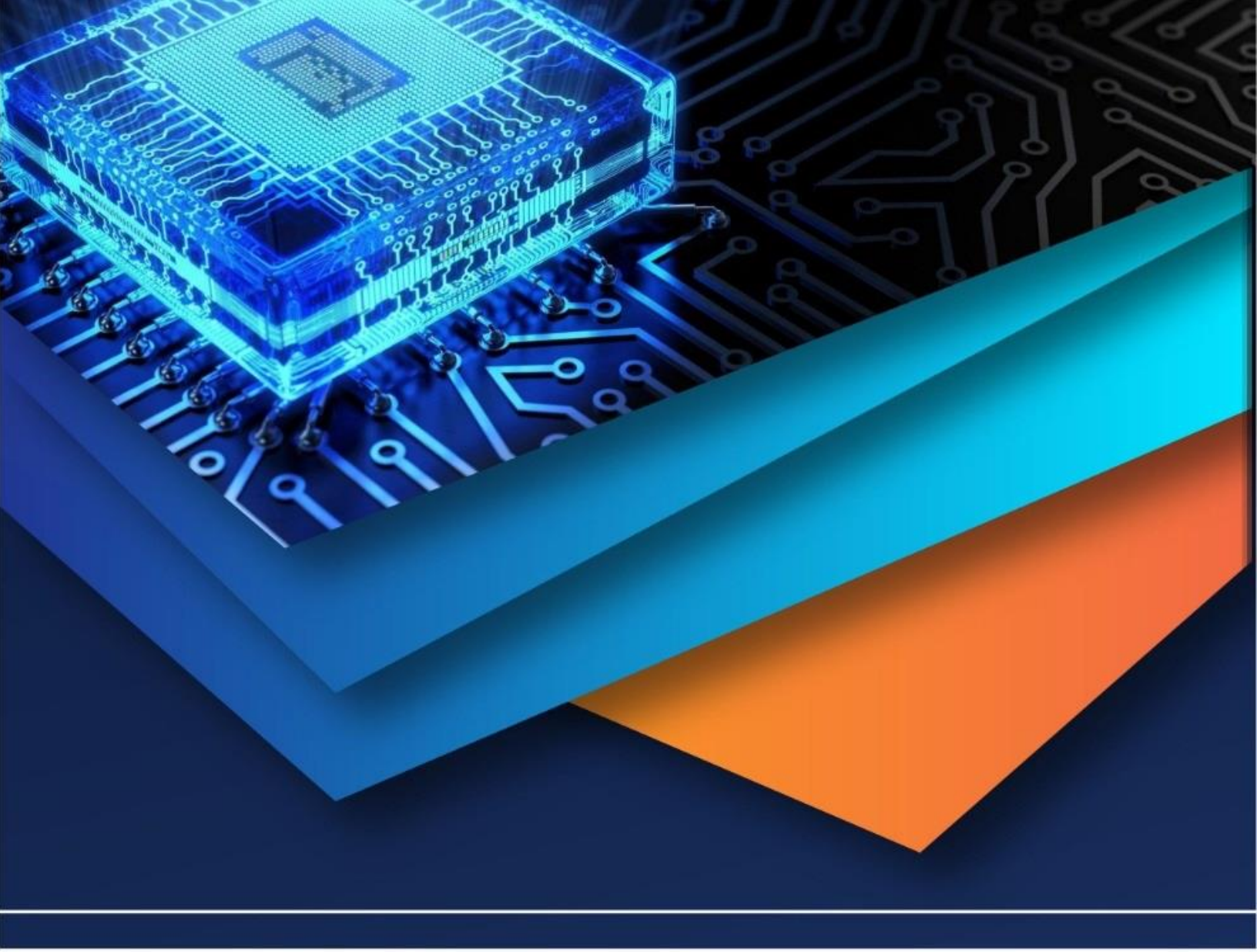

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