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Design of AMBA APB Protocol

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Abstract: Advanced Microcontroller Bus Architecture (AMBA) is an open specification in managing functional blocks which comprises of System-on-chips (SOCs). The design presents Advanced Peripheral Bus Protocol (APB) in detail. It is integrated into a system chipset. This paper revolves around building Advanced Microcontroller Bus Architecture (AMBA) Advanced Peripheral Bus (APB) protocol. The whole design is implemented using Verilog HDL, simulated and synthesized in Cadence tools.

I. INTRODUCTION

Today in this era of modern technology, multitudes of devices are integrated in SOC form. Every processor processors, memories and input/output devices. To(IP) blocks, bus systems are used. Several companies that are of SOCs. Today it is fair to say that the ARM industry standard for ASIC design for portable applications. Re-usable intellectual Property (IP) which is capable of enhancing an ARM core is very much important to any ASIC design centre. Intellectual an interconnection of many verified IP blocks that digital systems depend on Hardware Description Language (HDL) instead of schematic diagrams. These RTL codes are well tested for any use in the development of SOC

A. Description of AMBA Architecture

There are 5 versions of AMBA. Following is the history of AMBA

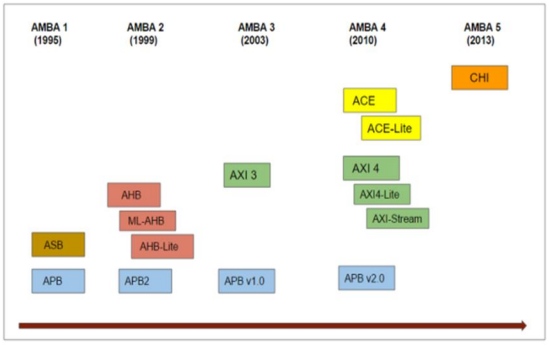


Fig1: AMBA history

AMBA Bus architecture components are Advanced High performance Bus (AHB), Advanced System Bus (ASB), Advanced Peripheral Bus (APB), Advanced eXtensible Interface (AXI), Advanced Trace Bus (ATB).

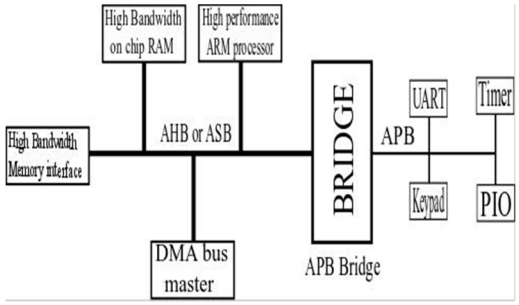


Fig2: AMBA bus architecture

APB has unpipelined protocol whereas AHB has pipelined protocol and can interface with high bandwidth and high performance required peripherals. Peripherals that can be connected to AHB are of high performance like On Chip RAM, and that APB are like UART and Keyboard.

B. APB Block diagram

The basic block diagram of APB is given as:

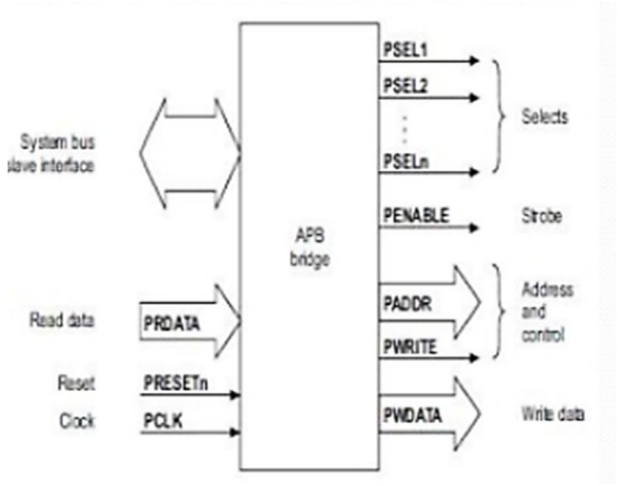


Fig 3: Basic block diagram of APB Bridge

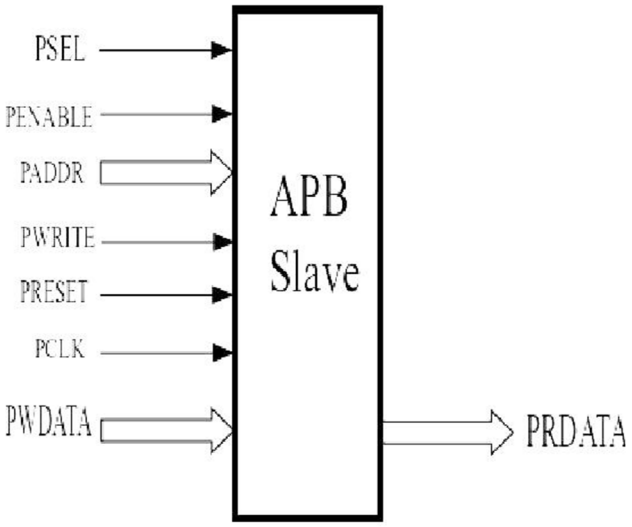


Fig 4: Basic block diagram of APB Slave

C. Operating States Of Apb

The following is the finite state machine of AMBA APB Protocol

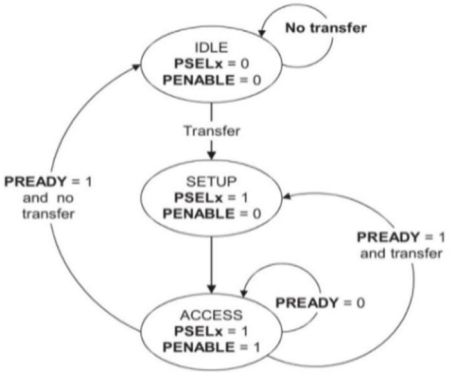


Fig 5: FSM of APB protocol

D. List Of Signals

SIGNAL	SIGNAL NAME
PCLK	Clock signal
PSEL	Select signal
PWRITE	Direction signal
PWDATA	32 bit write data bus
PREADY	Ready signal
PRESET	Reset signal
PENABLE	Enable signal
PADDR	32 bit address bus
PRDATA	32 bit read data bus

IDLE is the default state where there is no operation to be performed. The change in PSELx signal indicates the beginning of the SETUP state.

Whenever the transfer TRANS is HIGH, then the bus goes into the SETUP state. During this phase PWRITE, PADDR and PWDATA are provided. The bus will remain in the SETUP phase until the next rising edge of the clock arrives and moves to the ACCESS phase in the next clock cycle.

The start of ACCESS state is asserting the PENABLE signal. During this transition from SETUP to ACCESS state, all the control signals, data signals and address signals are remained to be in a stable condition.

In this phase, in case of READ operation PRDATA is present on the bus. For one clock cycle the PENABLE signal also remains HIGH.

Now, if there is no further data transfer then the bus moves to the IDLE state if there is further data transfer then it moves to the SETUP state.

E. APB Bridge module

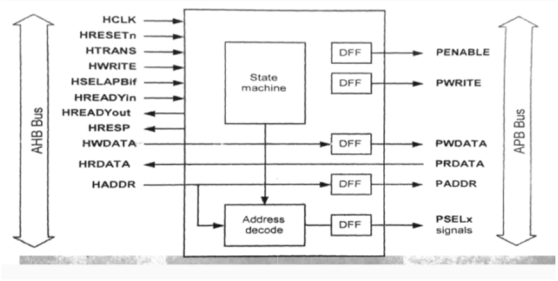


Fig 6: APB Bridge module

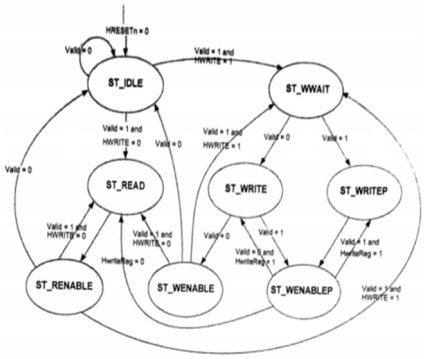


Fig 7: FSM of APB Bridge

II. SIMULATION AND SYNTHESIS RESULTS

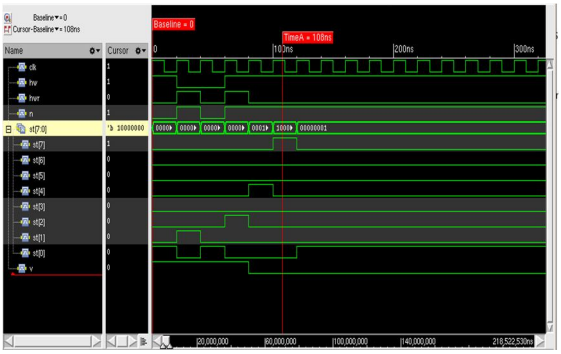


Fig 8: Simulation of APB Bridge

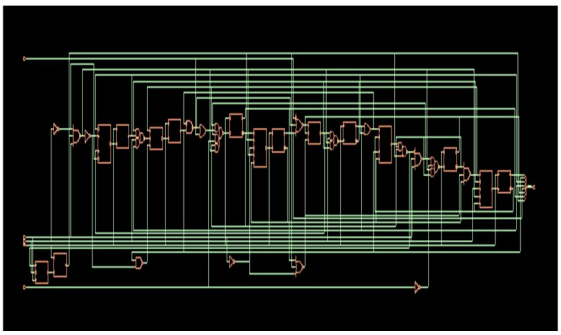


Fig 9: RTL schematic of APB Bridge

he cadence tool gives us the option of simulating and synthesizing a valid logic code. The Verilog code for APB Bridge is written and simulaed using cadence tool.

The above figures are the simulation graph and RTL Schematic diagrams of APB Bridge

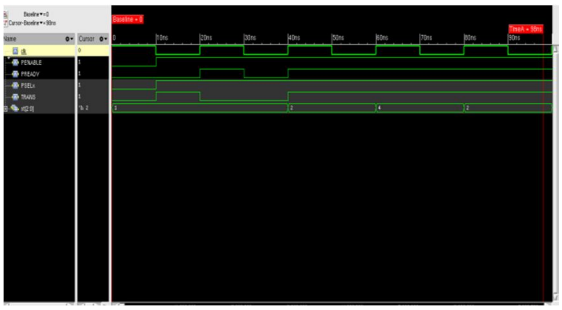


Fig 10: Simulation of APB slave

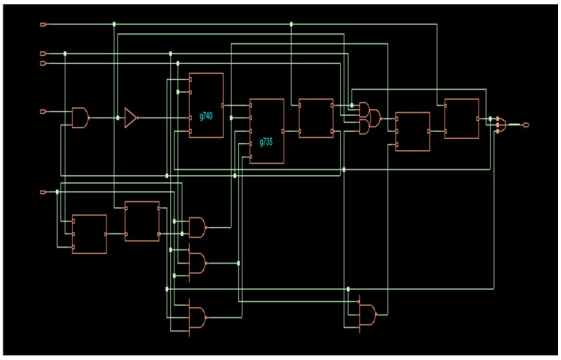


Fig 11: RTL schematic of APB slave

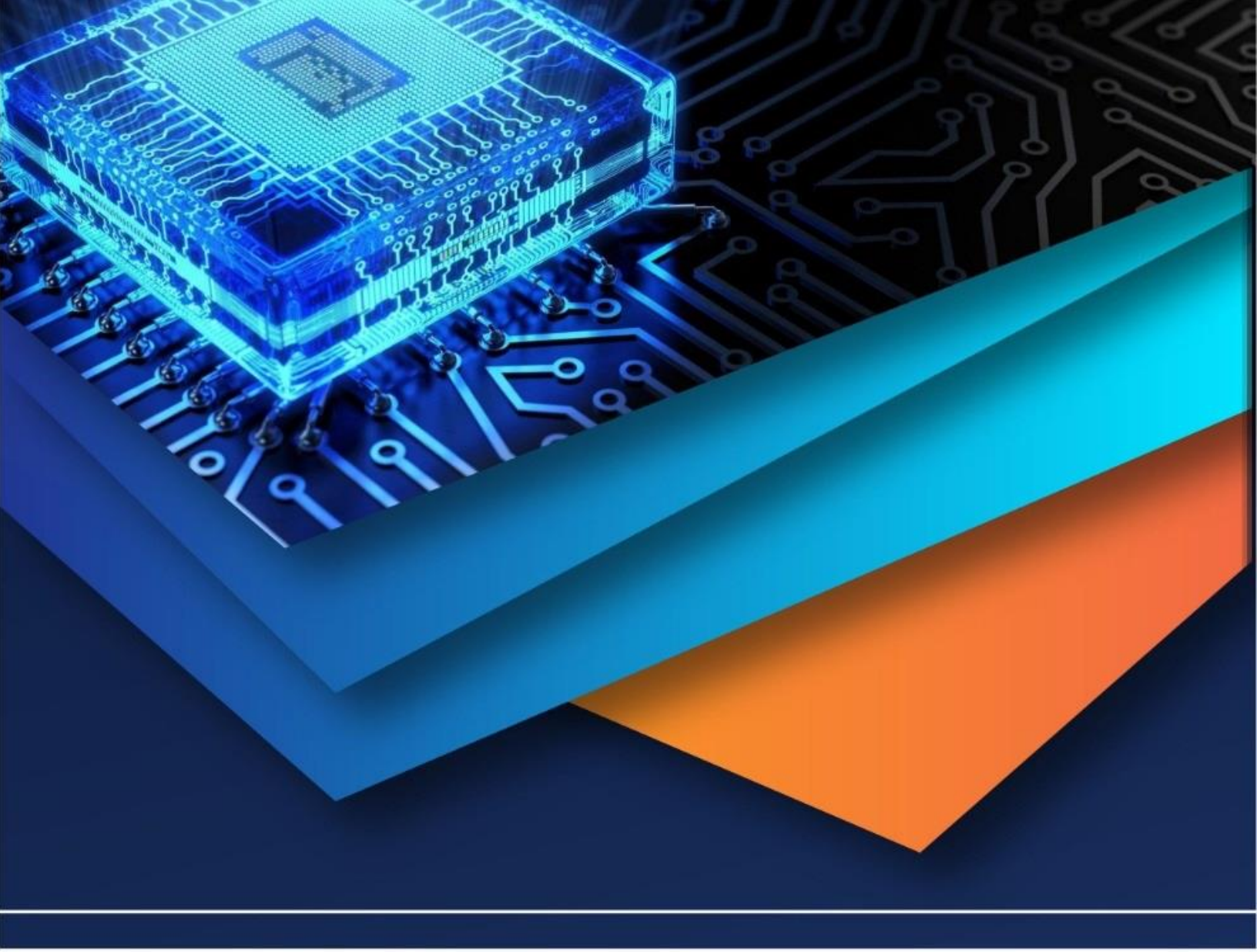
The Verilog code for APB slave is written and simulated using cadence tool. The simulation graph and RTL Schematic diagrams of APB slave are shown above. The design and test bench is written in Verilog and has been compiled using CADENCE Tools.

III. CONCLUSION

This Paper gives a detailed response of Advanced Microcontroller Bus Architecture (AMBA) and APB bus. The APB bus is coded and designed using Verilog HDL and is simulated using Cadence tools. The simulation results show the design of APB Bridge and APB Slave.

REFERENCES

[1] ARM, "AMBA Specification Overview", http://www.arm.com/.
[2] AMBA Specification (Rev 2.0).
[3] ARM, "AMBA APB3 Specification Overview", http://www.arm.com/
[4] Akhilesh Kumar, Richa Sinha, "Design and Verification analysis of APB3 Protocol with Coverage," IJAET, Nov 2011.
[5] Santhi Priya Sarekokku, K. Rajasekhar, "Design and Implementation of APB Bridge based on AMBA AXI 4.0," IJERT, Vol.1, Issue 9, Nov 2012.
[6] Xilinx ISE Synthesis and Verification Design Guide
[7] URL:http://www.testbench.com.
[8] Samir Palnitkar, "Verilog HDL: A guide to Digital Design and Synthesis (2nd Edition), Pearson, 2008.



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