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A general diode current versus voltage relationship is expressed as:

$$I = I_s * (e^{\frac{qV_f}{KT}} - 1)$$

$$\approx I_s * e^{\frac{qV_f}{KT}}$$

[As V_f is much greater than $\frac{KT}{q}$]

$$V_f = V_T * \ln \frac{I}{I_s}$$

Where K is the Boltzmann's constant ($1.38 * 10^{-23} \text{J/K}$) and q is the electronic charge ($1.6 * 10^{-19} \text{C}$).

In the conventional circuit, a pair of input voltages for the op-amp V_a and V_b , are controlled to be the same voltage. dV_f is the forward voltage difference between one diode D_1 and N diodes d_2 .

$$dV_f = V_{f1} - V_{f2}$$

$$= \dots\dots\dots (3)$$

The BGR output voltage V_{ref} then becomes

$$V_{ref} = V_{f1} + \frac{R_2}{R_3} dV_f = V_{ref-con}$$

V_{f1} has a negative temperature coefficient of $-2 \text{mv}/^\circ \text{C}$ whereas V_T has a positive temperature coefficient of $0.086 \text{mv}/^\circ \text{C}$.

Thus the V_{ref} is determined by the resistance ratio. The value of V_{ref} is about 1.25V which limits the low-voltage design for the CMOS circuit.

The concept of the proposed BGR is that two voltages V_T and V_f are generated by only one feedback loop. The PMOS transistor dimensions of p1, p2 and p3 are the same, and the resistance values of R_1 and R_2 are same.

We know that if the gates of PMOS transistors are connected they will draw equal currents. For the same reason, $I_1 = I_2 = I_3$

.In this case, $I_{1a} = I_{2a}$ and $I_{1b} = I_{2b}$.

$$dV_f = V_{f1} - V_{f2} = V_T * \ln(N)$$

I_{2a} is proportional to V_T

$$I_{2a} = \frac{dV_f}{R_3}$$

I_{2b} is proportional to V_{f1}

$$I_{2b} = \frac{V_{f1}}{R_2}$$

Here, I_2 is the sum of I_{2a} and I_{2b} , and I_2 is same as I_3 ,

$$I_3 = I_2 = I_{2a} + I_{2b}$$

Therefore, the output voltage of the proposed BGR, V_{ref} , becomes

$$V_{ref} = R_4 \left(\frac{V_{f1}}{R_2} + \frac{dV_f}{R_3} \right) \equiv V_{ref-prop}$$

If the resistor and diode parameters for the proposed BGR are the same as those for the conventional BGR, $V_{ref-prop}$ is simplified

$$as V_{ref-prop} = \frac{R_4}{R_2} * V_{ref-con}$$

Therefore, $V_{ref-prop}$ can be freely changed from $V_{ref-con}$ of 1.25V. V_{ref} For the proposed BGR is determined by the resistance ratio of R_2 , R_3 and R_4 and little influenced by the absolute value of the resistance. The transistors M_1 , M_2 and M_3 must operate in the saturation region, so that their drain-to-source currents are reduced.

In the Ref [12] the ordinary OP-AMP is used. We take the idea from Ref [6] to modify the OP-AMP for 1V operation. Implementation an OPAMP with 1V power supply is challenging. The OPAMP is modified as shown in fig.2.

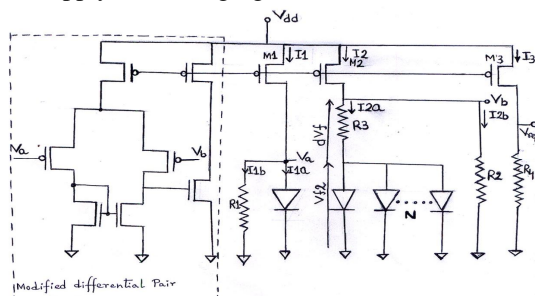


Fig.2

Using this modified OP-AMP and using the theory explained above the BGR circuit generated can operate definitely in sub 1V supply and can generate a reference voltage much lower than 1V..

The V_{dd} minimum for the BGR in fig2 can be successfully lowered by the SPICE simulation when the threshold voltages are optimized for a low-voltage operation. As we use the 0.25 technology the VTOs that are used, (-0.55V) for PMOS and (0.4V) for NMOS MOSFETs.

What I modify again in the circuit of fig2 is that I apply a feedback loop at the output of BGR to the (-Ve) input terminal of the modified OP-AMP. The modified BGR with the using of a feedback loop is shown in fig3.

We all are familiar with the (-ve) feedback amplifier. In

(-ve) feedback technique a very little part of output voltage or current are feeding to the input of the amplifier in out of phase. As a result the variation of the output voltage with the variation of the temperature reduces. And as a result we used to get a stable output even at the variation of the temperature in a large scale. This conception is used in this BGR circuit also.

Whenever we develop a BGR for low voltage, with the modification of OPAMP and by using the resistors and diodes only, but without using the feedback loop we get a low voltage at the output of BGR, but this voltage varies with temperature. When we add the feedback loop at the output of the same BGR we get a fully constant output with respect to the variation of temperature. The new BGR with feedback loop is shown in fig.3.

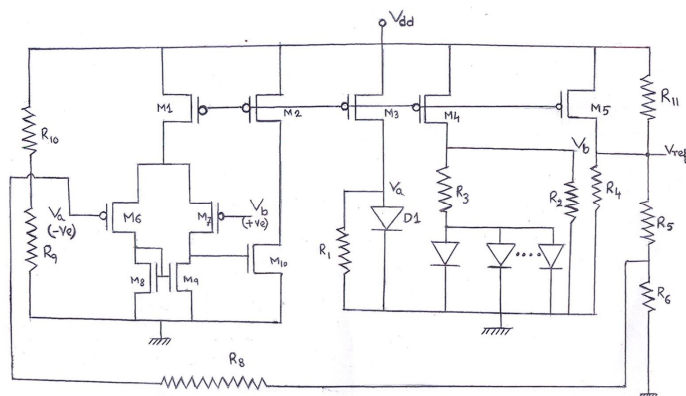


Fig3

Actually we take a little part of the output of the BGR through resistive subdivision method, and this voltage is feeding to the (-Ve) input terminal of the modified OPAMP to get a (-Ve) feedback. As a result the absolute constant BGR voltage is obtained. The changes of the BGR output without using feedback loop, and the BGR output with using feedback loop is shown in two tables. We can vary the output voltage of the new BGR by changing the values of two output resistances R5 and R6.

Two resistors R9 and R10 are used to stabilize the biasing of the modified BGR. We get a absolute stable voltage of any value below 1V at the output of the modified BGR by changing the values of the two output resistances R5 and R6 in sub 1-V operation.

Vdd(V)	Vref at -20°	Vref at 0°	Vref at 27°	Vref at 50°	Vref at 50°	Vref at 100°
1	0.1957	0.1938	0.1927	0.193	0.1933	0.195
0.8	0.077	0.082	0.088	0.093	0.098	0.105
0.6	0.005	0.110	0.021	0.027	0.032	0.040

Table-1

The variation of the BGR output voltage with the variation of the temperature in centigrade scale when no feedback loop is applied is shown in the above table1

Vdd(v)	Vref at -20°	Vref at 27°	Vref at 50°	Vref at 70°	Vref at 100°
1 V	0.018	0.018	0.018	0.018	0.018
0.8 V	0.047	0.047	0.047	0.047	0.047
0.6 V	0.011	0.011	0.011	0.011	0.011

Table2

The above table2 shows the changes in value of reference voltage with the variation of temperature in centigrade scale after using feedback loop.

The resistance R11 is also taking a important role in stabilize the biasing arrangement. If we not connect this resistance at this place we will never get any satisfactory result. It is clear from above two tables that we get almost stable, very low reference voltage after modifying the OP-AMP according to the circuit in fig2. But we get absolutely stable (absolute zero TC) and more low BGR voltage after adding the feedback loop. at different temperature and also we tried to show that how the BGR voltage varies with the resistance value. We also try to vary the different resistance values apart from the R11(which is the most important) to get a realisation of the variation of the Vref at different temp. The temperature coefficient (TC) of our BGR in PPm/0C is shown in table shown below:

Temp in centigrade	-20	-40	0	50	100
TC	0	0	0	0	0

Table-3

Now we can take a look at the Power supply rejection ratio of the Reference Generator. The followin table-4 shows the variation of the modified BGR with Different resistance values. PSRR is a measure of the variation of the output voltage with the variation of the supply voltage. PSRR mainly calculated at the unity gain configuration of the OPAMP.

Case-1	R1=1M	R2=1M	R3=1M	R4=1M	R5=1M	R6=1M	R8=1M	R9=1M	R10=1M	R11=1M
Value of Vref at different Temperature with different supply voltage										
Supply voltage	-40degree centigrade	-20 degree centigrade	0 degree centigrade	50 degree centigrade	100 degree centigrade					
15v	6.20	6.20	6.20	6.20	6.20					
3v	1.24	1.24	1.24	1.24	1.24					
0.7v	0.289	0.289	0.289	0.289	0.289					
0.01v	0.0041	0.0041	0.0041	0.0041	0.0041					
Case-2	R1=1M	R2=1M	R3=1M	R4=1M	R5=100M	R6=1M	R8=1M	R9=1M	R10=1M	R11=1M
Value of Vref at different Temperature with different supply voltage										
Supply voltage	-40 degree centigrade	-20 degree centigrade	0 degree centigrade	50 degree centigrade	100 degree centigrade					
15v	7.47	7.47	7.47	7.47	7.47					
3v	1.49	1.49	1.49	1.49	1.49					
0.7v	0.348	0.348	0.348	0.348	0.348					
0.01v	0.005	0.005	0.005	0.005	0.005					
Case-3	R1=100M	R2=1M	R3=1M	R4=1M	R5=100M	R6=1M	R8=1M	R9=1M	R10=1M	R11=1M
Value of Vref at different Temperature with different supply voltage										
Supply voltage	-40 degree centigrade	-20 degree centigrade	0 degree centigrade	50 degree centigrade	100 degree centigrade					
15v	6.42	6.42	6.42	6.42	6.42					
3v	1.28	1.28	1.28	1.28	1.28					
0.7v	0.299	0.299	0.299	0.299	0.299					
0.01v	0.004	0.004	0.004	0.004	0.004					

Table-4

We also tried to look the PSRR of the BGR circuit We calculated it at different temperature and showed it in tabular method in table-5. This result is calculated with the resistance values of

$R1=1M, R2=1M, R3=1M, R4=1M, R5=1M, R6=1M, R8=1M, R9=1M, R10=1M, R11=1M$.

Temperature in centigrade	-40	-20	0	50	100
PSRR in db	7.66	7.66	7.66	7.66	7.66

Table-5

We see that PSRR is fixed at different temperature but the value of PSRR is very high. This is the main disadvantage of this BGR. The two stage OPAMP will never have good PSRR unless some modifications are made. We can use Miller capacitance for the improvement of PSRR. The principle of the technique is to create an additional signal path from the power supply to the output which cancels the dominating unity gain signal path through the output stage. Anything affecting the gain of the feedback loop also affects the PSRR. As load current increases, the open loop output impedance decreases, thus lower the gain, increasing the load current also pushes the output pole to higher frequencies, which increases the feedback loop bandwidth. The net effect is increasing the load is therefore reduces the PSRR. This also can be proved directly from the table-4. From the Fig-3 (Modified BGR) we can see that resistance $R5$ is directly connected with the feedback loop. So when we increased the value of $R5$ the output of BGR also increased. This shows that this reduces the value of PSRR. The table-6 is shown below to give the reduced value of PSRR at different temperatures.

Temperature in centigrade	-40	-20	0	50	100
PSRR in db	6.05	6.05	6.05	6.05	6.05

Table-6

So we became successful to reduce the PSRR of our modified BGR of low power supply by varying the feedback resistance value.

We also analyze the circuit on the point of view of DC gain. As it is not an amplifier the gain reduces. So the gain in db is (-ve). The following table-7 shows the variation of gain in db with different values of resistance value that shown in table-5.

Different resistance value	Gain in db		Remarks
$R1=1M, R2=1M, R3=1M, R4=1M, R5=1M, R6=1M, R8=1M, R9=1M, R10=1M, R11=1M$	15V	7.67	For this combination of resistance the DC gain varies very little bit with input voltage..
	3v	7.67	
	0.7v	7.68	
	0.01v	7.74	
$R1=1M, R2=1M, R3=1M, R4=1M, R5=100M, R6=1M, R8=1M, R9=1M, R10=1M, R11=1M$	15V	6	For this combination of resistance the DC gain is totally constant
	3v	6	
	0.7v	6	
	0.01v	6	
$R1=100M, R2=1M, R3=1M, R4=1M, R5=100M, R6=1M, R8=1M, R9=1M, R10=1M, R11=1M$	15V	7.37	For this combination of resistance the DC gain varies very little bit with input voltage.
	3v	7.399	
	0.7v	7.389	
	0.01v	7.958	

Table-7

From the above table(Table-7) it is clear that the combination of the resistance value shown on row-2 is the most suitable for getting constant gain as well as lower PSRR. We can analyse the circuit also from the point of view of Signal to noise ratio of the circuit. For this we applied a white Gaussian Noise of 0.125v with our input supply voltage and measure the output voltage and its corresponding SNRs. The following table(Table-8) shows the calculated SNR in Tabular form. The SNR is calculated as: $20\log_{10}\left[\frac{V_{ref}}{(V_{supply}+V_{noise})}\right]$

Supply voltage	Noise Voltage	Vref at -20°	Vref at 27°	Vref at 50°	Vref at 70°	Vref at 100°	SNR in db
1 V	0.125v	1.125v	1.125v	1.125v	1.125v	1.125v	19.084
0.8 V	0.125v	0.925v	0.925v	0.925v	0.925v	0.925v	17.3846
0.6 V	0.125v	0.725v	0.725v	0.725v	0.725v	0.725v	15.268

So we can conclude that the noise performance of our BGR is very good. We know that the value of SNR should be high. We are getting a high value and it increases with the increasing of the supply voltage.

REFERENCES

- [1] CMOS Analog Circuit Design by Allen Holberg.
- [2] Design of analog cmos Integrated Circuits by Razavi.
- [3] A wide temperature range voltage Band gap Reference Generator by Anjani Kr.singh (and others) in Conference on Communication Technology (GCCT)
- [4] Novel CMOS Band gap Reference Circuit with Improved High-Order Temperature Compensation' by Koudounas, Charalambos M. Andreou and Julius Georgiou. Holistic research Lab, ECE Dept, University of Cyprus, Nicosia. A IEEE Journal of 2010
- [5] 'A high precision high PSRR band gap reference with thermal hysteresis protection' by Yang Yintang, Li Yani, and Zhu Zhangming. A journal of Chinese Institute of Electronics September 2020.
- [6] 'Design of Band Gap Reference and Current Reference Generator with Low Supply Voltage' by Dong-Ok Han, Jeong-Hoon Kim, and Heung Kim. A IEEE journal of 2008.
- [7] 'Low Noise Low Voltage Sub Band Gap Reference Voltage with PTAT Current Generator' by Muhammad M.EI. Kholy, Student Member. An IEEE journal of 2009.
- [8] 'Low-Voltage Band Gap Reference Design Utilizing Schottky Diodes' by David L. Butler and R. Jacob Baker. An IEEE journal of 2005.
- [9] 'Novel Start-Up Circuit With Enhanced Power-Up Characteristic For Band Gap references' by Tuan Vu Cao, Dag T. Wisland, Tor Severe Lande, Farshad Moradi, Young hee Kim. An IEEE journal of 2008.
- [10] 'A Sub-1-V Linear CMOS band Gap Voltage Reference' by Yang Welli, Wang Xichuan, Cai Jun' A journal of Microelectronic Research & Development Centre of Shanghai University.
- [11] 'Curvature Compensated BiCMOS Band Gap With 1V Supply voltage' by P. Malcovati, F. Malcovati, M. Pruzzi and C. Focci. A journal of Integrated Microsystems Laboratory, University of Pavia.
- [12] 'A low-Power Fully-MOSFET Voltage Reference Generator For 90nm CMOS Technology' by G. Di nardo, G. Lombardo, C. Paolino and G. Lullo. An IEEE Journal of 2006.
- [13] 'A CMOS Band Gap Reference Circuit For sub-1-V Operation Without Using Extra Low-Threshold-Voltage Device' by Ming Duo Ker, Jung-Sheng Chen, and Ching-Yun Chu. A IEEE journal of 2004.
- [14] 'A CMOS Band Gap Reference Without Resistor' by arne E. Buck, Charles L. McDonald (IEEE Members). A IEEE journal of 2002.
- [15] 'A CMOS Bandgap Reference Circuit with Sub-1-V Operation' by Hironori Banba, Hitoshi Shiga, Akira Umezawa, Takehi Miyaba, Toru Tanzawa, Shigeru Atsumi, and Koji Sakui, Member, IEEE.



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