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Review on Design Simulation of a Modified ALU Using QLUT

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***Abstract:** In VLSI interconnections are main contributor to delay, energy consumption and area Multiple-valued logic (MVL) allows the reduction of the required number of signals in the circuit, so can be effectively used to reduce the impact of interconnections. In this paper we propose an modified ALU which uses a quaternary logic look up table. The ALU is compatible with standard CMOS processes. The ALU is designed And Simulated Using TANNER. Schematics are designed using S-spice and simulated in T-spice.*
***Keywords:** Multiple valued logic (MVL), Quaternary logic look up table (QLUT), TANNER, Arithmetic logic unit (ALU)*

I. INTRODUCTION

In today's world where the use of semiconductor technology is explosive main concern is to reduce power consumption, delay and energy. Number of interconnections is main contributor to this problem. Multiple-valued logic allows reduction in number of interconnects in circuit, hence can serve as a mean to effectively cut down the impact of interconnects by decreasing average power required for level transitions and number of interconnections required. Using multiple valued look up table (LUT) designed using single power supply and single voltage mode is better than binary LUT. A quaternary look up table is delay area and energy efficient as compared to binary look up table since consuming 122µW power. An ALU which is designed by mapping binary LUT into quaternary LUT with integrated circuits is more efficient than binary ALU. The transistor count can be reduced to one fourth of the binary circuits by using circuits which are based on quaternary logic using voltage mode structures by mapping binary LUT into quaternary LUT using integrated linear programming. This ALU is power, area and cost effective also. The ALU can be implemented in multiple valued voltage mode logic (MV- VML). The arithmetic and logical operations can be performed with less number of gates in this way which reduces the depth of net.

II. DOWN LITERAL CIRCUIT

The down literal circuit (DLC) divides a multiple valued signal into a binary signal at an arbitrary threshold value. DLC consists variable threshold voltage values by way of controlling only two bias voltages. Therefore, DLC is very useful circuit element in quaternary logic or any multiple value logic system.

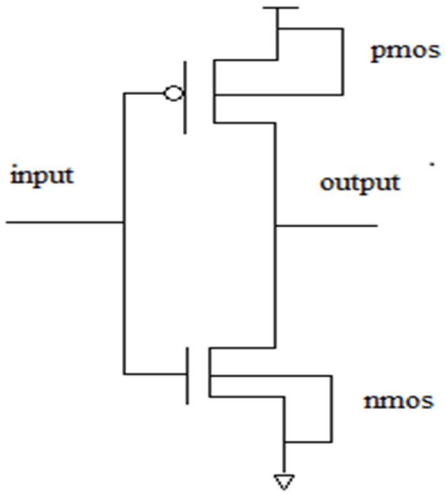

Figure 1: Circuit diagram of DLC

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III. QUATERNARY LOGIC

As the name suggests a quaternary variable can have four possible values that means a system implemented in quaternary logic has four different logic levels. The three different reference voltage values required to determine a quaternary value are 1/6 VDD, 3/6 VDD, 5/6 VDD. From this we can say that a quaternary variable holds double information as compared to a binary variable this can be given mathematically by following relation:

$$| V_Q| = 2 X |V_B| \quad (1)$$

Where, V_Q is quaternary variable and V_B is binary variable A group of two binary variables can be considered as a quaternary variable without any loss of information.

IV. LOOK UP TABLE

Look-up tables (LUT) are digital blocks which can store data depending on function implemented. The basic element of look-up table is multiplexer. Number of stages required to implement given functionality define the switching of data. The multiplexers to be used depend upon the number of input processed in LUT and radix of number system. The desired result or data are programmed and attached to the LUTs. A n-bit look-up table is designed using multiplexer with select lines as inputs to the LUT. The capacity of an LUT |C| is given by

$$C=n \times b^k \quad (2)$$

Where n: outputs, k: inputs and b: logic values for a function.

V. QUATERNARY LOOKUP TABLE

The quaternary look-up table (QLUT) has 16 inputs and the basic multiplexer used is 4 × 1 MUX. It have 4 quaternary input, a delta literal circuit are connected as select input to multiplexer.

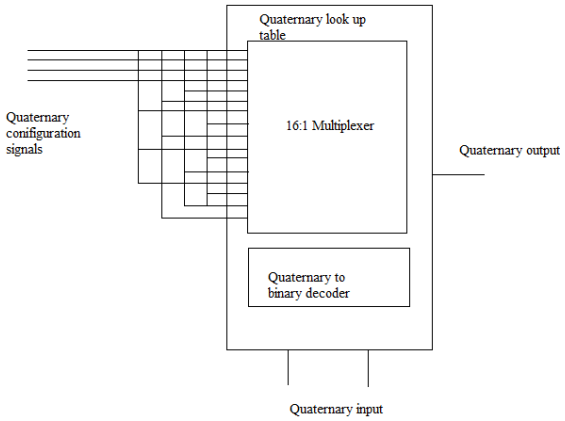

Figure 2: Block diagram of Quaternary lookup table

The total functions implemented in an LUT with k input are given by

$$F = b^{|C|} \quad (3)$$

Where $C= n \times b^k$ from equation (2) and b: logic values for a function. For a LUT with a single output (n = 1), the number of different functions for binary

(b =2) and quaternary (b =4) representations is given, respectively, by

$$|F2|=2^{2k} =4^k \; |F4|=4^{4k} =256k \quad (4)$$

From equation (4) it is evident that the number of possible functions that may be represented in a quaternary LUT is much larger than in a binary LUT with the same number of inputs and outputs this means using quaternary logic systems along with reduced interconnections number of gates used are also reduced.

A. 16:1 multiplexer

The main reason of selecting a multiplexer to design LUT is that it can also be used as adder, subtractor, divider or any arithmetic operation in the ALU along with the LUT. As we know a 16:1 multiplexer will have 16 inputs lines one output and four select line in a binary system but because of the use of quaternary to binary decoder the select lines are reduced to two.

B. Quaternary to binary (Q to B) decoder

The Q to B decoder is important component which is responsible for reducing the select lines from four to two. It fetches quaternary input and converts it into binary to perform regular operations of the designed system. The decoder allows the use of a single row of switches to drive the input configuration signals to the output of the QLUT for this purpose 16 control signals are generated which are applied to clock input of each switch. The switches connect input to the output. For generation of required control signals the quaternary configuration variables are converted into binary so as to use binary logic gates.

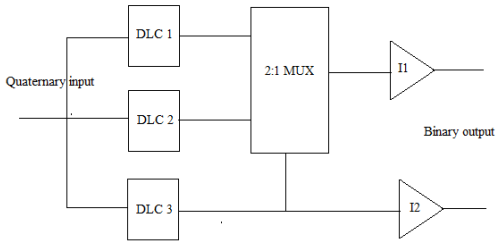

Figure 3: Block diagram of Q to B converter

C. Binary to quaternary (B to Q) decoder

Since the internal operations are done in binary at the output side a binary to quaternary decoder is required. The functionality of this decoder is reversed of the Q to B decoder used at the input side.

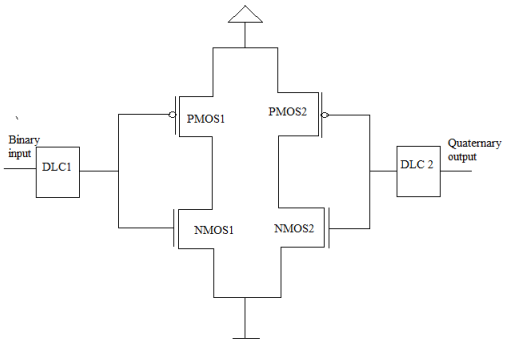

Figure 4: Block diagram of B to Q

VI. LITERARTURE REVIEW

A. Few researches were analyzed on the design and use of QLUT. DiogoBrito, Jorge Fernandes, Paulo Flores, Jose Monteiro, Taimur Rabuske [10] propose a new look-up table structure based on a low-power high-speed quaternary voltage-mode device and a clock boosting technique to enhance speed without increasing consumption. In this paper authors have given only idea of high speed look up table is given devices are not implemented.

B. In research paper [3] authors have given idea of a look up table in binary technology they have used a full adder to demonstrate a programming technique using binary functionality for increased functional density in quaternary Look-up table-based field programmable gated arrays (FPGAs).

C. Regarding to the advantages of MVL over binary logic many researches are done researches have studied and compared different parameters of circuit efficiency with binary and MVL by implementing different circuits of standard COMS technologies in MVL. In paper [5] E. Ozer, R. Sendag, and D. Gregg have proposed multiple value logic buses which can lower the power consumption of the designed system.

D. In research paper [7] the authors have studied the impact of using quaternary logic instead of binary logic on the performance of a look up table and concluded with several parameters comparison that the use of quaternary logic not only enhances the speed of look up table by reducing the delay it also makes the LUT area and power efficient. They have designed circuit with standard

CMOS processes, employing single voltage supply designed using voltage-mode structures. Presented in this work is quaternary lookup table (QLUT) able to work at 1MHz consuming 36.48 μW. The experimental results demonstrate the correct quaternary operation estimate the power efficiency of the proposed design.

E. Paper [8] proposes a clock boosting technique is used to optimize the switches resistance and power consumption. This technique overcomes several limitations found in previous quaternary implementations published so far, such as the power-hungry current-mode cells. They have implemented a prototype adder based on the proposed LUT. The experimental results confirm the power efficiency of the proposed design.

F. In paper [11] authors have designed and implemented an AU (arithmetic unit) based on QLUT. Addition, Subtraction and multiplication i.e. arithmetic operations in Modulo-4 and in galois field logic are design and simulation results are shown in this paper by using Quaternary logic.

VII. CONCLUSION

A. It has been seen from various researches and experiments that using quaternary look up table (QLUT) for implementing mathematical functions in standard CMOS technology is more beneficial than using conventional binary LUT. It reduces the number of required interconnections, hence reducing the impact of interconnections on overall energy consumption. Area power & delay are expected to be further reduced by using an ADP efficient adder. One fourth of transistor usage is expected. (ALU) employed using quaternary logic by mapping binary LUT into the quaternary LUT using integrated linear circuits is more efficient than binary arithmetic logic unit (ALU) in term of area and speed required.

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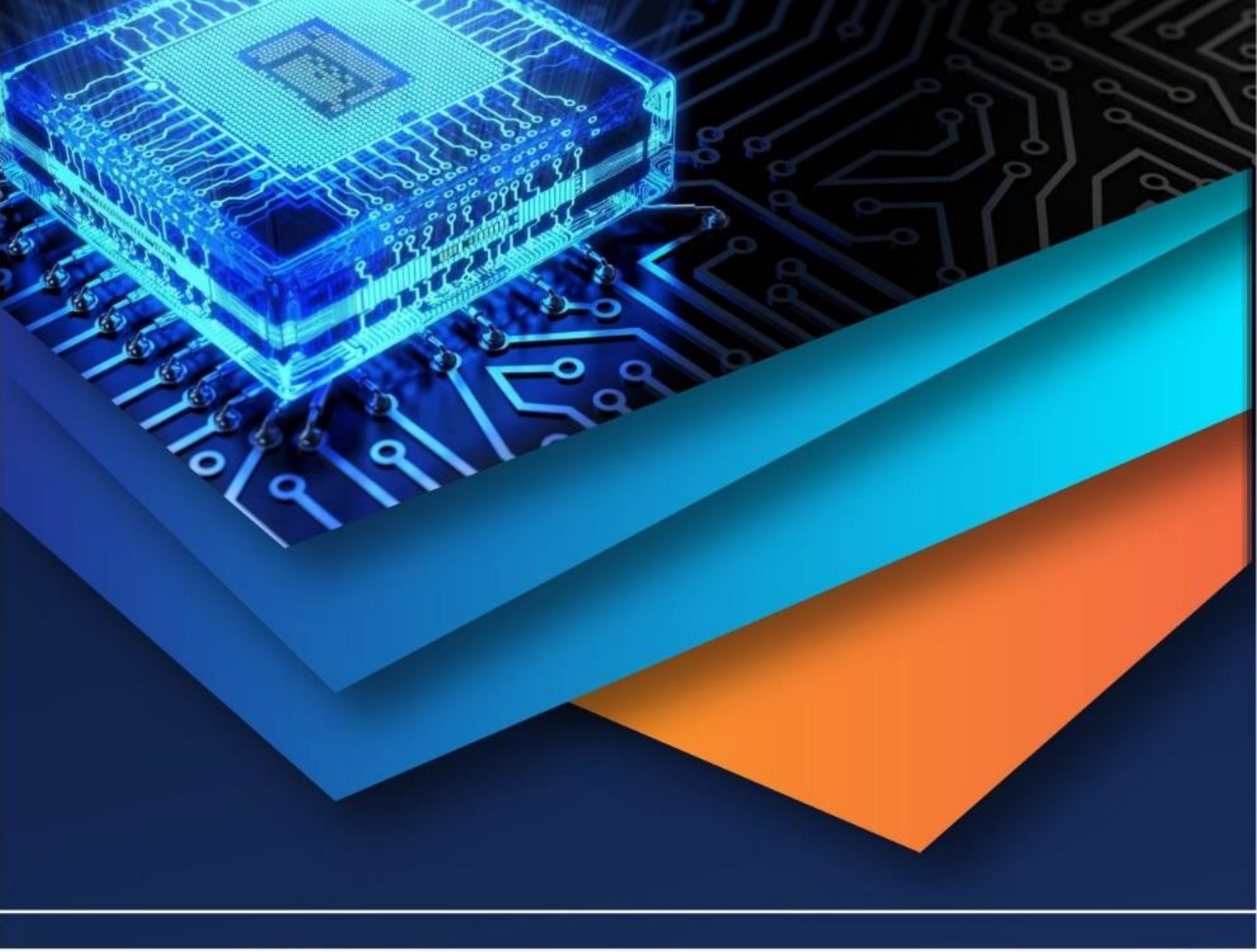

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