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# Design of Pulse Triggered Flip-Flop and Analysis of Average Power

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**Abstract-** In this brief, Pulse-triggered FF (P-FF) is a single-latch structure which is more popular than the conventional transmission gate (TG) and master-slave based FFs in high-speed applications. Low power design has become one of the main concerns in Very Large Scale Integration design. Among the various building blocks in digital designs, one of the most complex and power consuming is the flip-flop. As transistors used have small area and low power consumption, they can be used in various applications like digital VLSI clocking system, buffers, registers, counters, microprocessors etc. Proper selection of flip-flop is necessary in order to satisfy low power and high performance circuit. The investigation of conventional and proposed pulse Triggered flip-flop using pass transistor logic flip-flop is done with comparisons of average power which claims that proposed design is suitable for low power applications. The circuits are simulated with Metal Oxide Semiconductor Field Effect Transistor using TANNER EDA and CANDENCE GPDK180 nm process technology. The average power consumption of proposed pulse triggered flip-flop using pass transistor logic is 40.94 $\mu$ W and the number of transistors used 17.

**Index Terms**—Flip-flop (FF), low power, pulse triggered.

## I. INTRODUCTION

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift where power dissipation has become as important a consideration as performance and area. So this Low Power Pulse Triggered Flip Flop reviews various strategies and methodologies for designing low power circuits and systems. It describes the many issues facing designers at architectural, logic, circuit and device levels and presents some of the techniques that have been proposed to overcome these difficulties. The article concludes with the future challenges that must be met to design low power, high performance systems. Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs now a-days often adopt intensive pipelining techniques and employ many FF-rich modules such as register file, shift register, and first in-first out. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 50% of the total system power. FFs thus contribute a significant portion of the chip area and power consumption to the overall system design. A P-FF consists of a pulse generator for strobe signals and a latch for data storage. If the triggering pulses are sufficiently narrow, the latch acts like an edge-triggered FF. Since only one latch, as opposed to two in the conventional master-slave configuration, is needed, a P-FF is simpler in circuit complexity. This leads to a higher toggle rate for high-speed operations. P-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. Despite these advantages, pulse generation circuitry requires delicate pulse width control to cope with possible variations in process technology and signal distribution network. In a statistical design framework is developed to take these factors into account. To obtain balanced performance among power, delay, and area, design space exploration is also a widely used technique. In this brief, we present a novel low-power P-FF design based on a signal feed-through scheme. Observing the delay discrepancy in latching data 1 and 0, the design manages to shorten the longer delay by feeding the input signal directly to an internal node of the latch design to speed up the data transition. This mechanism is implemented by introducing a simple pass transistor for extra signal driving. When combined with the pulse generation circuitry, it forms a new P-FF design with enhanced speed and power-delay-product (PDP) performances.

## II. CONVENTIONAL P-FF DESIGNS

P-FFs, in terms of pulse generation, can be classified as an implicit or an explicit type. In an implicit type P-FF, the pulse generator is part of the latch design and no explicit pulse signals are generated. In an explicit type P-FF, the pulse generator and the latch are separate. Without generating pulse signals explicitly, implicit type P-FFs is in general more power-economical. However, they suffer

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from a longer discharging path, which leads to inferior timing characteristics. Explicit pulse generation, on the contrary, incurs more power consumption but the logic separation from the latch design gives the FF design a unique speed advantage. Its power consumption and the circuit complexity can be effectively reduced if one pulse generator is shares a group of FFs (e.g., an n-bit register). In this brief, we will thus focus on the explicit type P-FF designs only.

### A. EP-DCO: explicit -Data closed to output Flip-Flop

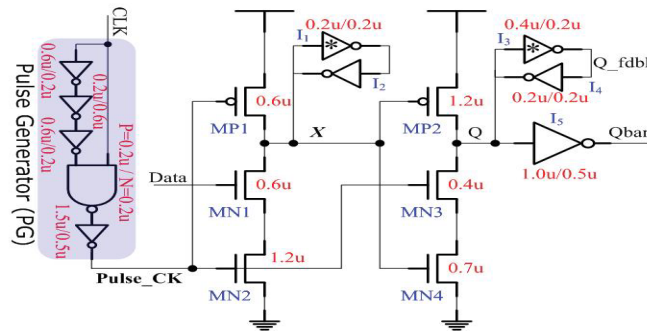


Fig.2.1(a) EP-DCO

To provide a comparison, some existing P-FF designs are reviewed first. Fig. 2.1(a) shows a classic explicit P-FF design, named data-closed- to- output (ep-DCO). It contains a NAND-logic-based pulse generator and a semi dynamic true single-phase-clock (TSPC) structured latch design. In this P FF design, inverters I3 and I4 are used to latch data, and inverters I1 and I2 are used to hold the internal node  $X$ . The pulse width is determined by the delay of three inverters. This design suffers from a serious drawback, i.e., the internal node  $X$  is discharged on every rising edge of the clock in spite of the presence of a static input “1.” This gives rise to large switching power dissipation. To overcome this problem, many remedial measures such as conditional capture, conditional precharge, conditional discharge, and conditional pulse enhancement scheme have been proposed .

### B. CDFF: conditional discharged Flip- Flop

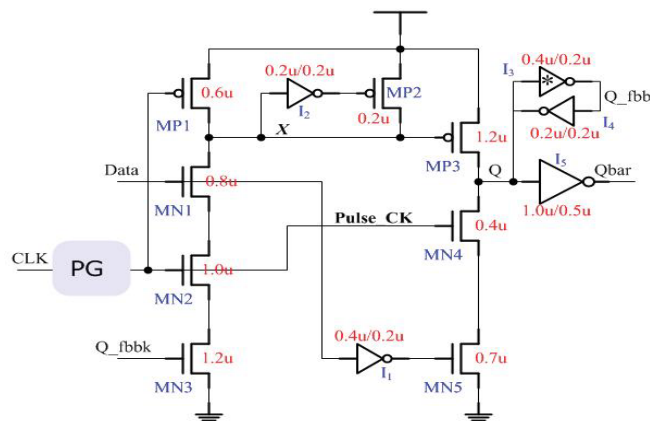


Fig.2.1(b)CDFF

Fig. 2.1(b) shows a conditional discharged (CD) technique. An extra nMOS transistor MN3 controlled by the output signal  $Q\_fbbk$  is employed so that no discharge occurs if the input data remains “1.” In addition, the keeper logic for the internal node  $X$  is simplified and consists of an inverter plus a pull-up pMOS transistor only.

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## C. SCDFF: Static- conditional discharged Flip-Flop

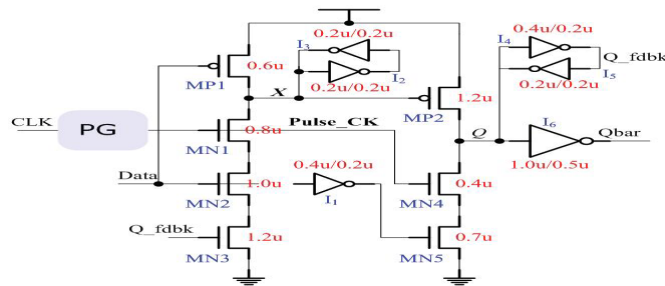


Fig.2.1(c) SCDFF

Fig. 2.1(c) shows a similar P-FF design (SCDFF) using a static conditional discharge technique. It differs from the CDFF design in using a static latch structure. Node  $X$  is thus exempted from periodical precharges. It exhibits a longer data-to-Q (D-to-Q) delay than the CDFF design. Both designs face a worst case delay caused by a discharging path consisting of three stacked transistors, i.e., MN1–MN3. To overcome this delay for better speed performance, a powerful pull-down circuitry is needed, which causes extra layout area and power consumption. The modified hybrid latch flip-flop (MHLFF).

## D. MHLFF: Modified hybrid latch flip flop

Fig. 2.1(d) also uses a static latch. The keeper logic at node  $X$  is removed. A weak pull-up transistor MP1 controlled by the output signal  $Q$  maintains the level of node  $X$  when  $Q$  equals 0. Despite its circuit simplicity, the MHLFF design counters two drawbacks. First, since node  $X$  is not precharged, a prolonged 0 to 1 delay is expected. The delay deteriorates further, because a level-degraded clock pulse (deviated by one  $V_T$ ) is applied to the discharging transistor MN3. Second, node  $X$  becomes floating in certain cases and its value may drift causing extra dc power.

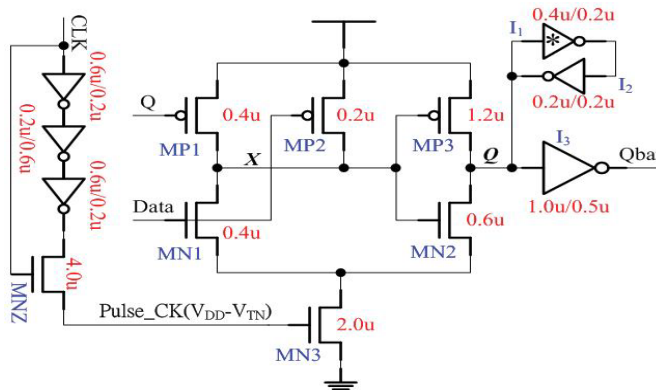


Fig.2.1(d) MHLFF

## E. TSPCFF: True single phase clock flip-flop

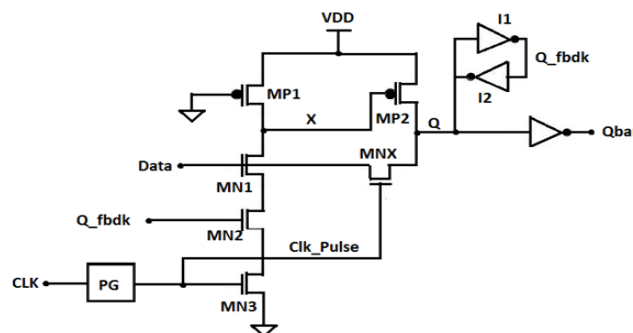


Fig.2.1(e)TSPCFF design



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In figure.2.1(e) [14] shows the TSPC pulse triggered flip-flop, a novel P-FF design by employing a modified TSPC latch structure incorporating a mixed design style consisting of a pass transistor and a pseudo-nMOS logic. The key idea was to provide a signal feed through from input source to the internal node of the latch, which would facilitate extra driving to shorten the transition time and enhance both power and speed performance. The design was achieved by employing a simple pass transistor. All circuits encounter the same worst case timing occurring at 0 to 1 data transitions, the design adopts a signal feed-through technique to improve this delay. This gives rise to a pseudo-nMOS logic style design, and the charge keeper circuit for the internal node X can be saved. In addition to the circuit simplicity, this Similar to the SCDFE design, the PFF design also employs a static latch structure and a conditional discharge scheme to avoid superfluous switching at an internal node. However, there are three major differences that lead to a unique TSPC latch structure and make this PFF design distinct from the previous one. First, a weak pull-up pMOS transistor MP1 with gate connected to the ground is used in the first stage of the TSPC latch. approach also reduces the load capacitance of node X. Second, a pass transistor MN<sub>x</sub> controlled by the pulse clock is included so that input data can drive node Q of the latch directly (the signal feed-through scheme). Along with the pull-up transistor MP2 at the second stage inverter of the TSPC latch, this extra passage facilitates auxiliary signal driving from the input source to node Q. The node level can thus be quickly pulled up to shorten the data transition delay. Third, the pull-down network of the second stage inverter is completely removed. Instead newly employed pass transistor MN<sub>x</sub> provides a discharging path. The role played by MN<sub>x</sub> is thus two fold, i.e., providing extra driving to node Q during 0 to 1 data transitions, and discharging node Q during “1” to “0” data transitions. The circuit savings of the PFF design include a charge keeper (two inverters), a pull-down network (two nMOS transistors), and a control inverter. The only extra component introduced is an nMOS pass transistor to support signal feed through. This scheme actually improves the “0” to “1” delay and thus reduces the disparity between the rise time and the fall time delays. On the other hand, if a “0” to “1” data transition occurs, node X is discharged to turn on transistor MP2, which then pulls node Q high. However, with the signal feed through scheme, a boost can be obtained from the input source via the pass transistor MN<sub>x</sub> and the delay can be greatly shortened. The MN<sub>x</sub> conducts only for a very short period. When a “1” to “0” data transition occurs, transistor MN<sub>x</sub> is likewise turned on by the clock pulse and node Q is discharged by the input stage through this route. In addition, since a keeper logic is placed at node Q, the discharging duty of the input source is lifted once the state of the keeper logics inverted. It has high hold time which reduces the speed of Operation and increases average power. Due to charging and discharging in flip-flop, it consumes some power. When compares all flip-flop design, main drawback is power consumption and number of transistor used in flip-flop. i.e., transistor count. In existing pulse triggered flip-flop design of conditional capture technique, a set-up time has increases, so it is the performance limiting parameter. In conditional discharge pulse triggered flip-flop causes extra layout area and power consumption. In modified hybrid latch flip-flop, it causes extra dc power consumption. In conditional pulse enhancement scheme pulse triggered flip-flop causes extra layout area in pulse generation circuit. So the main objective of the project to reduce number of transistor count and average power consumption in pulse triggered flip-flop design.

#### F. PROPOSED FLIP FLOP

In figure.2.2 shows the Proposed pulse triggered flip-flop design discharging path using PTL. Transistor N2, in conjunction with an additional transistor N3, forms a two-input pass transistor logic (PTL)-based AND gate to control the discharge of transistor N1.

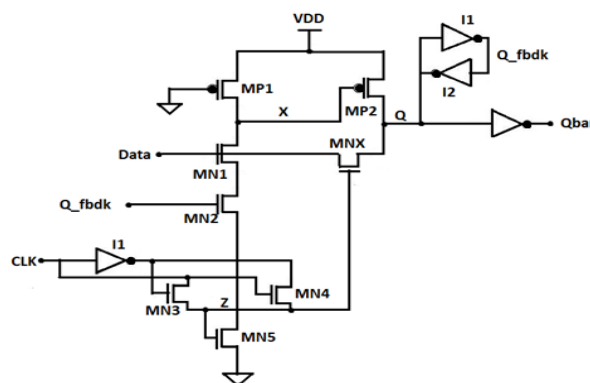


Fig.2.2.proposed FF design

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The proposed design, as shown in Fig. 2.2, adopts two measures to overcome the problems associated with existing PFF designs. The first one is reducing the number of nMOS transistors stacked in the discharging path. The second one is supporting a mechanism to conditionally enhance the pull down strength when input data is "1." Refer to Fig. 2.2, As opposed to the transistor stacking design in Fig.2.1 (a),(b),(c),(d) and (e), this PFF design discharging path using PTL. Transistor N2, in conjunction with an additional transistor N3, forms a two-input pass transistor logic (PTL)-based AND gate to control the discharge of transistor N1. Since the two inputs to the AND logic are mostly complementary (except during the transition edges of the clock), the output node Z is kept at zero most of the time. When both input signals equal to "0" (during the falling edges of the clock), temporary floating at node Z is basically harmless. At the rising edges of the clock, both transistors N2 and N3 are turned on and collaborate to pass a weak logic high to node Z, which then turns on transistor N1 by a time span defined by the delay inverter I1. The switching power at node Z can be reduced due to a diminished voltage swing. Unlike the MHLLF design, where the discharge control signal is driven by a single transistor, parallel conduction of two nMOS transistors (N2 and N3) speeds up the operations of pulse generation. With this design measure, the number of stacked transistors along the discharging path is reduced and the sizes of transistors N1-N3 can be reduced also. In this design, the longest discharging path is formed when input data is "1" while the Qbar output is "1." It steps in when node X is discharged VTP below the VDD. This provides additional boost to node Z (from VDD-VTH to VDD). The generated pulse is taller, which enhances the pull-down strength of transistor N1. After the rising edge of the clock, the delay inverter I1 drives node Z back to zero through transistor N3 to shut down the discharging path. This means to create a pulse with sufficient width for correct data capturing, a bulky delay inverter design, which constitutes most of the power consumption in pulse generation logic, is no longer needed. It should be noted that this conditional pulse enhancement technique takes effects only when the FF output Q is subject to a data change from 0 to 1. This leads to a better power performance than those schemes using an indiscriminate pulse width enhancement approach. Another benefit of this conditional pulse enhancement scheme is the reduction in leakage power due to shrunken transistors in the critical discharging path and in the delay inverter.

### III. RESULTS

The performance of the proposed P-FF design is evaluated against existing designs through post-layout simulations. The compared designs include four explicit type P-FF designs shown in Fig. 1, an implicit type P-FF design named Sdff, a TG latch based P-FF design ep-SFF, plus two non-P-FF designs. One of them is a conventional TG master-slave-based FF (TGFF) and the other one is an adaptive-coupling-configured FF design (ACFF). A conventional CMOS NAND-logic-based pulse generator design with a three-stage inverter chain as show in Fig. 1(a) is used for all P-FF designs except the MHLLF design, which employs its own pulse generation circuitry as specified in Fig. 2.1(d).

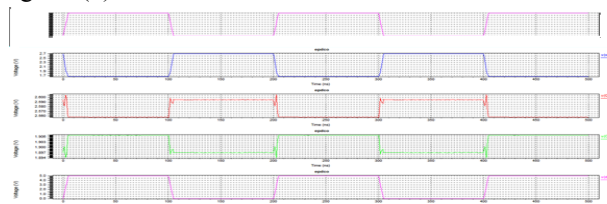


Fig.3(a) ) EP-DCO flip-flop waveform in tanner tool.

It shows the Glitches appear at the output that would cause noise problem. The internal node X is discharged on every rising edge of the clock inspite of the presence of a static input "1." This gives rise to large switching power dissipation.

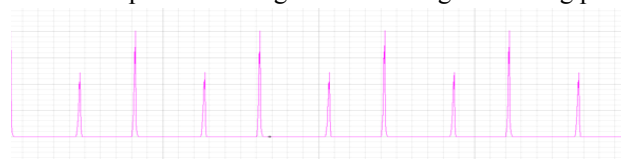


Fig.3(b) ) EP-DCO flip-flop power waveform in cadence tool.

It shows the average power consumption of explicit data close to output flip-flop is 88.76μw. The peak power is 98.16 μw. The number of transistors used in explicit data to output flip-flop design is 28.

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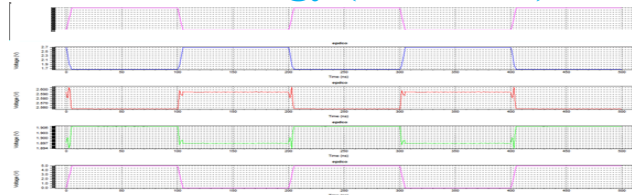


Fig.4(a) CDFF waveform in tanner tool.

It shows the designs face a worst case delay caused by a discharging path consisting of three stacked transistors, i.e., MN1–MN3. To overcome this delay for better speed performance, a powerful pull-down circuitry is needed, which causes extra layout area and power consumption.

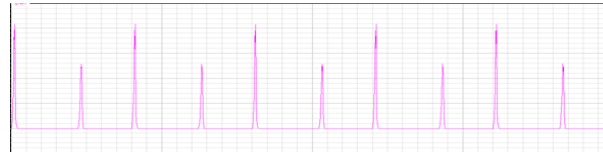


Fig.4(b) CDFF power waveform in cadence tool.

It shows the average power consumption of conditional discharge flip-flop is 55.61  $\mu\text{W}$ . The peak power is 92.18  $\mu\text{W}$ . The number of transistors used in conditional discharge flip-flop is 31.

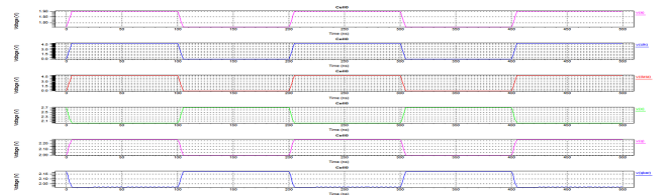


Fig.5(a) SCDFFWaveform in tanner tool.

At the rising edge, N3 and N4 turn on for the short transparency duration, causing the input D to propagate to the output. The keeper maintains the output state. During the D transparency period, when input D is stable high, X goes low, causing Q to go high.

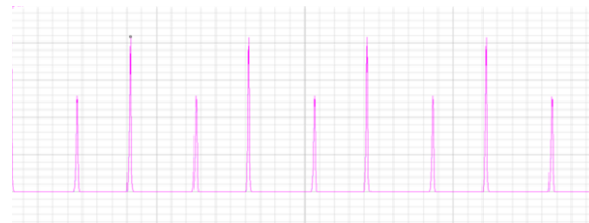


Fig.5(b) SCDFFWpower waveform in cadence tool.

It shows the average power consumption of static conditional discharge flip-flop is 54.74  $\mu\text{W}$ . The peak power is 87.69  $\mu\text{W}$ . The number of transistors used in static conditional discharge flip-flop design is 30.

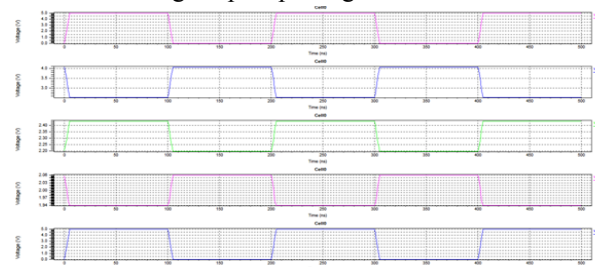


Fig.6(a) MHLFF waveform in tanner tool.

The modified hybrid latch flip-flop design eliminates the unnecessary discharging problem it shows in output waveform. The drawback of this design is that node becomes floating, when output Q and input Data both equal to “1”. It consumes extra power consumption.

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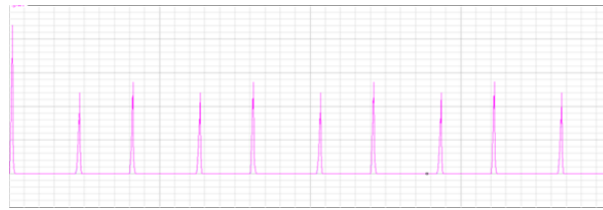


Fig.6(b) MHLFF power waveform in cadence tool.

It shows the average power consumption of modified hybrid latch flip-flop is  $49.49\mu\text{W}$ . The peak power is  $82.43\mu\text{W}$ . The number of transistors used in modified hybrid latch flip-flop design is 19.

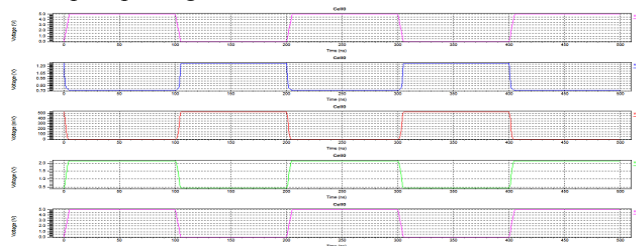


Fig.7(a) TSPC flip-flop waveform in tanner tool.

When both input signals equal to “0” (during the falling edges of the clock), temporary floating at node Z is basically harmless.



Fig.7(b) TSPC flip-flop power waveform in cadence tool.

It shows the average power consumption of True single phase clock flip-flop is  $48.99\mu\text{W}$ . The peak power is  $80.43\mu\text{W}$ . The number of transistors used in True single phase clock flip-flop design is 24.

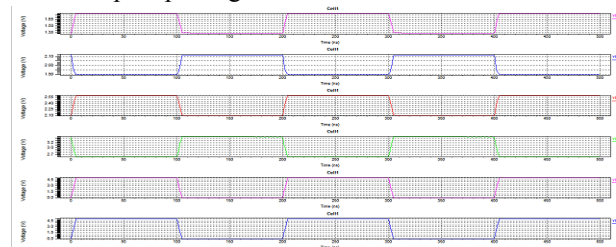


Fig.8(a) proposed flip-flop waveform in tanner tool.

It shows each period of clock signal is 10ns and pulse width is 5ns. The data is given and corresponding output Q is produced. Pulse triggered flip-flop are sensitive to any change of the input levels during the clock pulse is still HIGH, the inputs must be set up prior to the clock pulses rising edge and must not be changed before the falling edge.

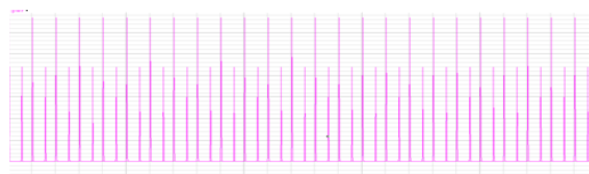


Fig.8(b) proposed flip-flop power waveform in cadence tool.

It shows the average power consumption of proposed pulse triggered flip-flop is  $40.94\mu\text{W}$ . The peak power is  $78.67\mu\text{W}$ .

The number of transistors used in proposed pulse triggered flip-flop is design is 17. It achieves reduced average power and area



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when compared to the other designs.

The target technology is the TSMC 90-nm CMOS process. Since pulse width design is crucial to the correctness of data capture as well as the power consumption, the transistors of the pulse generator logic are sized for a design spec of 120 ps in pulse width in the TT case. The sizing also ensures that the pulse generators can function properly in all process corners. With regard to the latch structures, each P-FF design is individually optimized subject to the product of power and D-to-Q delay. To mimic the signal rise and fall time delays, input signals are generated through buffers. Since the proposed design requires direct output driving from the input source, for fair comparisons the power consumption of the data input buffer (an inverter) is included. The output of the FF is loaded with a 20-fF capacitor.

**Table 1. Comparison of various P-FF designs**

<b>P- FF(PULSE TRIGGER FLIP- FLOP)</b>	<b>EP- DC O</b>	<b>SCD FF</b>	<b>CD FF</b>	<b>M HL FF</b>	<b>TSP C FF</b>	<b>Prop osed pulse trigge red flip- flop</b>
<b>NO.OF TRANSIST OR</b>	<b>28</b>	<b>31</b>	<b>30</b>	<b>19</b>	<b>24</b>	<b>17</b>
<b>AVG. POWER (<math>\mu</math>W)</b>	<b>88.7 6</b>	<b>55.6 1</b>	<b>54. 6</b>	<b>49. 4</b>	<b>48.99</b>	<b>40.94</b>

## IV. CONCLUSION

In this Paper, the various Flip flop design like, EP-DCO, MHLLF, SCDF, CDF, TSPC based P-FF & Proposed NEW P-FF are discussed. The pulse triggered Flip Flop (P-FF) design by employing two new design measures. The first one successfully reduces the number of transistors stacked along the discharging path by incorporating a PTL based AND logic. The second one supports conditional enhancement to the height and width of the discharging pulse so that the size of the transistors in the pulse generation circuit can be kept minimum. These were been also designed in Cadence & Tanner Tool those result waveforms are also discussed. The comparison table also added to verify the designed methods using UMC CMOS 90-nm technology. With these all results Proposed PTLFF performed speed or power better than EP-DCO, MHLLF, SCDF, CDF and TSPCFF designs.

In this brief, we presented a novel P-FF design by employing a modified TSPC latch structure incorporating a mixed design style consisting of a pass transistor and a pseudo-nMOS logic. The key idea was to provide a signal feedthrough from input source to the internal node of the latch, which would facilitate extra driving to shorten the transition time and enhance both power and speed performance. The design was intelligently achieved by employing a simple pass transistor. Extensive simulations were conducted, and the results did support the claims of the proposed design in various performance aspects.

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