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A Novel Method for Diagnosis of Faults Caused At Multiple Locations

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Abstract— Testing is an important early step in design of VLSI. With tens of billions of transistors being integrated in one chip, multiple faults may exist. To accurately and efficiently identify the fault locations, a cube-based EPP analysis technique is proposed. The calculated percentage represents the EPP of the injected fault. In the circuit, the cube values of location at the initial stages are altered and the error count is calculated. This is done until the error count reduces to zero. Both the techniques are applied to ISCAS '89 benchmark circuits and the parameters such as area, speed and power are computed. It can be observed that the area and power are reduced remarkably by EPP method compared to FEG method and the speed increases approximately by 7 times. The results show that the EPP method is more advantageous than the graph-based approach.
Keywords—fault tolerance, reliability, probability-based, multiple fault diagnosis.

I. INTRODUCTION

In the production of integrated circuits, testing is done to identify defective chips. Testing is also done to diagnose the reason for a chip failure in order to improve the manufacturing process. Testing a digital circuit involves applying an appropriate set of input patterns to the circuit and checking for the correct outputs. However, built-in self-test (BIST) techniques have been developed in which some of the tester functions are incorporated on the chip enabling the chip to test itself. BIST provides a number of well-known advantages. It eliminates the need for expensive testers. It provides fast location of failed units in a system because the chips can test themselves concurrently. The increasing pin count, operating speed, and complexity of IC's is outstripping the capabilities of external testers. BIST provides solutions to these problems. Fig. 1. is a block diagram showing the architecture for BIST. The circuit that is being tested is called the circuit-under-test (CUT). There is a test pattern generator which applies test patterns to the CUT and an output response analyzer which checks the outputs. The test pattern generator must generate a set of test patterns that provides high fault coverage in order to thoroughly test the CUT.

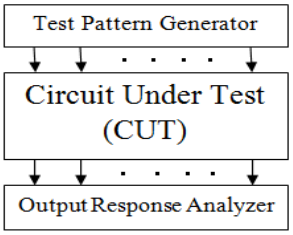


Fig. 1. Block Diagram for BIST

Pseudo-random testing is an attractive approach for BIST. A linear feedback shift register (LFSR) can be used to apply pseudo-random patterns to the CUT. An LFSR has a simple structure requiring small area overhead. Moreover, an LFSR can also be used as an output response analyzer thereby serving a dual purpose.

II. BACKGROUND

In [1], an effective multiple defect diagnosis methodology that does not depend on failing pattern characteristics. The methodology consists of a conservative defect site identification and elimination algorithm, and an innovative path-based defect site elimination technique. But, it can be used only for Single Location At a Time (SLAT) type of problems. A diagnosis of interconnect opens was

proposed in [2] which considers any possible open location along the defective line using the full open segment (FOS) model. However, open faults even when diagnosed, are not accurate. In [3], an SLAT pattern which is a failing pattern which can be explained by a single location fault. SLAT patterns are used to build up a composite picture of the multiple faults using the fewest faulty locations. But on extending them to diagnose delay faults, the assumption that the fault simulation results match delay defect behavior in real silicon becomes unrealistic. Two fault-diagnosis methods for improving multiple-fault diagnosis resolution are proposed in [4].This is ineffective as it has overhead in area and delay. In [5], a graph-based approach is used in which Fault Element Graph (FEG) is constructed to diagnose the faults. This method, although it identifies multiple fault locations, is with less accuracy.

III. EPP BASED APPROACH

To accurately and efficiently evaluate the error propagation probability, we propose a cube-based EPP analysis technique. Percentage represents the EPP of the injected fault. Monte Carlo simulation is highly accurate but very time consuming because it needs to feed the whole input set for each fault to obtain an EPP. Therefore, existing Monte Carlo simulation techniques have to trade off accuracy against computational complexity In contrast; static analysis uses the probability theory to compute EPPs. Fig. 2. provides an example for an example of using cubes and covers.

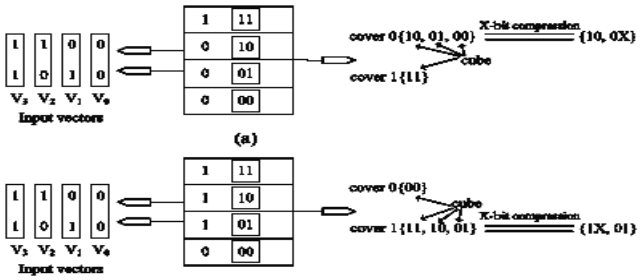


Fig. 2. Example of EPP cube and covers

For example, in order to find the cubes that have an output value 0 under both the AND logic and the OR logic, an interface calculation on cover 0 of the AND logic and cover 0 of the OR logic is given as follows:

$$\{10, 01, 00\} \text{ I } \{00\} = \{10 \text{ I } 00, 01 \text{ I } 00, 00 \text{ I } 00\}$$

$$= \{00\}.$$

On the other hand, the adjoin of two cubes, denoted as a V b, is the union of two cubes a, b. Assuming the signal probability of each input wire is equivalent, the method proposed can use structural information to quickly estimate signal probabilities of internal wires that interconnect LUTs. Afterwards, EPPs are computed by using signal probabilities for off path wires and by using error propagation rules for on path wires. With the help of probability theory, static analysis only needs to traverse the entire circuit just twice to obtain EPPs for all faults, so its computational complexity is very low.

A. Computation Of EPP

EPP is computed by tracing the paths in the circuit and assigning probabilities to the paths based on the number of gates present in the path. This could be easily explained by using the CUT in the Fig. 3.

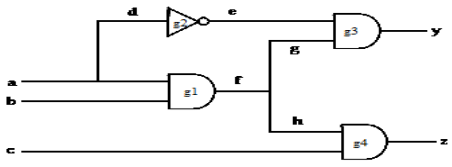


Fig. 3. Example CUT

The truth table of the given example circuit is given in Fig. 4.

Inputs			Outputs	
a	b	c	y	Z
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	0
1	0	0	0	0
1	0	1	0	0
1	1	0	0	0
1	1	1	0	1

Fig. 4. Truth table for fault-free CUT

Introducing the faults at locations a and e with SA-0 and SA-1 respectively as shown in Fig. 5.

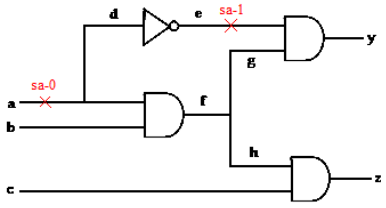


Fig. 5. Example CUT with faults

A comparator is used to compare between the faulty and fault-free values and can be identified.

By exercising the input patterns, the failure patterns are found to be p1=110 and p2=1110. This could be given by the truth table in Fig. 6. This is noted for the first step alone and stored, so that it can be utilized for the steps until the entire computation is over. Even though, there are variations at each stage's output, the initial table is used for comparison.

Inputs			Outputs	
a	b	c	y	Z
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	0
1	0	0	0	0
1	0	1	0	0
1	1	0	1	0
1	1	1	1	1

Fig. 6. Truth table for faulty CUT

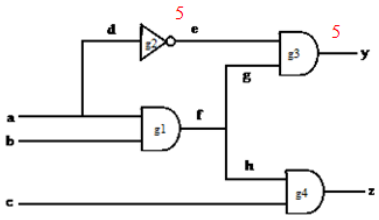
The paths in the circuit correspond to the propagation from the primary input to the primary output. There are six paths existing in the example CUT, and it can be given as follows:

- p1 – a – d – e – y
- p2 – a – f – g – y
- p3 – a – f – g – y
- p4 – b – f – g – y
- p5 – b – f – h – z
- p6 – c – z

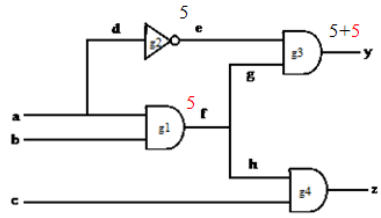
Using these paths the EPP computation is done. Considering path p1, the number of gates encountered in the path is 2, hence, the probability is equally divided as 5 and 5 (taking total probability as 10, for easier calculation).

The value is equally divided among the gates encountered in the path. If there are two gates it is divided into (10/2=5) for each gate. If there are three gates, each gate has (10/3=3.33) distributed equally and so on.

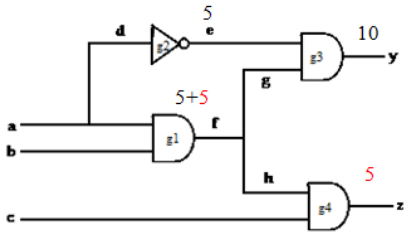
Considering each path, the EPP assignment is given in Fig. 7.



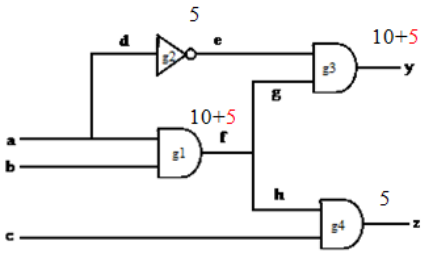
(a) EPP for path p1



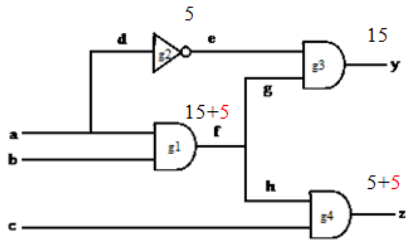
(b) EPP for path p2



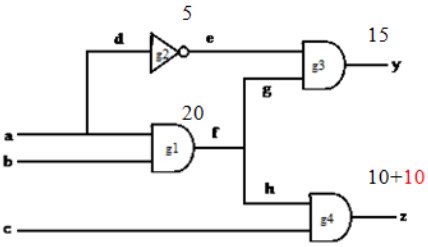
(c) EPP for path p3



(d) EPP for path p4



(e) EPP for path p5



(f) EPP for path p6

Fig. 7. EPP step 1

The total EPP at each gate is computed and tabulated in Table I.

The computed EPP values reveal that the scores are high at gates g1 and g4. Hence, these two gates are to be considered for the inversion cube technique in the next step. While inverting the cubes, the error count seems to vary. If the error count tends to reduce then the gate is listed as a faulty element. Else the gate is left out of consideration. The EPP score is then updated and the procedure is continued until the error count is zero.

TABLE I
EPP SCORE TABLE

GATE	EPP
g1	20
g2	5
g3	15
g4	20

Inverting the cubes at each gate yields a different output and error count which is given in Fig. 8.

a	b	c	y	z
0	0	0	1	0
0	0	1	1	1
0	1	0	1	0
0	1	1	1	1
1	0	0	0	0
1	0	1	0	1
1	1	0	0	0
1	1	1	0	0

Fig. 8. Truth table after inversion in step 1

Thus, the gate g1 and g4 are with no error. In the next step, EPPs are to be reassigned without considering the gates eliminated during the step 1. In the next step, only one path exists between the primary input and the output, a-d-e-y. The updated EPP is given in Fig. 9.

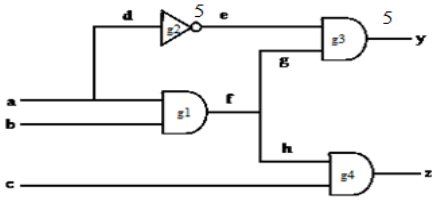


Fig. 9. Updated EPPs for step 2

Taking gates g2 and g3 for this step, the truth table gets changed which resembles the table in Fig. 9. Thus, it can be concluded that the error is present in the path between primary input 'a' and primary output 'y', through path a-d-e-y. Hence, there is a faster and easier identification of the solution.

IV. SIMULATION

A. Schematic Of CLB Based Adder

The methods are tested using a CLB based adder. The CLB blocks are made up of AND, OR and EX-OR gates. It consists of numerous elements which are named as CLB_(gate type)_(gate number). Faults are injected at certain locations randomly and both the procedures are applied via coding. Once applied, the results can thus be tabulated and compared.

Fig. 10. shows the schematic of the CLB based adder used for testing. Its simulation results are specified below.

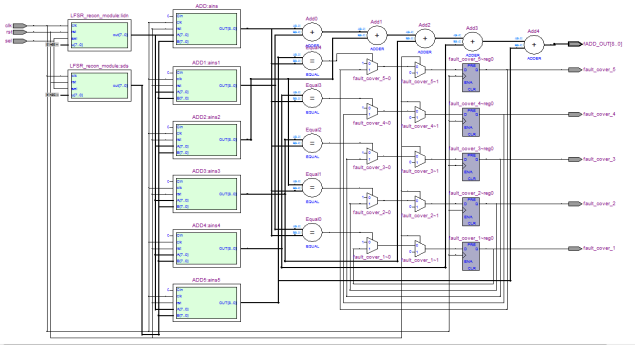


Fig. 10. Schematic of CLB Based Adder

The output produced by the graph-based technique is given in Fig. 11.

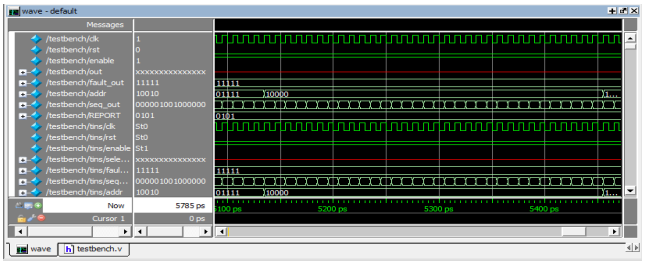


Fig. 11. Output of Graph Based method

The error count need to be calculated at each step and can be related to the EPP percentage. If the path has 10 gates, the probability is assigned as 1 each and the gate which holds a number of values are summed up and given as a whole value. This leads to a huge value at the gate which is associated with more number of gates. The error count in the output is given in Fig. 12.

```
# @time=          9945,Error_count=206
# EPP_80_percentage
# Incorrect_output
# @time=          9955,Error_count=207
# EPP_80_percentage
# Incorrect_output
# @time=          9965,Error_count=208
# EPP_80_percentage
# Incorrect_output
# @time=          9975,Error_count=209
# EPP_80_percentage
# Incorrect_output
# @time=          9985,Error_count=210
# EPP_80_percentage
# Incorrect_output
# @time=          9995,Error_count=211
# EPP_80_percentage
# Incorrect_output
# @time=          10005,Error_count=212
```

Fig. 12. Faults identified in the adder

The faults were injected at 5 locations and all the locations are identified under this method.

B. Comparison

The comparison of the results obtained by applying both the Graph-based approach and EPP method are tabulated in Table II.

TABLE II
COMPARISON OF RESULTS

	Graph- based approach	**EPP method**
No. of Logic Elements (Area)	2325	38
Dynamic Power (mW)	24.22	1.26
Speed in Frequency (MHz)	134.21	931.1

It can be observed from the results that the power consumption is reduced and area utilized is reduced remarkably from the graph-

based approach to the EPP method. The speed is increased by approximately 7 times.

The parameters can be given in the form of a bar chart in Fig. 13.

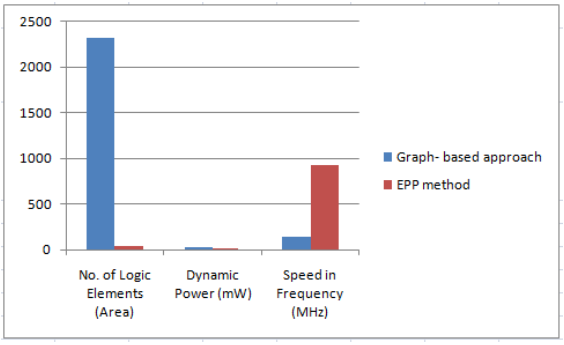


Fig. 13. Bar chart showing the comparison of parameters

The number of logic elements used is less compared to other techniques as the need for registers in storing the failure patterns is removed. Dynamic power is remarkably reduced and the speed is enormously increased in multiples of 7.

V. CONCLUSION

The multiple faults were detected using other existing techniques and the results were compared. In the future, a new single cycle access test structure for logic test. It will eliminates the unnecessary dynamic power consumption problem of conventional shift-based scan chains during switching transition in the scan FF and also reduces the accessing time into one clock cycles. This leads to more realistic circuit behavior during stuck-at and at-speed tests. It enables the complete test to run at much higher frequencies equal or close to the one in functional mode. In this work complexity will be increased linearly with design level. In order to retain the design complexity by grouping the design units as a various independent pages and accessing will be carried out by selecting pages.

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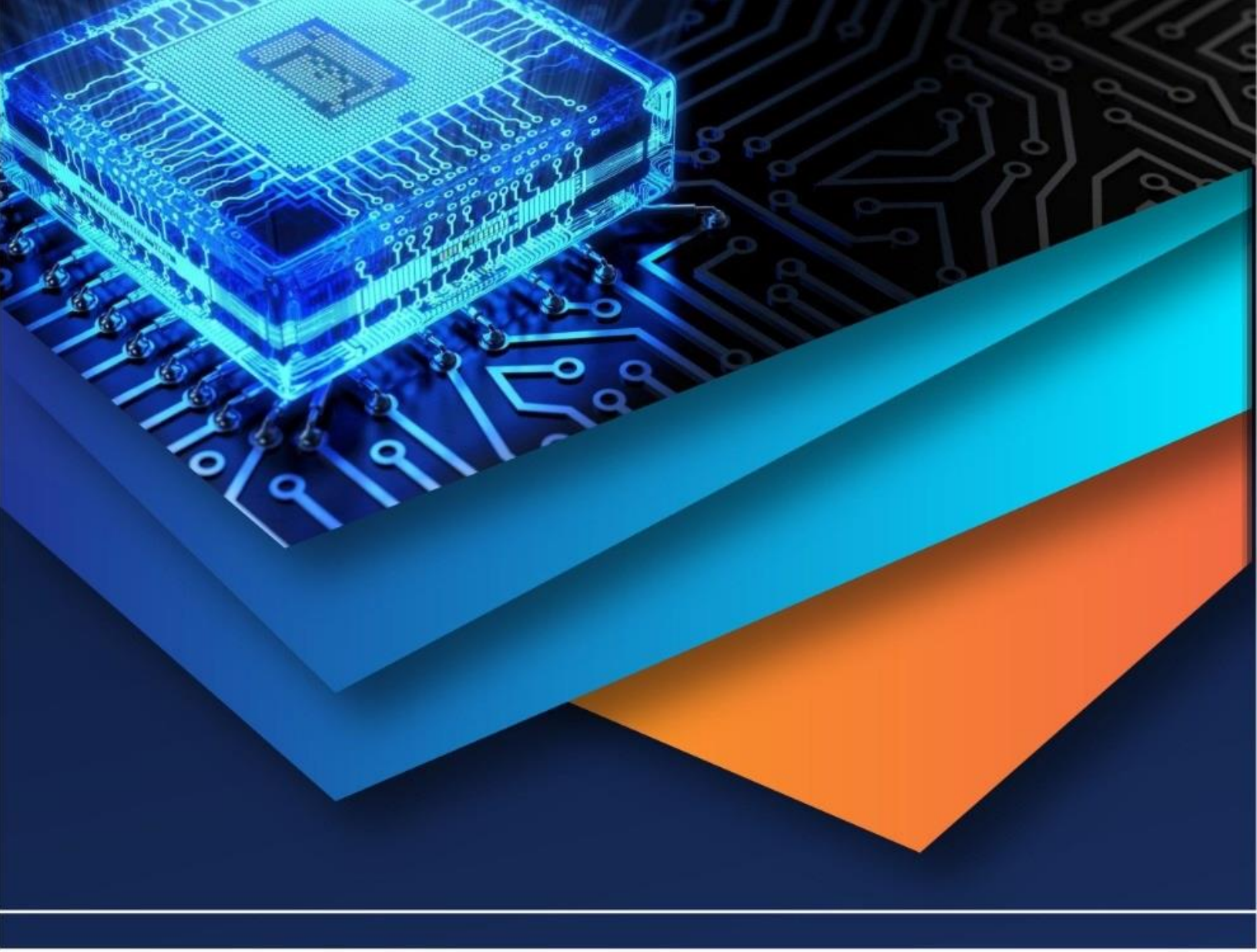

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