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Three Phase Three Level ZVS DC-DC Converter with Asymmetrical Duty Cycle Control

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Abstract—This paper proposes development of soft switching scheme for three phase three level DC-DC converter for different duty cycles to achieve ZVS for all switches. The ZVS is achieved with output inductor and leakage inductor of transformer. This paper describes the main operational modes of proposed converter for different duty cycle and simulation results are observed and compare the switching losses of proposed converter with and without ZVS.
KEYWORDS—Zero Voltage Switching (ZVS), Three Phase Three Level (TPTL),DC-DC converter ,Pulse width modulation ,Duty cycle ,Soft switching.

I. INTRODUCTION

In high voltage high power applications the ordinary converters exists many problems like stress on switches, switching losses, EMI etc…. These problems can be eliminated by using ZVS and ZCS converters. In ZVS, the switches are turned on and off at zero voltages and in ZCS, the switches are turned on and off at zero currents. As a result power reduces almost to a least value, by which the stress on the switches can be reduced .Full-bridge dc/dc converters have been widely used in medium to high power applications to further reduce the stress on switches for high power application TPTL was proposed. With three phase architecture the converter has the superior features including lower current rating of switches reducing input output current ripple allowing small size filter requirement. Although predominant characteristics exist in TPTL soft switching has not been achieved which limits the switching frequency and power loss.
The use of Asymmetrical duty cycle in the three phase three level dc/dc converter was proposed in order to achieve ZVS commutation over a wide load range.

II. PROPOSED TPTL DC/DC CONVERTER FOR DIFFERENT DUTY CYCLES

Fig. 1 shows the circuit configuration of TPTL converter in which, a three-phase transformer with Δ–Y connection is employed for the smaller turns ratios and transformer VA rating . As shown, L_{ra}, L_{rb} and L_{rc} are the additional resonant inductances to widen the ZVS commutation load range. L_{lka}, L_{lkb}, and L_{lkc} are the equivalent primary leakage inductances of each phase. D_{f1} and D_{f2} are freewheeling diodes. C_{ss} is the flying capacitor, which is in favor of decoupling the switching transition of Q_1,Q_3,Q_4, and Q_6 . D_{R1} – D_{R6} are rectifier diodes. The output filter is composed of L_f and C_f, and R_{Ld} is the load. Fig. 2 shows the control strategy of proposed converter. To realize the soft-switching for switches, the original interleaved switches should be designed in a complementary manner, and a short delay time *td* is necessary to be introduced between the two complementary switches to provide an interval for the ZVS commutation, which is similar to the control strategy of asymmetrical half-bridge converter .Accordingly, the duty cycles of Q_1,Q_3 , and Q_5 are served to regulate the output voltage, while the drive signals of Q_4,Q_6 , and Q_2 are complementary to that of the Q_1,Q_3 , and Q_5 , respectively.

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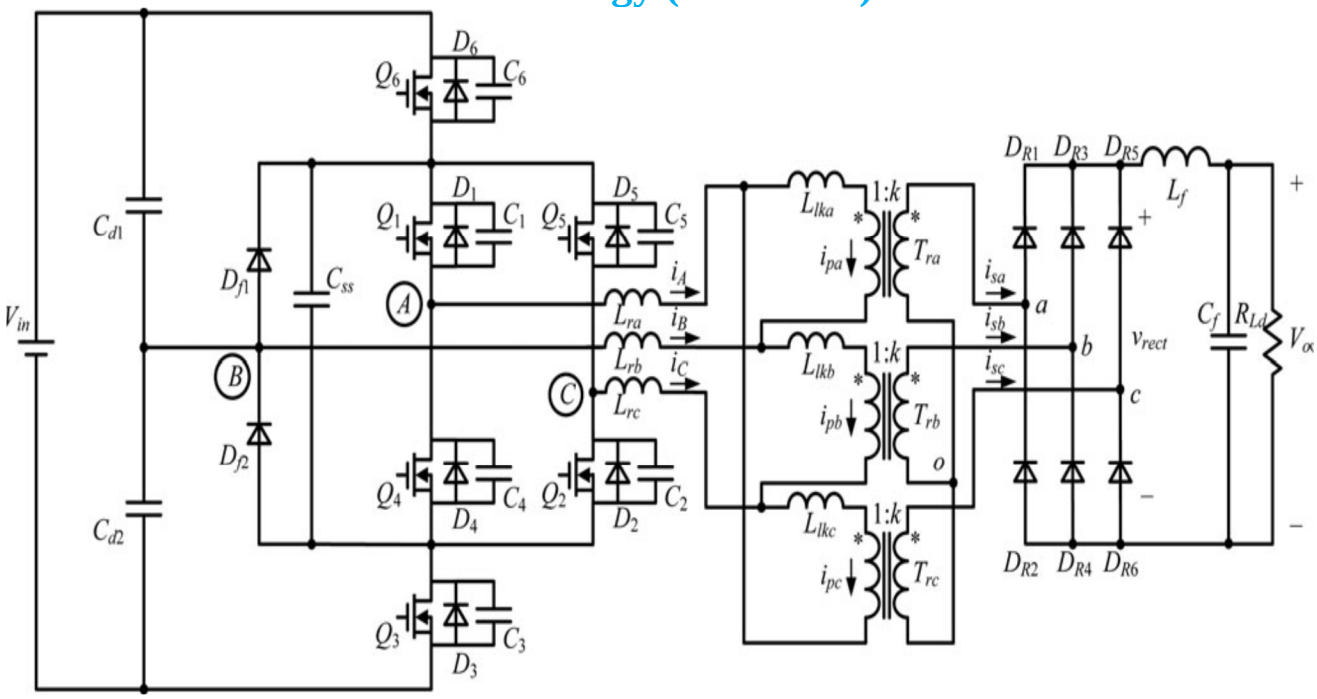

Fig. 1. Topology configuration of TPTL dc/dc converter.

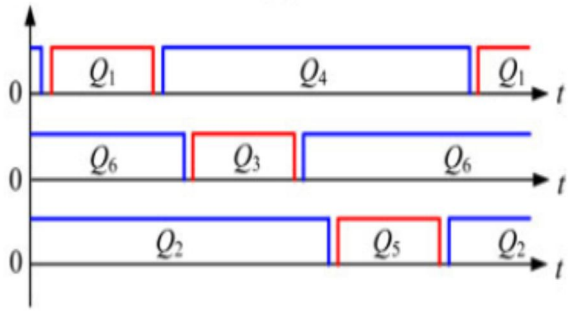

Fig. 2. Asymmetrical duty cycle control.

III. OPERATION OF PROPOSED TPTL CONVERTER

This section will analyze the operation principles of the TPTL converter under the modified control scheme. The following assumptions are made for the simplicity before the analysis:

1) all power devices and diodes are ideal;
2) all capacitors and inductances are ideal;
3) the output filter inductance is large enough to be treated as a constant current source during a switching period; its value equals to output current
4) the inductances of each phase are identical, i.e., L_{lka}=L_{lkb}= L_{lkc}= L_{lk}, L_{ra}= L_{rb}= L_{rc}= L_r;
5) C_1 = C_2 = C_3 = C_4 = C_5 = C_6 = C_p.

Fig. 3 shows the key waveforms of the TPTL converter with asymmetrical duty cycle control, as seen, the operation of the TPTL converter can be classified by different modes, according to the duty cycle range and the load current. The corresponding operation modes are defined as the small duty cycle mode (SDCM), and the large duty cycle mode (LDCM),respectively,

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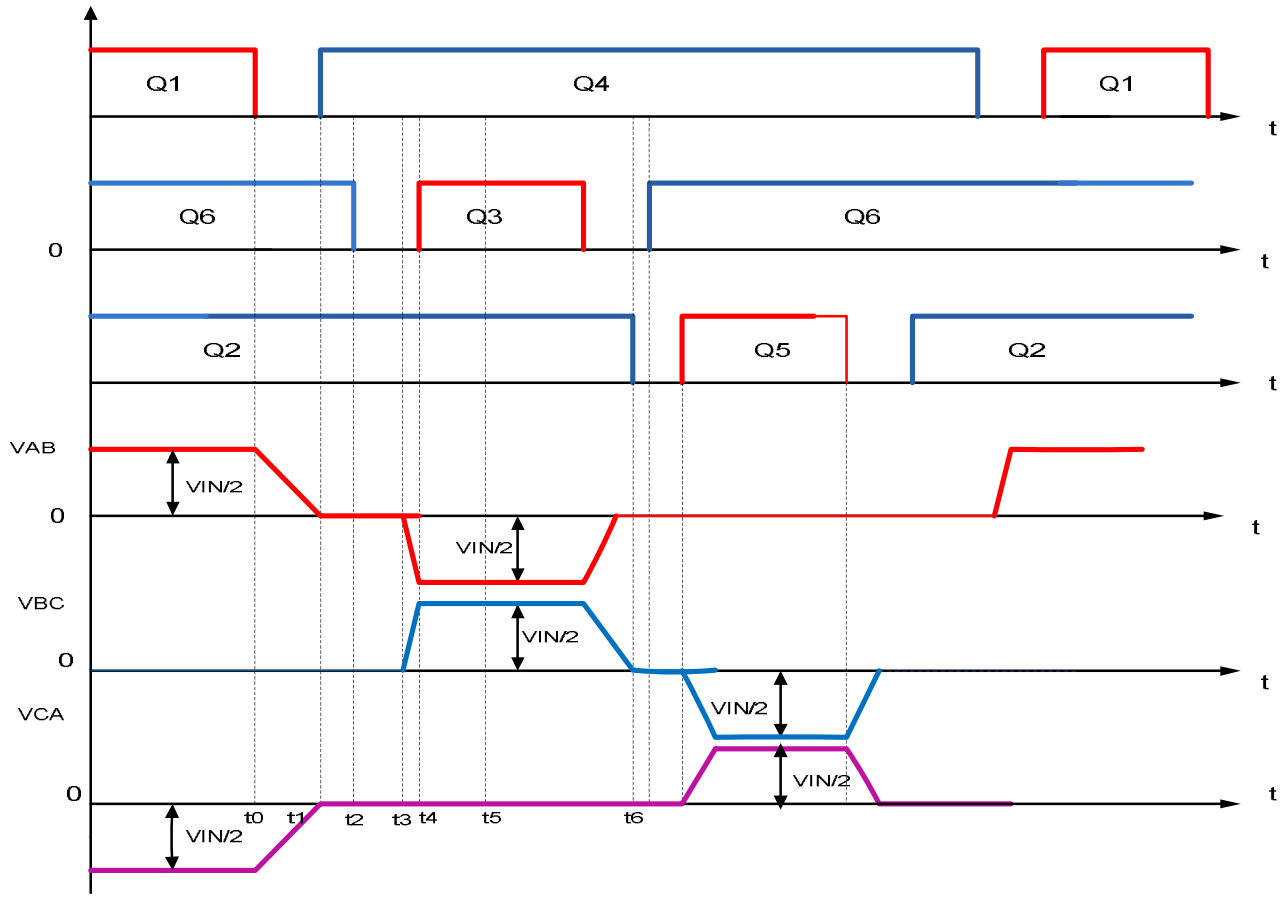

Fig. 3. Key waveforms of the TPTL converter with asymmetrical duty cycle control with SDCM.

The basic equations of the voltages and currents of the transformer are listed as follows:

$$V_{AB} + V_{BC} + V_{CA} = 0 \qquad (1)$$

$$i_{sa} + i_{sb} + i_{sc} = 0 \qquad (2)$$

$$\frac{dia}{dt} = k\frac{(disa)}{dt} = \frac{vLlka}{Llk}, \frac{dipb}{dt} = k\frac{(disb)}{(dt)}$$

$$= \frac{vLlkb}{Llk}, \frac{(dipc)}{dt} = k\frac{(disc)}{dt} = \frac{VLlkc}{Llk} \qquad (3)$$

Where k represents the secondary-to-primary turns ratios of the transformer. The voltage across the leakage inductance of transformer can be derived from (2) and (3) and is given as follows

$$V_{Llka} + V_{Llkb} + V_{Llkc} = 0. \qquad (4)$$

Stage1[0 − t_0]:

Fig.4(a) Shows Q_1,Q_2,Q_6,and D_{f2} are conducting at the primary side, and D_{R1} and $DR6$are conducting at the secondary side. $V_{AB}= V_{in}$ /2, $V_{BC}= 0$,and

$V_{CA}= -V_{in}$ /2. From (1), (2), (4), and other constraints between voltages and currents of transformers, the following expressions can be obtained.

$$Vpa = \frac{Vin}{2}, Vpb = 0, Vpc = -\frac{Vin}{2} \quad (5)$$

$$Vrect = Vsa - Vsc.k.Vin \quad (6)$$

Where V_{pi} and V_{si} are the primary voltage and secondary voltage of transformers, *I* represents the subscripts *a*, *b*, and *c*.

Stage 2[$t_0 - t_1$]:

Fig.4 (b) Shows At t_0,$Q_1$is turned off, the line current i_A charges C_1 and discharges C_4 linearly, and the rectified voltage decreases. As C_1 limits the rising rate of the voltage across Q_1,$Q_1$is zero-voltage turn-off. The voltages across C_1 and C_4 are

$$Vc1(t) = \frac{1}{Cp}\, kIo(t - to) \quad (7)$$

$$Vc4(t) = \frac{Vin}{2} - (\frac{1}{cp} k.Io(t - to)) \quad (8)$$

At t_1, v_{C1} rises to $V_{IN/2}$, and V_{C4} decays to zero; therefore, D4 conducts naturally, and Vrect decreases to zero.

Stage 3[$t_1 - t_2$]:

Fig.4(c) Shows after C_1 is fully charged, the current flowing through C_1 transfers to C_{ss} and begins to charge *Css*. The voltage across C_{ss} will increase and block D_{f2} to be off. During this stage, V_{AB}= V_{BC}= V_{CA}= 0. D_4 conduct sand clamps the voltage across Q_4 at zero, so Q_4 can be turned on at zero-voltage condition. D_{R1} and D_{R6} conduct, and V_{rect} is still zero.

Stage 4[$t_2 - t_3$]:

Fig.4 (d) Shows At t_2, Q_6 is zero-voltage turned-off and V_{AB} increases reversely. If v_{pa} keeps constant, the polarity of the voltage applied on L_{lka} will be non associated with the current flowing through L_{lka}; as a result, i_{pa} will decrease and cannot provide the load current, then D_{R3} begins to conduct, and the current commutation between D_{R1} and D_{R3}occurs. In the primary stage, C_3 and C_6 resonate with the leakage inductances and the resonant inductances, and the following expressions will be obtained.

$$Vc3(t) = \frac{Vin}{2} - (\frac{1}{2} k.Io.Zr.\sin[\omega r(t - t2)]) \quad (9)$$

$$Vc6(t) = (\frac{1}{2}.k.Io.Zr.\sin[\omega r(t - t_2)] \quad (10)$$

$$i_{A(t)} = \frac{3}{2} k.Io + \frac{1}{2} k.Io\cos[\omega r(t - t2)] \quad (11)$$

$$i_{B(t)} = -k.Io\cos[\omega r(t - t2)] \quad (12)$$

$$i_{C(t)} = -\frac{3}{2} k.Io + \frac{1}{2} k.Io.\cos[\omega r(t - t2)] \quad (13)$$

During this stage, V_{rect} remains at zero. When V_{c3} decays to zero, D_3 conducts naturally.

Stage5[$t_3 - t_4$]:

Fig.4 (e) Shows As D_3 is conducting, the voltage across Q_3 is clamped at zero; therefore, Q_3 is turned on at zero-voltage condition. During this stage, Q_2, Q_3, and Q_4 conduct in the primary stage, V_{AB}= $-V_{in/2}$, V_{BC}= $V_{in/2}$, and V_{CA}= 0. D_{R1}, D_{R3}, and *DR*6 conduct in the secondary stage, and V_{rect}= 0. From (1), (2), (4), and other constraints between voltages and currents of transformers, the expressions of the phase currents are given in (14)–(16)

$$i_{pa(t)} = i_{pa(t3)} - \frac{Vin}{2Lp}.(t - t3) \quad (14)$$

$$i_{pb(t)} = i_{pb(t3)} + \frac{Vin}{2Lp}.(t - t3) \quad (15)$$

$$i_{pc(t)} = -kIo \quad (16)$$

Therefore, the line currents can be obtained from (14) to (16)

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$i_{A(t)} = i_{A(t3)} - \frac{Vin}{2Lp}.(t - t3)$ (17) $i_{B(t)} = i_{B(t3)} + \frac{Vin}{Lp}.(t - t3)$ (18) $i_{c(t)} = i_{C(t3)} - \frac{Vin}{2Lp}.(t - t3)$ (19)

At the secondary stage, I_{sa} flows through D_{R1} and decreases with *ipa* from (14). When *Isa* decreases to zero, D_{R1} turns off and D_{R2} conducts. It should be noted that the rectified voltage is lost during the interval t_{34}, compared with the primary line voltage. Therefore, the duty cycle loss in SDCM is defined as

$$Dloss1 = \frac{t34}{\frac{Ts}{3}} = \frac{6k.Io.Lp}{Vin.Ts} \quad (20)$$

Where *Ts* is the switching period.

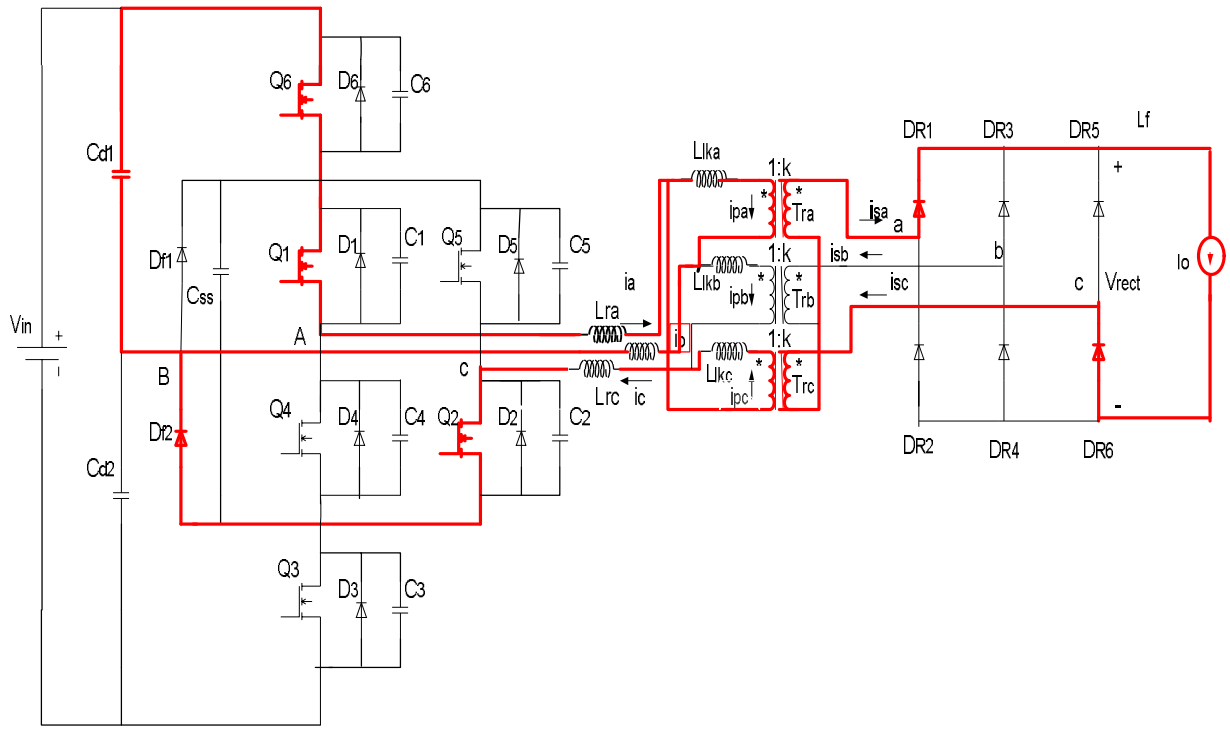
Stage 6 [$t_4 - t_5$]:

Fig.4 (f) Shows During this stage, $V_{AB}=-V_{in/2}$, $V_{BC}= V_{in/2}$, $V_{CA}= 0$.
I_{sc} flows through D_{R6}, i_{sc} and decreases with $i_{pc.}$ When i_{sc} decreases to zero, D_{R6} turns off, the primary and secondary currents of transformer T_{rc} are both zero. The time interval of this stage is given by

$$t45 = \frac{4k.Io.Lp}{Vin} \quad (21)$$

Stage 7[$t_5 - t_6$]:

Fig.4 (f) ShowsQ_2, Q_3, and Q_4 conduct at the primary side, while D_{R2} and D_{R3} conduct at the secondary side, and the rectified voltage is kV_{in}, whichissimilartothestage1.



4. (a)

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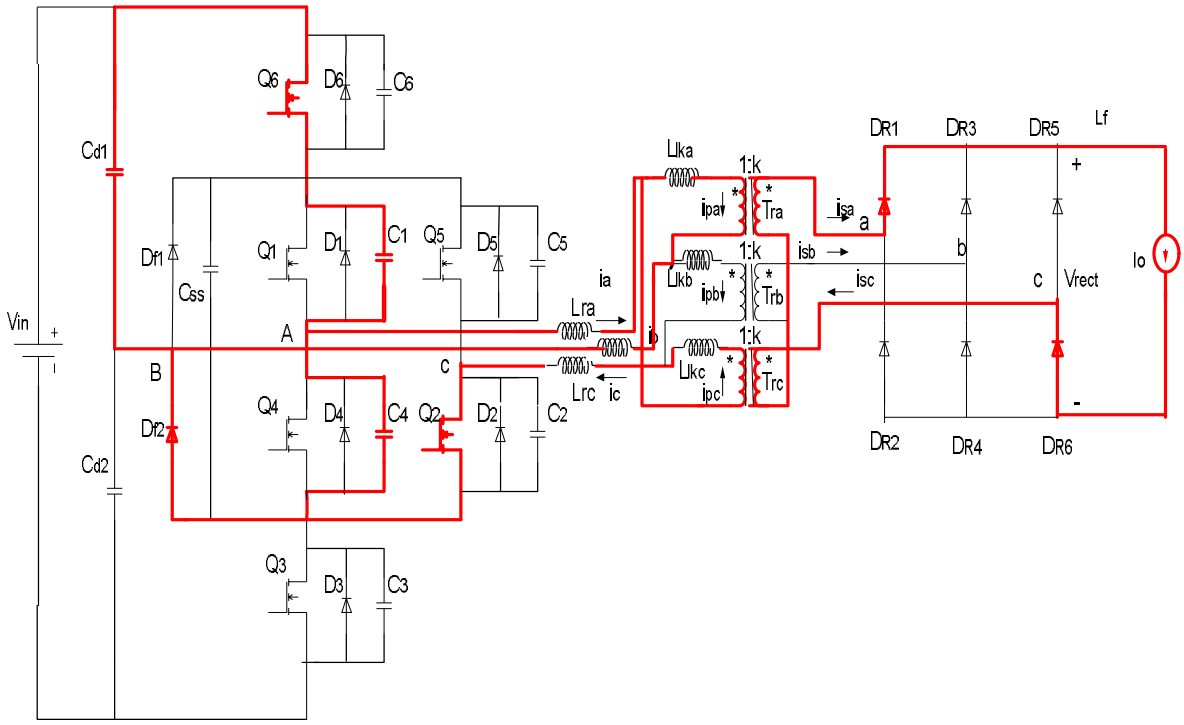
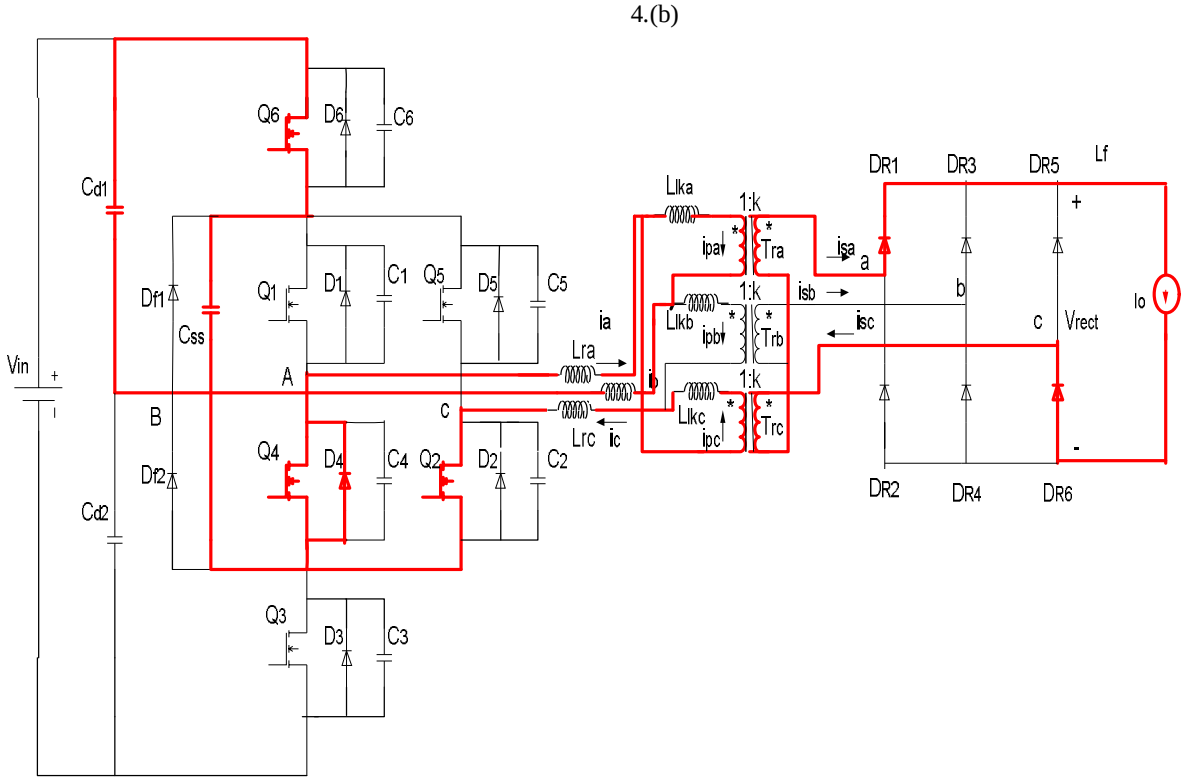


4.(b)



4.(c)

Fig. 4. Equivalent circuits under different operation stages. (a) Prior to[0 t_0] . (b) [t_0 , t_1]. (c) [t_1 , t_2]

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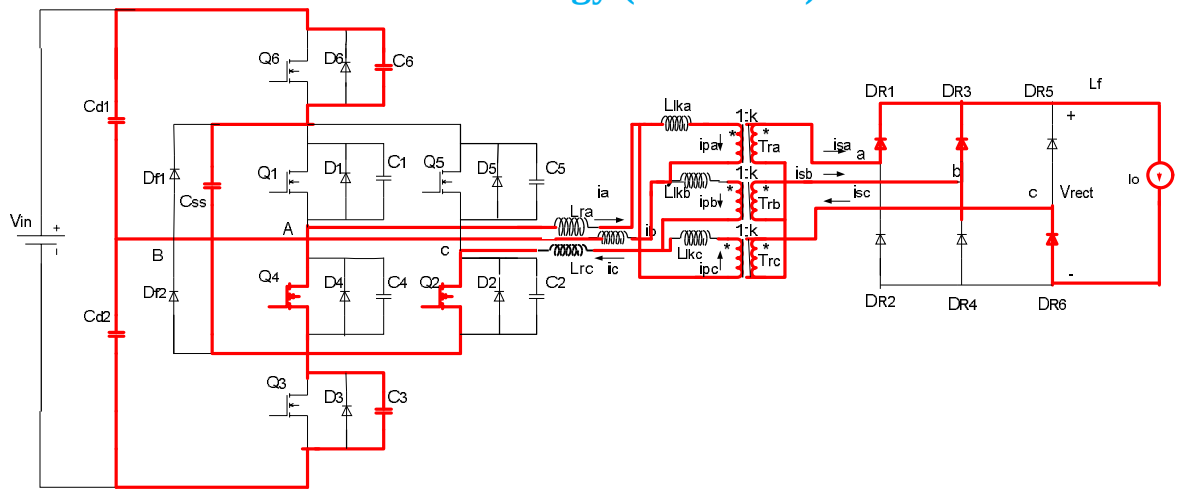
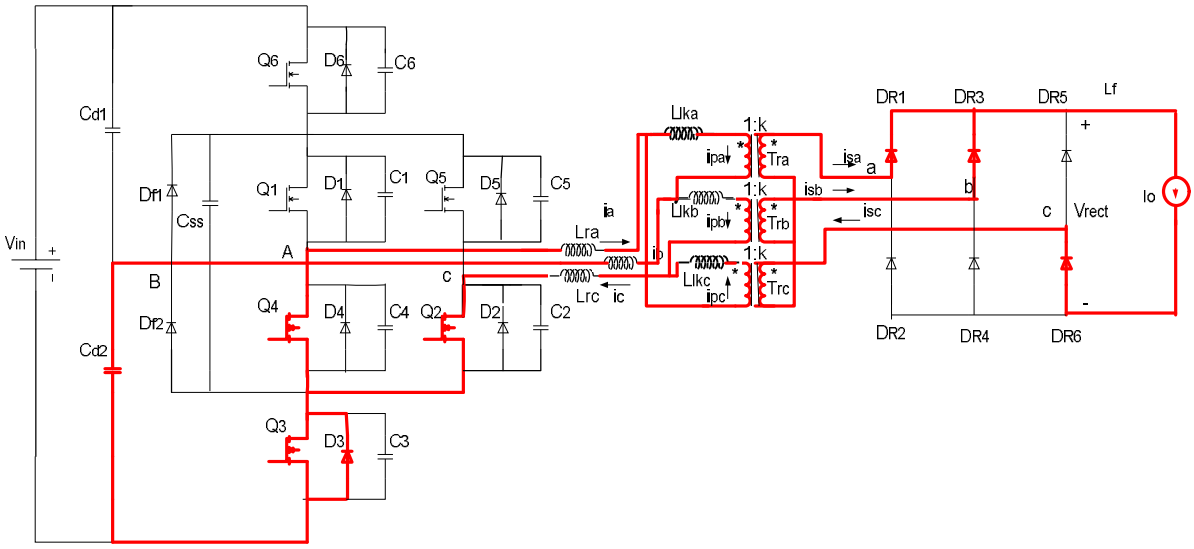
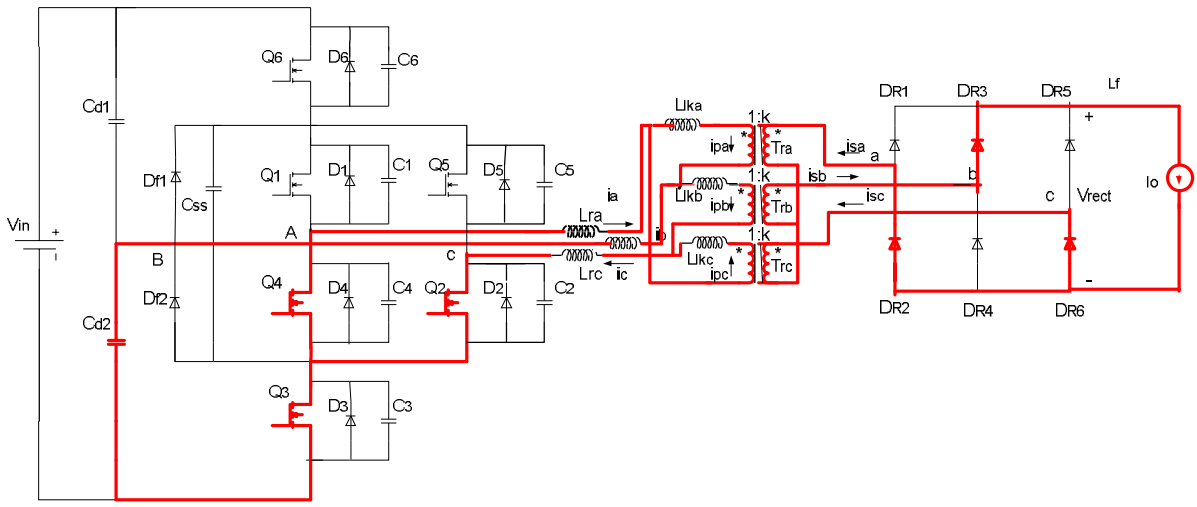


4.(d)



4.(e)



4.(f)

Fig. 4. Equivalent circuits under different operation stages (d) [t_2 , t_3]. (e) [t_3 , t_4]. (f) [t_4 , t_5].

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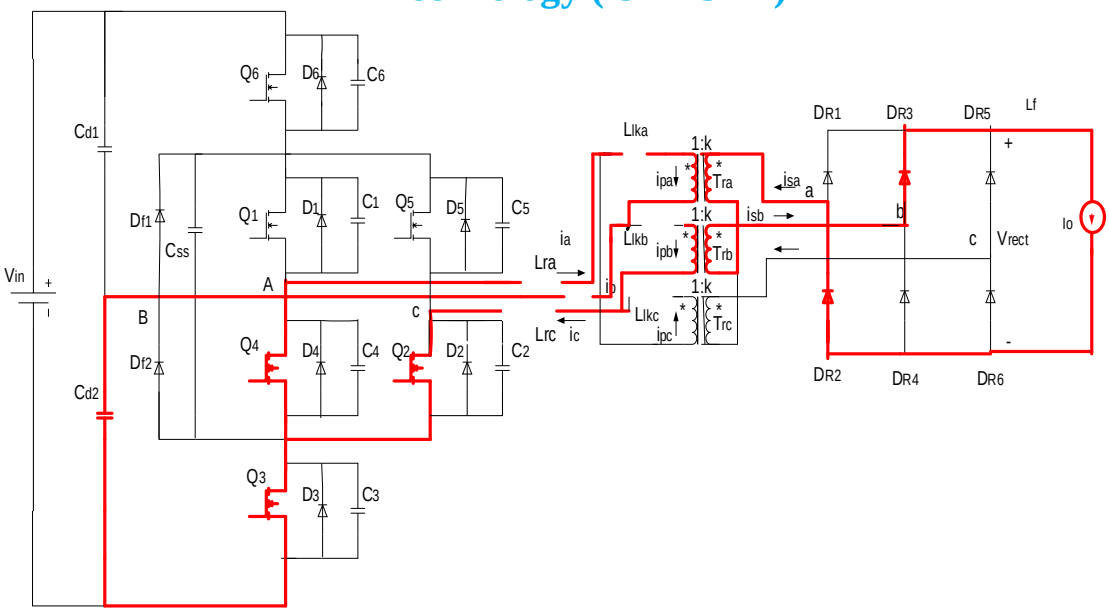

Fig. 4.

Equivalent circuits under different operation stages(g) [t_5 , t_6].

IV. SIMULATION RESULTS FOR THREE PHASE THREE LEVEL DC/DC CONVERTER

In fig.5 Simulink model of a 200V/16V DC-DC converter has been proposed .In fig.6.output waveforms of the proposed converter is shown. In the proposed converter there is total six switches out of it Q_1,Q_3,Q_5 are given with same duty cycle and Q_2,Q_4,Q_6 are same having same duty cycle. Though the switches have same duty cycle all the switches not on for the same time In the proposed converter there are total six switches in which all are under goes soft switching for different duty cycles Fig.7 & Fig.8 shows the simulation results for D=20%.

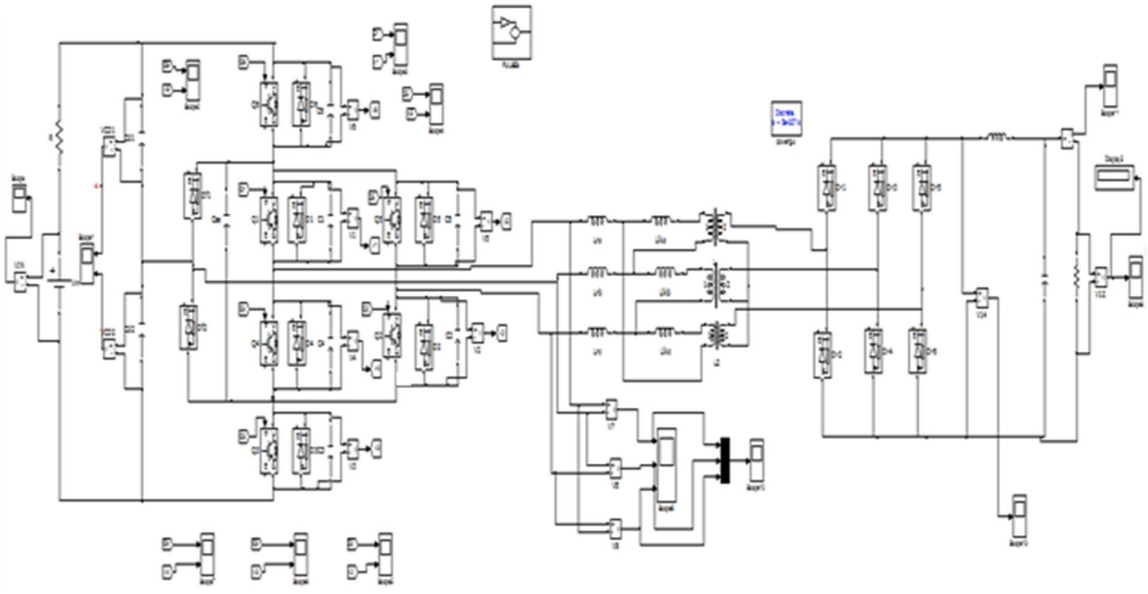

Fig.5.Simulink diagram of Three phase Three-Level DC-DC converter.

As the duty cycle increases the output voltage will increases is shown in Table 1 . In which the output voltage will increases form D=20% to 46% and efficiency also increases.Fig6 represents output waveforms of the converter and three phase output voltage also observed in which all the phases are shifted by 120° .Fig7 represents soft switching of the proposed converter for Q_1 and Q_4 switches .Which is also same for Q_2,Q_3,Q_5,Q_6.Fig.7a shows voltage across Q_1,fig 7b.shows the ZVS for Q_1 from off to on &fig7c shows on to off of Q_1 under the ZVS .Fig 8a. shows voltage across Q_4,fig 8b.shows the ZVS for Q_4 from off to on

&fig 8c.shows on to off of Q_4 under the ZVS.Fig9 shows graph between efficiency and load current at duty cycle D=20%,which will also represents the efficiency is high for with soft switching than without soft switching.

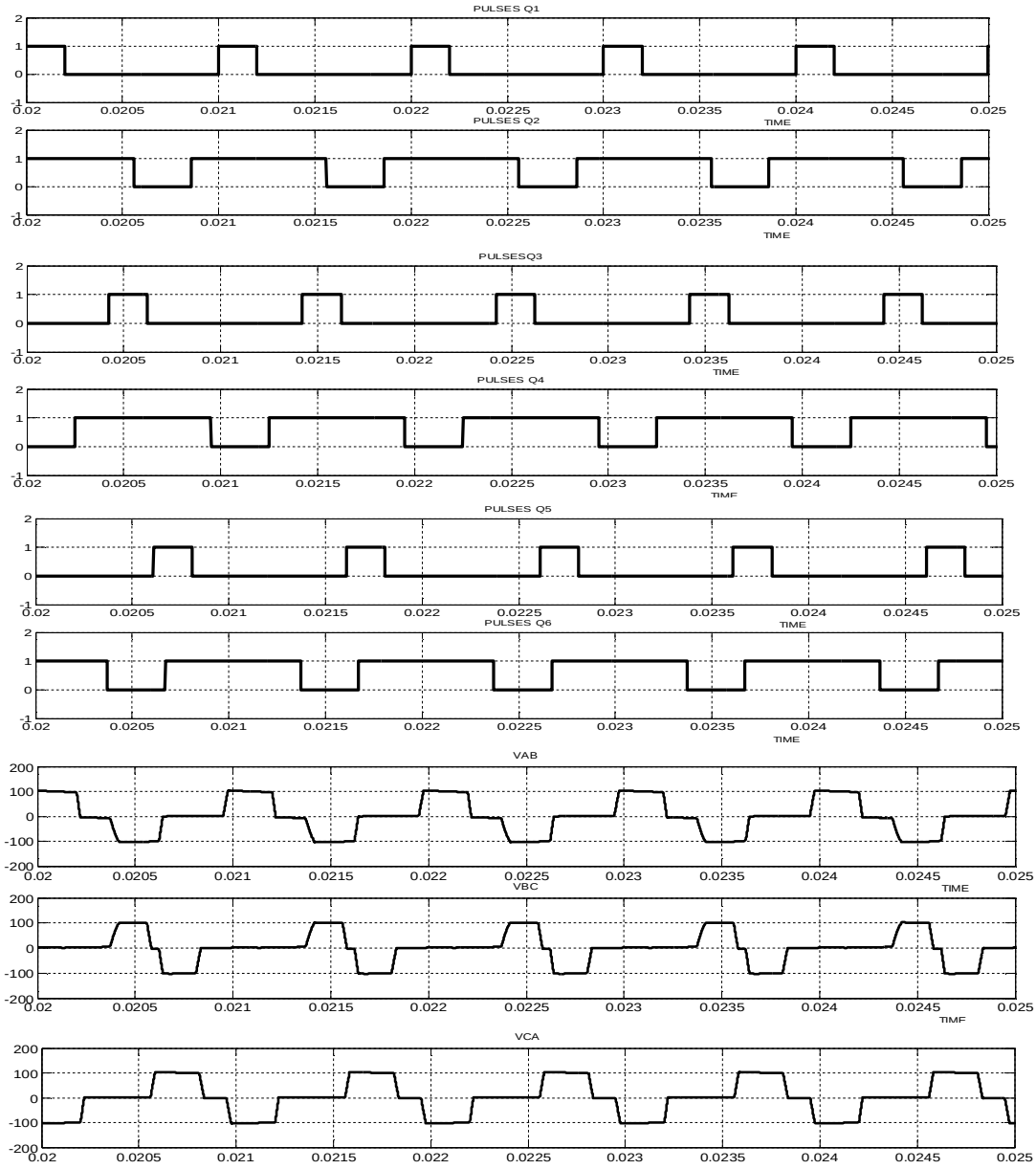

Fig 6 output waveform

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Simulation results for Duty cycle 20%

Voltage across Q_1

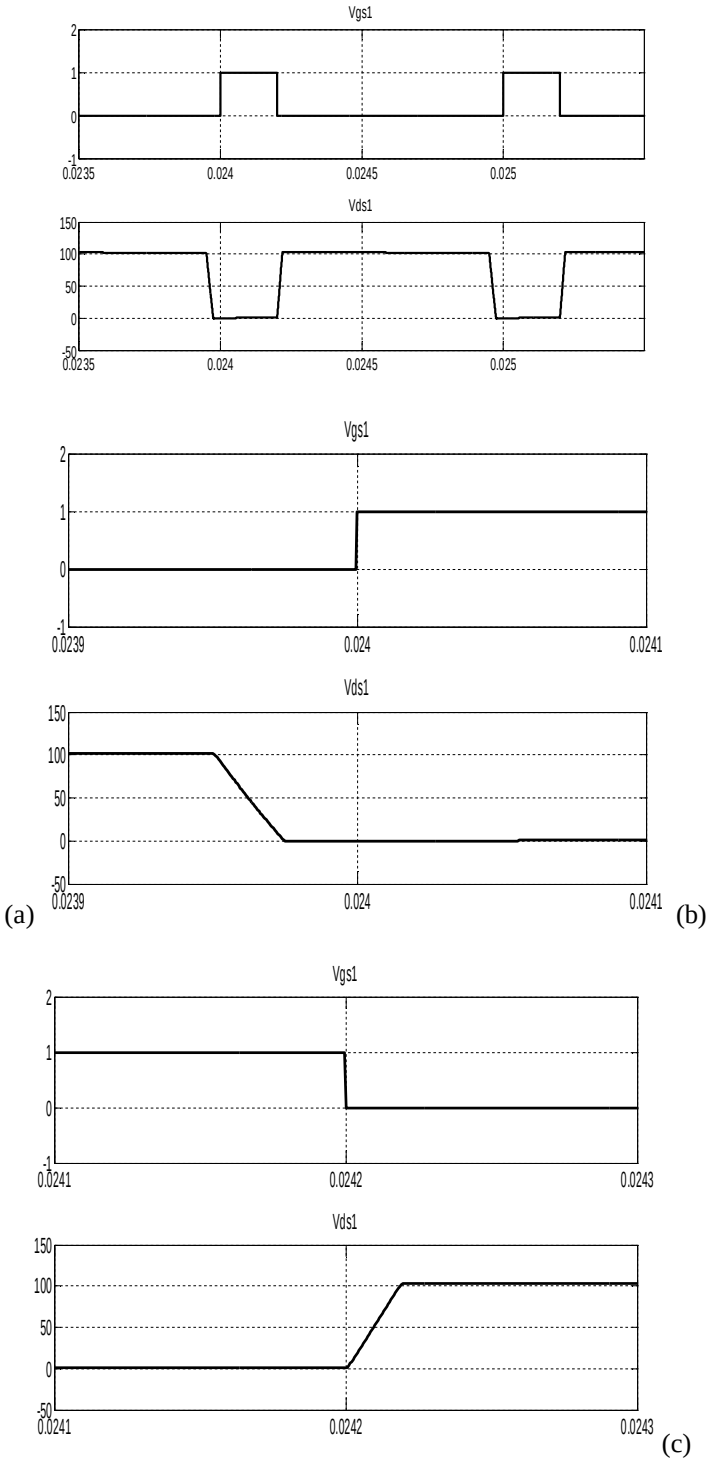

Fig.7 for 20% duty cycle(a) voltage across switch Q_1, (b). zvs turn off-on Q_1(c). zvs turn on-off Q_1.

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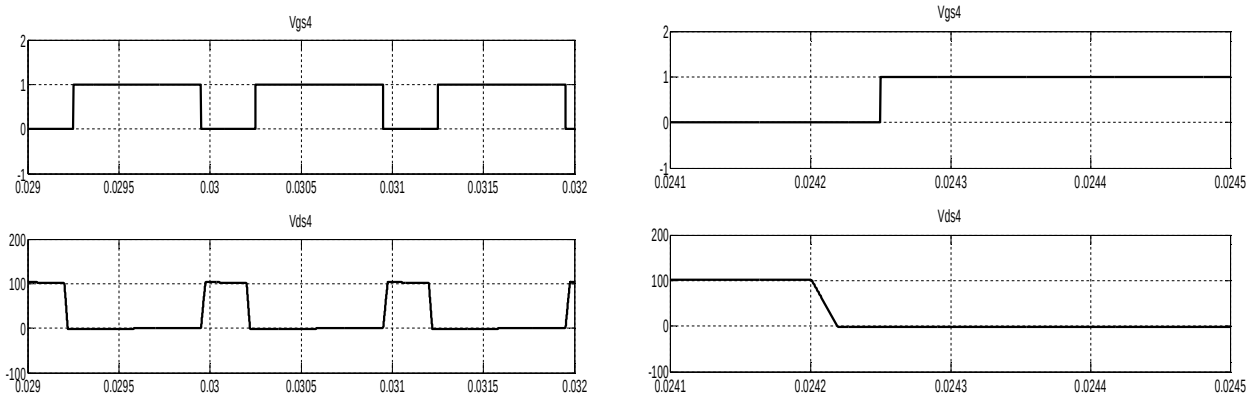
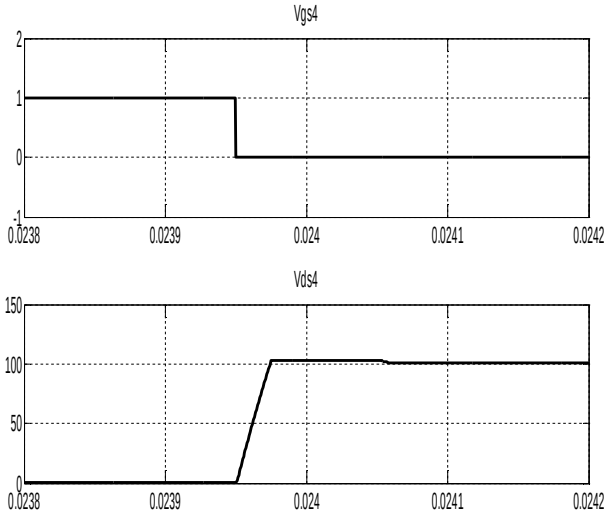


(a)



(b)

(c)

Fig.8 for 20% duty cycle(a) voltage across switch Q_4, (b). zvs turn off-on Q_4(c). zvs turn on-off Q_4.

TABLE1

Duty cycle (%)	Output voltage (V)	Efficiency with soft switching (%)	Efficiency with out soft switching (%)
15	6.56	51.78	38.29
20	11.7	64.67	44.1
30	13.95	69.81	50.36
40	15.33	71.45	54
48	15.8	81.87	57.77

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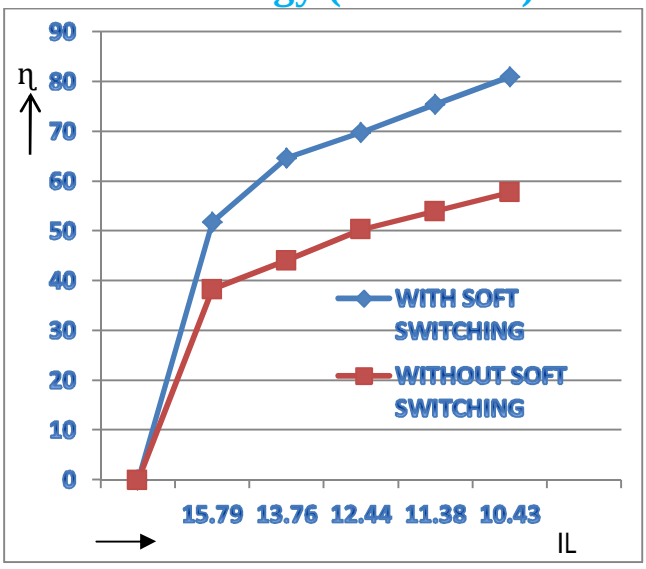

Fig.9 Load current Vs Efficiency at D=20%

V. CONCLUSION

Soft switching scheme is achieved in each and every switch. Voltage stress across each switch was reduced. By increasing the voltage levels the size of the filter elements may also reduced. The switching losses in the proposed converter are reduced. The proposed control scheme features the following characteristics:

A. Compared with the hard switching technique the losses in switches predominately reduced

B. The input capacitors can realize automatic and inherent voltage balancing, which ensures that all the switches sustain only one-half of the input voltage.

C. The TPTL converter will operate in different duty cycles.

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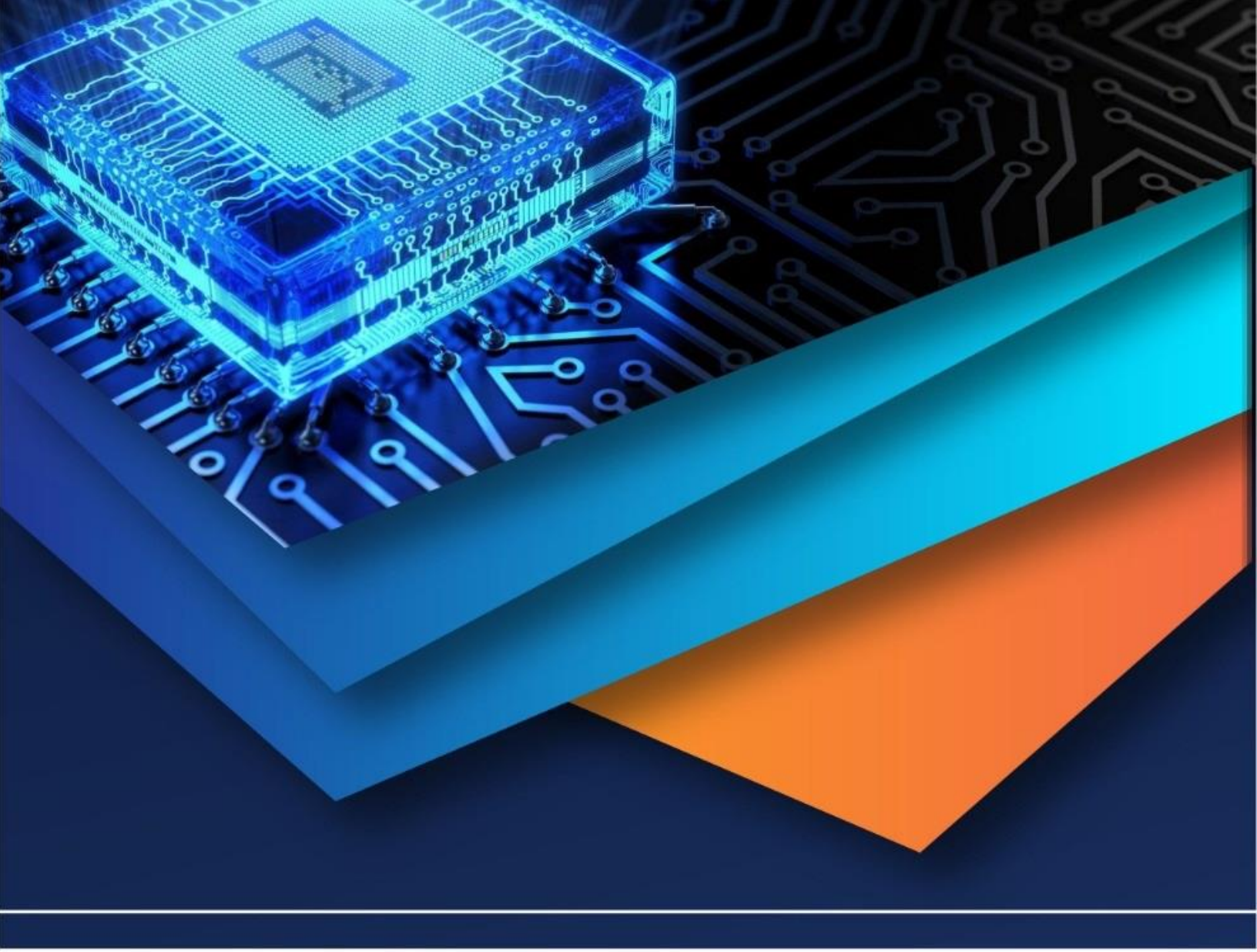

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