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Implementation of Inter-Integrated Circuit (I2C) Multiple Bus Controller on FPGA using VHDL

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***Abstract:** The Inter - Integrated Circuit bus commonly called as I2C (I squared C) or I2C bus is a serial bus invented by Philips Semiconductors during early 80's for interconnecting integrated circuits. In this paper, the design and implementation of a I2C Multiple Bus Controller (IICMB) core is presented.*
***Keywords:** I2CMB, I2C Protocol, Avalon Memory mapped Interfaces, I2C Communication (key words)*

I. INTRODUCTION

I2C bus was developed by Philips Semiconductors during 1980's for connecting computer peripherals together using a common protocol .This specification defines the architecture, hardware interface and parameterization options for the I2C Multiple Bus Controller (IICMB) core.

The IICMB core provides a low-speed, two-wire, bidirectionall serial bus interfaces compliant to industry standard I2C protocol. The key feature of the core is its ability to control several connected I2C buses effectively reducing complexity of system.

At any given moment the IICMB core works with a single I2C bus chosen from the range of connected buses (throughout this document such bus is called *selected bus*). When work with a particular selected bus is finished, user can switch to another one to continue configuring other peripherals. Every connected I2C bus is recognized by its number, or *bus ID*.

Note: The current version of the core supports master only functionality. Slave mode is under development.

Proposed Features

1) Compatible with Philips I2C standard
2) Works with up to 16 distinct I2C buses
3) Statically configurable system bus clock frequency
4) Statically configurable desired clock frequencies of I2C buses
5) Multi-master clock synchronization
6) Multi-master arbitration
7) Clock stretching
8) Digital filtering of SCL and SDA inputs
9) Standard (up to 100 kHz) and Fast (up to 400 kHz) mode operation
10) Connects as 8-bit slave on Wishbone bus
11) Connects as 32-bit slave on Avalon-MM bus

A. Architecture

The core is provided with three examples of its top level (iicmb_m_wb.vhd, iicmb_m_av.vhd and iic_m_sq.vhd). Two of them are designed for Wishbone and Avalon-MM buses, while third version is a sequencer based one for deeply embedded applications without any system bus at all.

In the center of the IICMB core is iicmb_m.vhd module which integrates byte- and bit level master mode FSMs together with I2C bus multiplexer functionality. It is controlled with byte-level commands sent through the so-called Generic Interface.

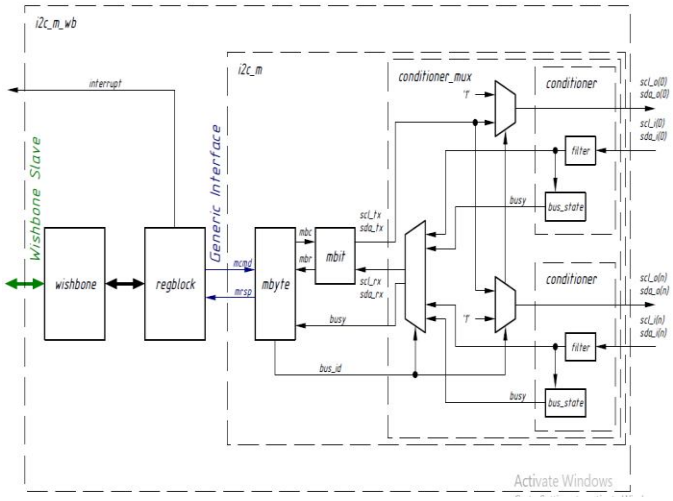


Fig. Block diagram of the Wishbone version of the top level

The wishbone.vhd module connects Wishbone bus to register block (regblock.vhd), which converts system bus accesses to byte-level commands of the Generic Interface. SCL and SDA inputs are digitally filtered to suppress unwanted spikes and to cope with long rising time of the I2C bus signals. The bus_state.vhd modules independently monitor busy states of all connected buses.

The conditioner_mux.vhd module, controlled by bus_id input, performs switching between connected I2C buses. The mbit.vhd and mbyte.vhd implement bit-level and byte-level FSMs, generating appropriate SCL and SDA waveforms in accordance to I2C Bus Specification

B. Operation

Some of the basic features on which have been implemented are as follows.

1) Implementation of IICMB core which provides low-speed, two-wire, bidirectional serial bus interfaces compliant to industry standard I2C protocol.

2) "Manchester encoded UART" which enables running small peripherals with parasitic power derived from the TXD line, and allowing large clock differences typical of RC oscillators.

3) The key feature of the core is its ability to effectively reducing complexity of the system and control several connected I2C buses.

Signal Name	I/O	Description
Clk	Input	Avalon-MM clock. Main clock for the controller
s_rst	Input	Synchronous reset. Active high.
waitrequest	Output	Wait request.
readdata[31:0]	Output	Data output.
readdatavalid	Output	Data validity indication.
writedata[31:0]	Input	Data input.
Write	Input	Indicates a write transfer.
Read	Input	Indicates a read transfer.
byteenable[3:0]	Input	Enables specific byte lane(s) during

Keeping in mind all the above specifications the key features of our design are

4) Works with up to 16 distinct I2C buses

5) Statically configurable system bus clock frequency

6) Statically configurable desired clock frequencies of I2C buses

7) Multi-master clock synchronization

8) Multi-master arbitration
9) Clock stretching
10) Digital filtering of SCL and SDA inputs
11) Standard (up to 100 kHz) and Fast (up to 400 kHz) mode operation
12) Example connection as 32-bit slave on Avalon-MM bus

C. Byte-level FSM

The byte-level FSM module (mbyte.vhd) communicates with upper level through so called Generic Interface. It accepts several byte-level commands listed in the Table 1 below.

After completion, each command is answered with an appropriate response. The main responsibility of the mbyte.vhd module is to translate byte-level commands to one or more commands for bit-level FSM (mbit.vhd).

Reception of a response is a mark of completion of the previously issued command. It is an error to send next command before previous command is responded. Such a command is ignored.

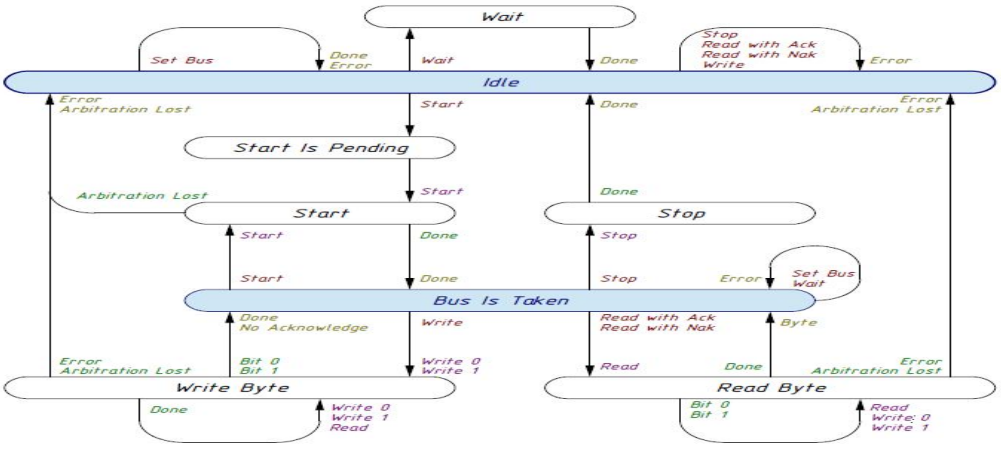
Command	Code	Parameter	Description
Start	"100"	–	If bus is not captured yet: issue Start Condition and capture selected bus. If bus captured: issue Repeated Start Condition.
Stop	"101"	–	Issue Stop Condition and free selected bus.
Read With Ack	"010"	–	Receive a byte with acknowledge.
Read With Nak	"011"	–	Receive a byte with not- acknowledge.
Write	"001"	Byte of data	Transmit the byte given as a parameter.
Set Bus	"110"	Bus number (ID)	Connect to the specified bus (select bus).
Wait	"000"	Milliseconds	Do nothing for specified amount of time.

Byte-level commands

Response	Code	Parameter	Description
Done	"000"	–	Command completed.
Arbitration Lost	"010"	–	Arbitration lost. Selected bus is freed, FSMs are set to their idle states.
No Acknowledge	"001"	–	Byte written got no acknowledge.
Byte	"100"	Byte of data	Byte of data received.
Error	"011"	–	Something went wrong.

Byte-level responses

The following diagram depicts the byte-level FSM

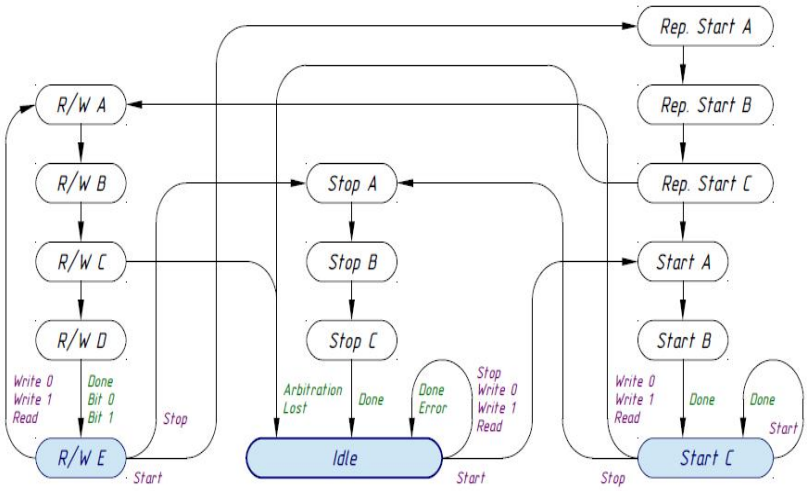


Byte-level FSM

D. Bit-level FSM

Bit-level commands and responses are hidden from the user of the core, but listed here for better understanding of how the two FSMs interact with each other.

Bit-level commands and responses have no parameters.



Level FSM

II. IMPLEMENTATION RESULTS

A. Setup 1

Top level module: iicmb_m_wb.vhd. Number of I2C buses (g_num_bus) = 1. System clock frequency (g_f_clk) = 100 MHz. I2C bus clock frequency (g_f_scl_0) = 100 kHz.

Device Utilization Summary

Family	Device	Fmax	Registe	Logics
Virtex-6	xc6vcx75t-2-ff484	290MHz	649	757

B. Setup 2

Top level module: iicmb_m_wb.vhd. Number of I2C buses (g_num_bus) = 16. System clock frequency (g_f_clk) = 100 MHz. I2C bus clock frequencies: g_f_scl_0 = 100 kHz, g_f_scl_1 = 120 kHz, g_f_scl_2 = 130 kHz, g_f_scl_3 = 200 kHz, g_f_scl_4 = 50 kHz, others = 30 kHz.

Family	Device	Fmax	Registe	Logics
Virtex-6	xc6vcx75t- 2-ff484	325MHz	154	264LUT

III. HIERARCHY OF MODULES

Hierarchy of modules with Avalon-MM top level

A. iicmb_pkg.vhd

B. iicmb_int_pkg.vhd

C. iicmb_m_av.vhd

1) avalon_mm.vhd

2) regblock.vhd

3) iicmb_m.vhd

a) mbyte.vhd

b) mbit.vhd

c) conditioner_mux.vhd

d) conditioner.vhd

i) filter.vhd

ii) bus_state.vhd

Device Utilization Summary

Slice Logic Utilization	Used	Available	Utilization
Number of Slice Registers	182	12,480	1%
Number used as Flip Flops	182		
Number of Slice LUTs	318	12,480	2%
Number used as logic	307	12,480	2%
Number using O6 output only	280		
Number using O5 output only	7		
Number using O5 and O6	20		
Number used as exclusive route-thru	11		
Number of route-thrus	18		
Number using O6 output only	17		
Number using O5 and O6	1		
Number of occupied Slices	147	3,120	4%
Number of LUT Flip Flop pairs used	375		
Number with an unused Flip Flop	193	375	51%
Number with an unused LUT	57	375	15%
Number of fully used LUT-FF pairs	125	375	33%
Number of unique control sets	15		
Number of slice register sites lost	22	12,480	1%
to control set restrictions			
Number of bonded IOBs	59	172	34%
IOB Flip Flops	1		
Number of BUFG/BUFGCTRLs	1	32	3%
Number used as BUFGs	1		
Average Fanout of Non-Clock Nets	4.36		

IV. CONCLUSION

In this project work, the multi-master facility of I2C protocol is implemented successfully. Address resolution is the major concern while using multiple masters in I2C bus. Arbitration procedure must be perfect for the bus to work properly when dual masters are present. A dual master I2C bus controller system with an EEPROM 24CXX series as the slave devices has been developed for realizing both the read and write cycles of the I2C bus and tested. The design has got successfully implemented in Spartan 3A FPGA and the outputs are verified. Also DS1307 RTC is connected as the slave device and performed the WRITE and READ operations following I2C protocol. This design can be used in systems where multiple devices needs to be interconnected by ensuring with low complexity and efficient resource utilization.

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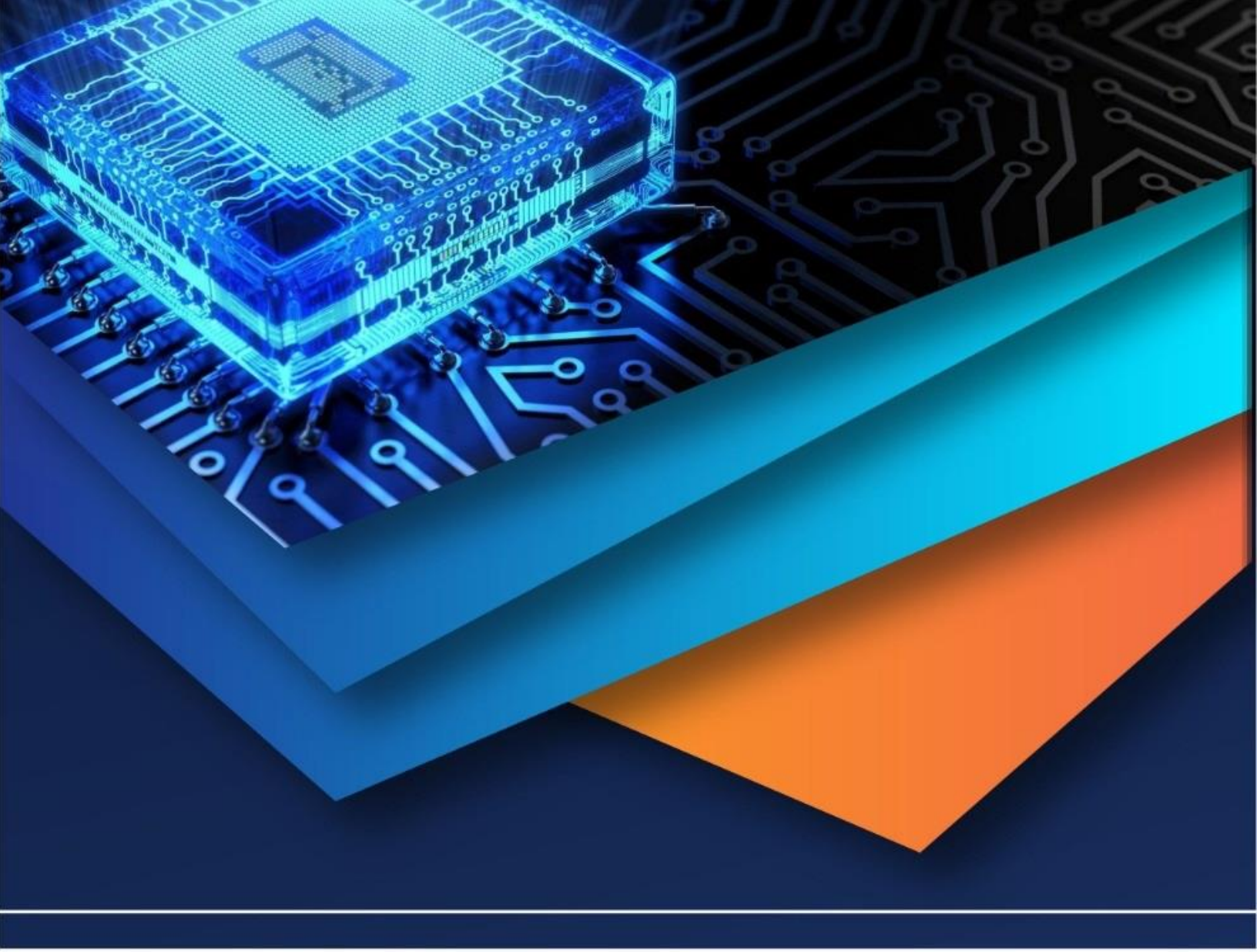

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