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Design and Analysis of MCML Carry Circuit with and without Sleep Transistor for Compressor Circuit Applications

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Abstract: ***The general CMOS logic circuit dissipates the power only when the load is charging and discharging. So, the consumption of the power in the CMOS logic circuit is generally small at low frequency. However, when the charging and the discharging time is decreased by the increasing of the operation frequency. When frequency is increases the of the power in the CMOS logic circuit also increases accordingly that contribute the incorrect output. This problem can be solved by MOS current mode logic (MCML). Due to small input capacitance and signal amplitude MCML is faster than the CMOS logic. The MCML operates the static current source. This does not cause the power consumption to increase with the operation frequency. In this paper we have designed 03 input carry circuits with and without concept of sleep transistor. Designed circuit find the application in compressor circuits.***

I. INTRODUCTION

Current Mode Logic (MCML) circuit provide digital circuit design with reducing power consumption analog friendly environment in VLSI world. While bipolar Current Mode Logic, is a modified version of emitter coupled logic (ECL), it has also used from many years in high performance VLSI applications. But is less desirable over time due to its high static power consumption and required bipolar processing.

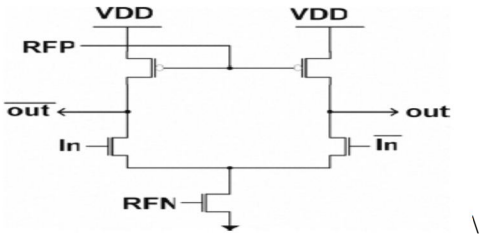

Figure1 A basic MCML inverter [3]

Figure 1 shows a basic MCML inverter. This inverter has two control voltages RFN and RFP. The RFN known as reference, determines the current value of entire circuit by using the controlled voltage at the gate. Generally, we use NMOS transistor to operate current source, the current source is larger than the minimum length of fabrication. The RFP and the gate input voltage of PMOS transistor is determines the turn-on resistance value when PMOS transistor is on these voltages also provides biasing so that RPF is chosen so that PMOS works in triode region and RFN is chosen so that NMOS works in saturation region[3]. In this paper we have designed MCML carry circuit with and without concept of sleep transistor. Which is finding the application in compressor circuit that has advantage over CMOS based circuit.

These implementations have been compared with compressor architectures those make use exclusively of three-level MCML gates. This investigation has shown that the compressors that use exclusively three input MCML gates outperform the other implementations in terms of speed, power consumption and silicon area. Another result is that the order in which the signals are connected to the gate inputs may greatly affects compressor performance [4].

MCML technology has two operating modes, one is active mode and other is sleep mode. The proposed technology has a sleep-transistor which is inserted in series with the supply voltage *(V_{DD})* of the circuit. The sleep-transistor is connected to the V_{DD} in the active mode to execute the normal operation. In the sleep mode, the sleep-transistor is isolated from the V_{DD} to reduce the power consumption. The sleep-transistor is implemented with a high-threshold voltage PMOS transistor to minimize the leakage current [3].

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II. CONCEPT OF SLEEP TRANSISTORS

A sleep-transistor which is inserted in series with the supply voltage *(V_{DD})* of the circuit. In the active mode, the sleep-transistor is connected to the V_{DD} to execute the normal operation. In the sleep mode, the sleep-transistor is isolated from the V_{DD} to reduce the power consumption. The sleep transistor is implemented with a high-threshold voltage PMOS transistor to minimize the leakage current.

III. SLEEP TRANSISTOR'S IMPLEMENTATION METHOD

There are a number of implementation methods of sleep transistors:

A. Fine grain and coarse grain sleep transistor implementations.
B. Header and footer switch implementation.
C. Grid and ring style sleep transistor implementation.

The sleep transistors can be implemented in a design in either "coarse-grain" or "fine-grain" power gating styles. In the "fine-grain" implementation, the sleep transistor is inserted in every standard cell which is often called MTCMOS cell. A power gating control signal is added to switch on and off power supply to the cell. An example of "Fine-grain" NAND gate is shown in figure 2.

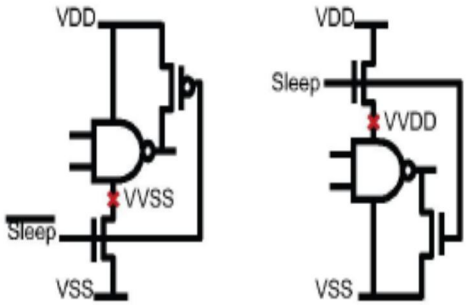


Fig 2: Header and Footer fine-grain sleep transistor implementation using NAND gate [10].

The advantage of the fine grain sleep transistor is implemented in the virtual power nets (VVSS or VVDD) and short and hidden by the cell. Furthermore, the MTCMOS cell can be designed by existing standard cell based on synthesis and place and route tools. However the fine- grain sleep transistor are implemented to a sleep transistor for every MTCMOS cell circuit that the result area is increased. Kindly note that it is not able to use the normal standard cells provided by different library vendors and ASIC foundries. Another issue is associated. Since PVT variation included to MTCMOS, which result produce IR-drop variation in the cell and hence performance variation also included.
In the "coarse-grain" power gating designs as shown in fig.3, the sleep transistors are connected together between the permanent power supply and the virtual power supply networks.[15]

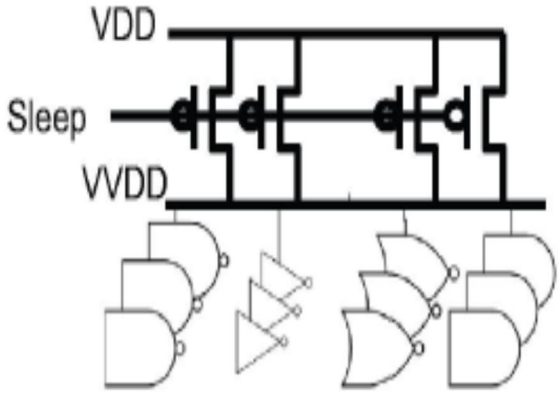


Fig 3: Header coarse-grain sleep transistor implementations [10].

IV. CIRCUIT IMPLEMENTATION

In this section we have designed schematic we have designed schematic of MCML inverter and 03 input carry circuit with and without concept with their input parameter and find the outputs for the same.

A. Schematic Of MCML Inverter With Following Input Parameter

1) L_N = 16nm
2) W_N = 40nm
3) L_P = 16nm
4) W_P = 120nm
5) Pulse= 0 to 1v
6) Rise time= 1ns
7) Fall time = 1ns
8) Width a,b = 10ns,20ns
9) period a,b = 20ns,40ns

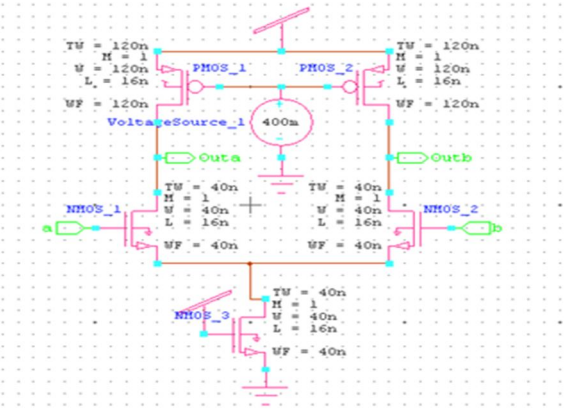


Fig 4: Schematic of MCML three input Carry circuit without sleep transistor

B. Input Parameters

1) L_N = 16nm
2) W_N = 40nm
3) L_P = 16nm
4) W_P = 120nm
5) Pulse= 0 to 1v
6) Rise time= 1ns
7) Fall time = 1ns
8) Width X1, X2 & X3=10ns, 20ns, 20ns
9) Period X1, X2 & X3=30ns, 40ns, 40ns

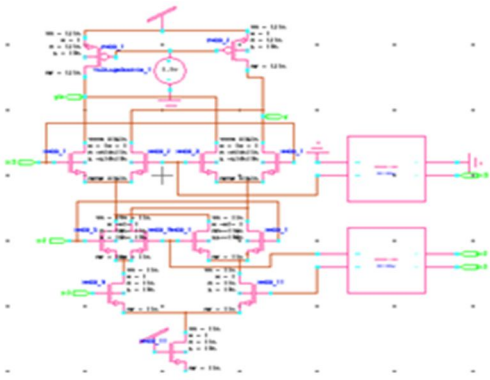


Fig.5: Schematic of MCML three input Carry circuit with sleep transistor

Input parameters

L_N = 16nm

W_N = 40nm

L_P = 16nm

W_P = 120nm

Pulse= 0 to 1v

Rise time= 1ns

Fall time = 1ns

Width X1, X2 &X3,Srb=10ns,10ns,20ns,20ns

Period X1,X2& X3,Srb=20ns,30ns,40ns,40ns

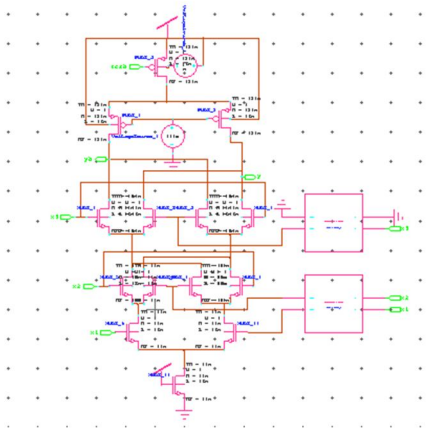
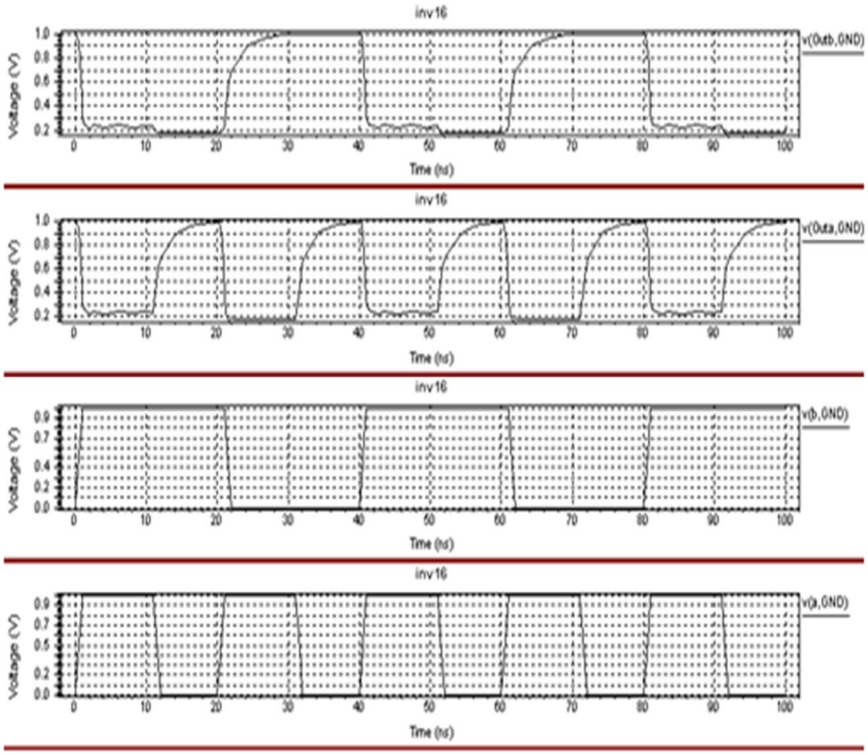


Fig.6: Schematic of MCML three input Carry circuit without sleep transistor

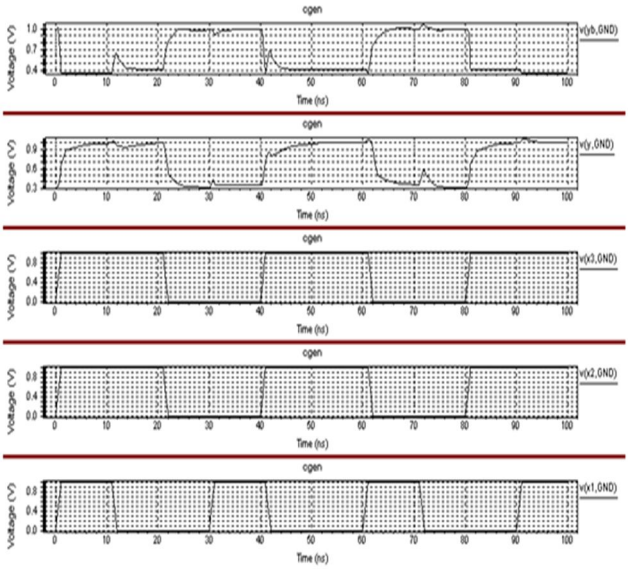
V. RESULT and DISCUSSION

In this section we have simulated the all designed circuits for the functionality correctness circuits.

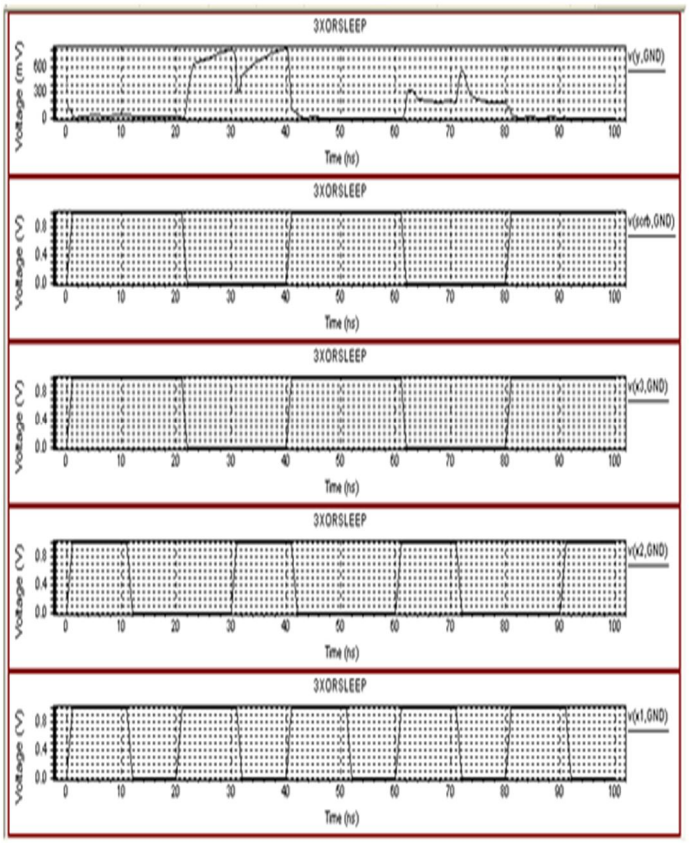
Waveform of MCML inverter



Waveform of 3 input carry circuit with out sleep transistor



Waveform of 3 input carry circuit with sleep transistor



VI. CONCLUSION

Mathematical operation is the key operation of many microprocessor and special purpose processors. Earlier presented carry circuits are efficient. But they are not so efficient than MCML based carry circuits with concept of sleep transistors. This research concluded that without sleep transistor carry circuit power consumption is 27.833uW while with concept of sleep transistor power consumption is 23.327uW

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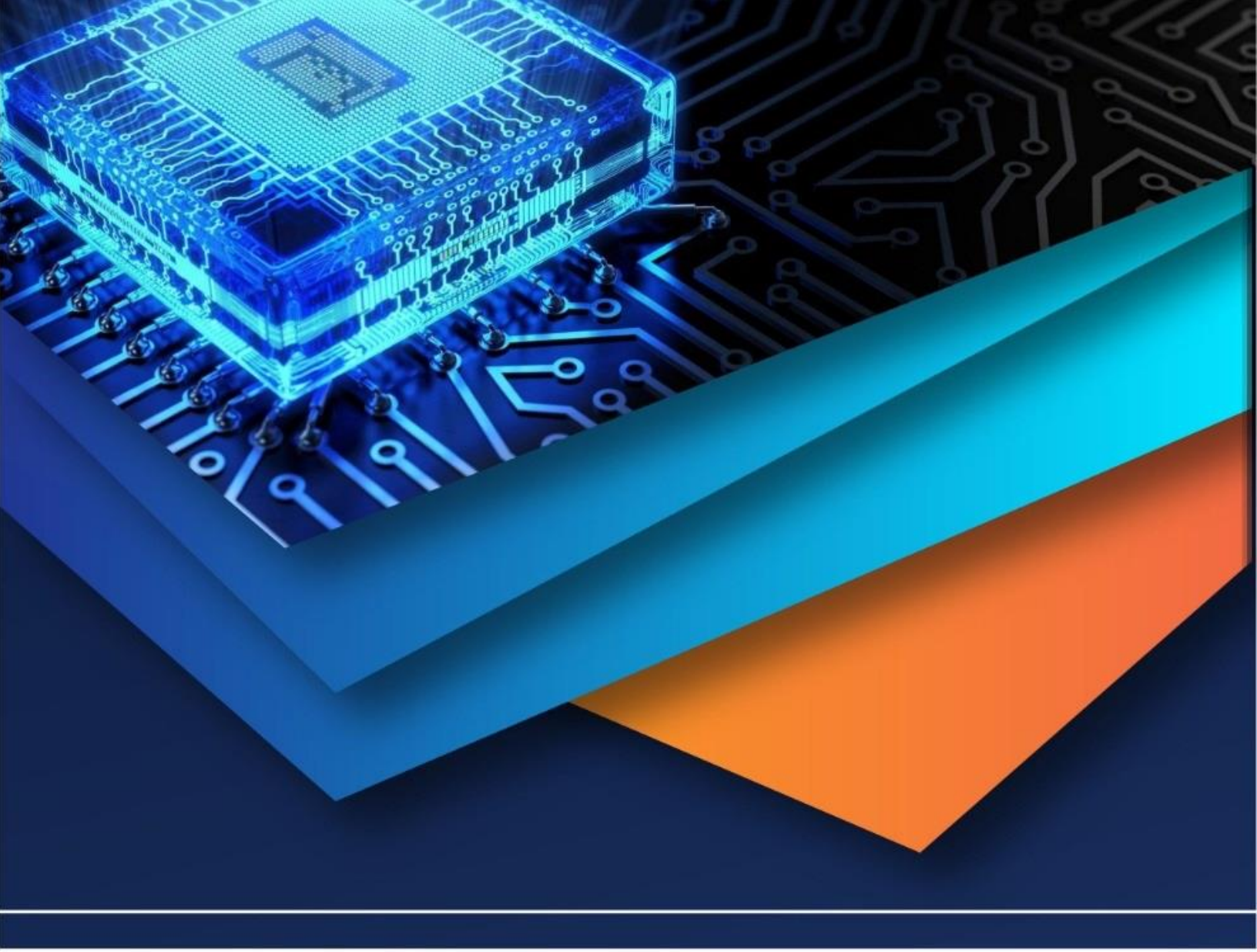

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