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Current Situation and Development of Power System Simulation Technologies

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Abstract: ***This team paper condenses the best in class ongoing advanced reenactment ideas and innovations that are utilized for the investigation, plan, and testing of the electric power framework and its contraption. This paper features the primary building squares of the continuous test system, i.e., equipment, programming, input-yield frameworks, displaying, and arrangement procedures, interfacing capacities to outside equipment and different applications. It covers the most usually utilized ongoing computerized test systems in both industry and the scholarly world. An exhaustive rundown of the ongoing test systems is given in an unthinkable survey. The goal of this paper is to outline striking highlights of different continuous test systems, with the goal that the peruser can profit by understanding the important innovations and their applications, which will be exhibited in a different paper.***

Index Terms: Digital constant reproduction (DRTS), advanced test systems, equipment on the up and up (HIL) reenactment, control designing, control framework transient recreation, continuous frameworks. To the chose time-step, the reenactment is viewed as

I. INTRODUCTION

Computerized ongoing reenactment (DRTS) of the electric power system is the reproduction of output (voltage/flows) waveforms, with the ideal exactness, that are illustrative of the conduct of the genuine power framework being demonstrated. To accomplish such an objective, a computerized ongoing test system needs to explain the model conditions for one time-venture inside a similar time in certifiable clock [1], [2]. Thusly, it produces yields at discrete time interims, where the framework states are figured at certain discrete occasions utilizing a fixed time-step.

DRTS is a strategy for the transient reenactment of intensity frameworks utilizing advanced PC time-space arrangement (e.g., utilizing an electromagnetic transient-type approach) [3]– [6]. Frameworks are spoken to by taking advan-tage of the part models accessible in the library of the product device utilizing a graphical interface and recreated on an equipment stage utilizing parallel calculation.

Two circumstances can emerge contingent upon the time required by the reenactment stage to finish the calculation of state yields for each time-step (Fig. 1): 1) if the execution time, Te, for the reenactment of the framework is shorter or rise to constant [Fig. 1(a)]; and 2) if Te is more noteworthy than now is the right time step measure for at least one time- steps, invades happen and the recreation is considered as nonreal-time or disconnected. In the last case, either the time-step can be expanded or the framework model can be rearranged to run it continuously.

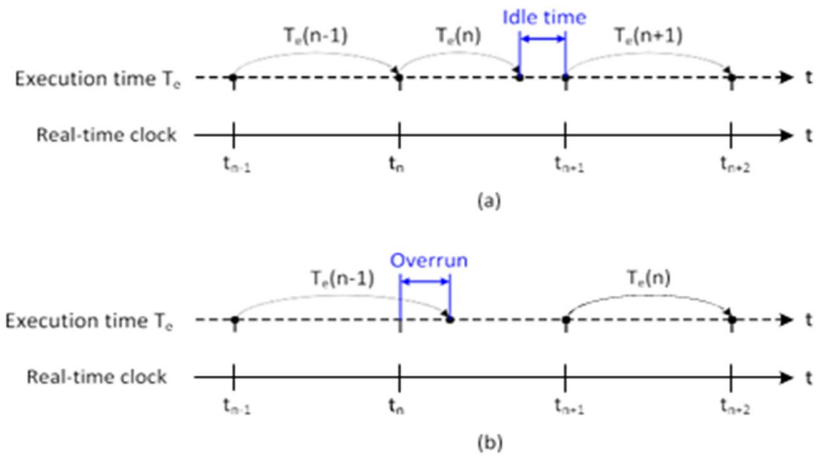

FIGURE 1. Illustration of real-time and offline simulation.

A. Real-Time Simulation.

B. Non-Real-Time Simulation.

The point of this paper, along these lines, is to given a review of the best in class continuously recreation advancements for power frameworks configuration, testing, and investigation. The principle com-ponents and ideas just as a diagram of ordinarily accessible arrangements are exhibited in this survey paper.

Whatever is left of this paper is composed as pursues. Segment II presents diverse classifications of continuous test systems, and in Section III, their assessment throughout the most recent couple of years is displayed.

II. CATEGORIES OF DIGITAL REAL-TIME SIMULATION

Connected to the area of intensity frameworks can be classi- fied into two classifications: 1) completely advanced continuous reproduction (e.g., show on the up and up, programming on top of it, or processor-on the up and up), and 2) equipment on the up and up (HIL) constant recreation. A completely advanced continuous reenactment requires the whole framework (counting control, insurance, and different frill) to be demonstrated inside the test system and does not include outside interfacing or data ources/yields (I/Os). Then again, the HIL reproduction alludes to the condition where parts of the completely computerized continuous recreation have been supplanted with real physical segments.

The HIL method of the reenactment continues with the gadget under-test or equipment under-test (HuT) associated through information yield interfaces, e.g., channels, advanced to-simple and simple to-computerized converters and flag conditioners. Constrained ongoing controls of the recreation can be executed with the client characterized control contributions, for instance, shutting or opening of changes to interface or disengage the segments in the mimicked power framework.

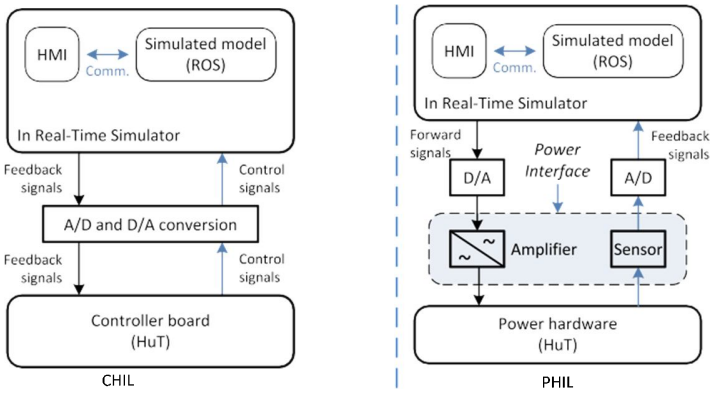

FIGURE 2. Basic HIL simulation concept for CHIL and PHIL.

Any HIL reproduction including power exchange to or from the HuT is known as power equipment insider savvy (PHIL) (Fig. 2). For this situation, some portion of the power framework is inside recreated and the other part is the genuine equipment control contraption associated remotely.

A power source or sink (associated through the PHIL interface) is required for this setup, which will either produce or retain control. Allude ence signals are created dependent on the arrangement of the vir-tual framework inside the ongoing test system and are sent to the power intensifier that produces voltages or flows to be connected to the HuT. Criticism signals acquired from the voltage/current estimations of the HuT are properly scaled and taken back to the test system to finish the reenactment circle.

A case of such reenactment could be the continuous testing of machines, converters [7], blame flow limiters, or some other electrical hardware.

Testing of security gadgets, for example, transfers, may require voltage or current enhancers for HIL-based testing; in any case, no power is traded all things considered [8], [9]. The utilization of a speaker is chiefly for the gadget to detect the genuine voltage and additionally current signs. All in all, a completely computerized reenactment is frequently utilized for understanding the conduct of a framework under certain cir-cumstances coming about because of outside or inward powerful influ-ences, though a HIL recreation is utilized to limit the danger of venture using a model once the under- lying hypothesis is set up with the assistance of a completely DRTS.

III. EVOLUTION OF DIGITAL REAL-TIME SIMULATORS

Using parallel processor-based computerized advancements and improved numerical examination methods with less com-putational load, various advanced constant simula-tors have been proposed and tried [10]– [20]. Starting ongoing test systems depended on the advanced flag processor (DSP) [10]– [12], decreased guidance set PC (RISC) [13]– [16], and complex guidance set PC [17] tech-nologies; be that as it may, the utilization of broadly useful processors as the calculation motor has turned into an appealing alternative on account of their lower cost and quicker improvement cycle [21]. Improvement of a bunched framework, utilizing off-the-rack computerized processors, depends on cutting edge correspondence systems, which is turning into a developing pattern for the advancement of the DRTS. The primary business constant computerized test system (RTDS) was shown by RTDS Technologies Inc. in 1991 utilizing DSPs [13]. It was interfaced to the controller of a high voltage direct current converter to evaluate its execution. A combi-country of both simple and computerized parts was utilized in that simu-lator. From that point forward, this test system has developed and turned out to be one of the broadly utilized business RTDSs. The primary little scale advanced constant test system for the continuous trial of the power framework hardware dependent on a standard multipurpose parallel-PC framework, known as the computerized transient system analyzer (DTNA), is exhibited in [16]. The DTNA could sim-ulate electromagnetic transient wonders up to 3 kHz, air conditioning/dc associations, electromechanical drifters, and comparative long-lasting marvels. A wide assortment of segments, gear, and controllers, including power electronic-based controllers, can be displayed and mimicked utilizing this test system. No completely advanced continuous test system was conceivable in a standard PC before 1996, when Électricité de France presented their first ongoing test system ARENE [18]. It was fit for reproducing the high-recurrence marvel in a standard, multipurpose parallel PC. Another PC-based continuous test system, NETOMAC [19], [20] from SIEMENS, was utilized to mimic extensive power frameworks. Nearly in the meantime, another universally useful processor-based continuous test system from OPAL- RT Technologies Inc. [21]– [25] was presented, which utilizes the MATLAB/Simulink as the primary demonstrating device for the reproduction. Right around a comparative methodology of utilizing a standard PC for constant reenactment and control was embraced by dSPACE [26], which utilizes universally useful processors and MATLAB/Simulink as the displaying bundle, however their more seasoned age test systems utilized DSPs. HYPERSIM [27]– [29] is another completely computerized continuous sim-ulator for the examination of the electromagnetic and electrome-chanical drifters in extensive and complex power frameworks and initially created by IREQ, the Hydro-Quebec's exploration organization. Other than the previously mentioned constant test systems, custom research center scale ongoing test systems have been exhibited in the writing. These continuous test systems utilize a mix of equipment and programming for the most part to serve spe-cific necessities. field-programmable entryway exhibits (FPGAs) [30]– [35] and designs preparing unit (GPU) [43] are two such advanced processors that are picking up establishment as a calculation equipment for continuous reproduction.

IV. COMPUTING CAPABILITIES OF REAL-TIME SIMULATORS

Around 50 µs or a littler time-venture (for appropriate goals in 50-/60-Hz control frameworks) to replicate homeless people reliably. Figuring ability might be characterized as the push uct of the quantity of hubs/transports in the reenacted power organize and the quantity of time steps taken every second. For a 50-/60-Hz air conditioning power organize, this ability compares to a substantial hub/transport tally and genuinely low speed; notwithstanding, for power-electronic frameworks working with higher exchanging frequencies, littler time-steps are required. Whenever controlled carefully, high-recurrence exchanging circuits may work with a microcontroller having an interior clock speed with times of 1 µs to 10 ns. A reenactment of such a framework may require all the more figuring capacity and the capacity to reproduce with a little time-step. Regardless of the fast inner dynam-ics of the power hardware based device, the framework level cooperations may not require a little time-step. Fig. 3 demonstrates the connection between registering hubs and time-step prerequisites for various frameworks. The power framework recreation might be adequate at a relatively bigger time-step, and for a steady registering force, it permits a bigger framework, though for power gadgets reproduction, littler time-steps are vital, bringing about a littler framework for a similar calculation control.

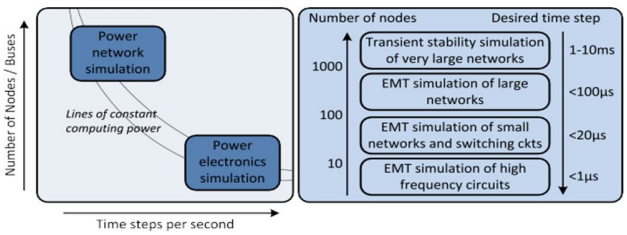

FIGURE 3. Illustration of (a) computing capability requirements for different types of systems and (b) time-step requirement for different types of simulation.

A continuous test system is frequently designed to be versatile. The addition of figuring power is conceivable by including rack-mount units that require information correspondence between racks. Singular processing units work in parallel, offering a sensible scaling property; nonetheless, commu-nication includes time delay. Correspondence bottlenecks are limited by misusing the making a trip wave properties to decouple the arrangements of the system subsystems that are isolated by transmission lines of suitable length that is predictable with the recreation step interim [13]. Power processors or other equipment, for example, universally useful focal handling units (CPUs) work in parallel by sharing normal recollections or transports to limit the correspondence latencies.

V. CHARACTERISTICS OF REAL-TIME SIMULATORS

A. Common Features Of Real-Time Simulators

Most DRTS have the accompanying regular qualities:

1) Multiple processors work in parallel to frame the objective stage on which the reenactment keeps running progressively;

2) A host PC is utilized to set up the model disconnected and afterward accumulate and load it on the objective stage. Host PCs are additionally utilized for observing the consequences of continuous reproduction; 3)

I/O terminals to interface with outer equipment; 4) a correspondence system to trade information between different targets when the model is part into various subsystems. A different correspondence connect is required for information trade between the host and the objective-specific names.

B. Large-Scale And Commercial Real-Time Simulators

This segment depicts the qualities of two broadly utilized vast and versatile RTDSs. We allude to them as Type-An and Type-B test systems.

1) *Hardware:* For the majority of the recreation conditions, equipment specifically impacts the figuring capacity of the test system. Equipment for various ongoing test systems developed with time, and in this paper, an exertion has been made to portray the present best in class equipment.

Fig. 4 demonstrates the equipment engineering of a Type-A test system [13] that utilizes custom equipment amassed in units called racks. The racks contain a few space mounted processor cards known as PB5 cards, each containing two PowerPC RISC processors working in parallel, and fills in as the principle computational motor. A limit of six processor cards or 12 processors can be put into one rack and the greatest number of hubs that can be reproduced utilizing each card are 72. The processor card likewise permits two system arrangements (each system arrangement requires one processor) to be incorporated into one rack to speak to two subsystems with 72 hubs each. Bigger systems with more hubs/subsystems can be spoken to utilizing extra racks.

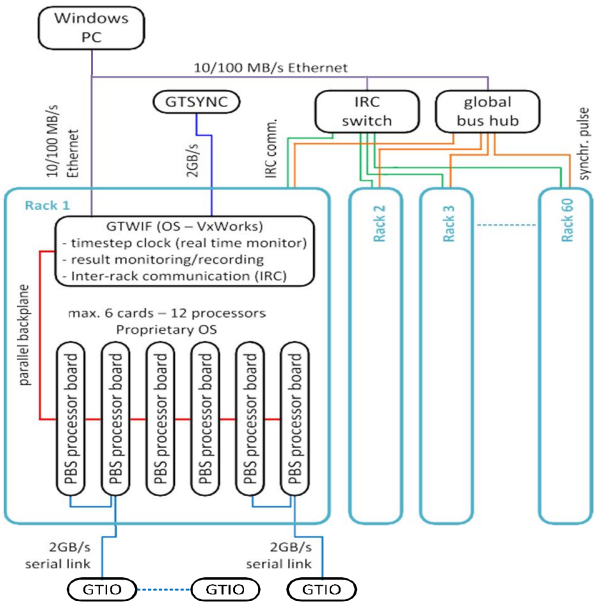

Figure 4. Hardware architecture of RTDS simulator.

Utilized for the Ethernet commu-nication between the host (i.e., a Windows-based PC) and the objective (i.e., the racks). The GTWIF additionally gives communica-tion interfaces between racks just as implements synchronization and ongoing task of the processors. Various fringe segments are likewise accessible for this test system. The GTSYNC card is utilized to synchronize the reproduction time-venture to an outer time reference (e.g., a worldwide position framework clock, which likewise synchronizes the gadgets under test), GTIO cards to encourage physical associations with outside equipment by means of simple and advanced I/O, the GTNET card to give correspondence by means of abnormal state Ethernet conventions (e.g., IEC 61850, DNP, C37.118, etc), the worldwide transport center for constant synchronization of three racks or more, etc. This equipment is specially crafted, and itemized portrayals are accessible in [36]. As of late, this test system presented the use of FPGAs related to its fundamental processors to play out the recreation of extremely high-recurrence (20– 100 kHz) exchanging circuits [37].

Another business off-the-rack segment based scal-capable constant (Type-B) test system is built up that utilizes broadly useful multicore multithread CPUs, for example, master cessors from Intel Xeon or the AMD group of CPUs [38]. Utilizing a multi-CPU motherboard, the test system can be stretched out up to numerous centers per target framework, and each center can be utilized to demonstrate a subsystem [38]. Fig. 5 demonstrates how different segments of the equipment are associated with structure the constant test system.

2) Software: Programming required for ongoing test systems can be isolated into two primary classes: 1) working framework (OS) programming and 2) application programming. All in all, commer-cially accessible constant test systems keep running on either Windows-or Linux-based OSs. Notwithstanding, contingent upon the equipment, particular OSs might be important. For a large portion of the test systems, the OS is provided by the merchant. For specially designed ongoing test systems, equipment explicit OS might be required and regularly accompanies the equipment. card known as a GTWIF card. The GTWIF is an IBM PPC405- based processor card.

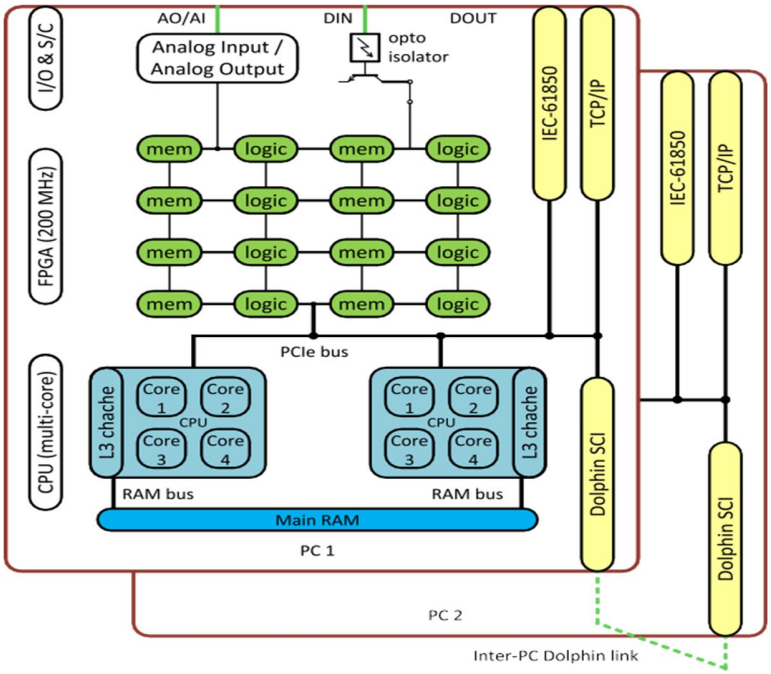

Figure 5. Hardware architecture of emegasim real-time simulator.

The utilization of a custom model or custom code is conceivable if the given model does not meet the client prerequisite. Since the test system depicted in [36] is based upon cus- tom equipment, the GTWIF OS depends on VxWorks, however the PB5 processor card utilizes an exclusive uncovered metal OS for expanded effectiveness. Its application program programming suite keeps running on a Windows-based host stage and is utilized to manufacture the model, set up reenactments, control, secure information, and change framework parameters amid a reproduction. The other test system [38] utilizes Linux-based stages, for example, RedHawk, RedHat, or QNX as the OS for the objectives, and adjusts them to help the usefulness and the perfor-mance required by complex continuous applications. One key part of the adjusted Linux is the finished center protecting, where every one of the centers aside from one are committed for continuous calculation and are protected from framework intrudes.

3) *Communication And Interfacing:* The Type-A test system utilizes a typical correspondence back-plane that interfaces all opening mounted cards inside a rack and encourages the trading of data. Direct card-to-card correspondence is additionally conceivable through the various fiber optic connections situated on the processor cards. The processor card fiber optic connections are likewise used to interface I/O cards in parallel or potentially in a daisy chain. In a multirack test system, the backplanes work autonomously and in parallel, along these lines decreasing correspondence bottlenecks. Data that must be shared between racks is passed by means of interrack communica- tion (IRC) channels on the GTWIF cards (point-to-point com-munication). For test systems with in excess of seven racks, an IRC change is utilized to give direct correspondence between upwards of 60 racks (star-point correspondence). The commu-nication between the test system racks and the host PC is performed by the GTWIF cards utilizing standard Ethernet.
4) *Modeling Tools/Libraries:* The Type-A test system utilizes a typical correspondence back-plane that interfaces all opening mounted cards inside a rack and encourages the trading of data. Direct card-to- card correspondence is additionally conceivable through the various fiber optic connections situated on the processor cards. The processor card fiber optic connections are likewise used to interface I/O cards in parallel or potentially in a daisy chain. In a multirack test system, the backplanes work autonomously and in parallel, along these lines decreasing correspondence bottlenecks. Data that must be shared between racks is passed by means of interrack communica-tion (IRC) channels on the GTWIF cards (point-to-point com-munication). For test systems with in excess of seven racks, an IRC change is utilized to give direct correspondence between upwards of 60 racks (star- point correspondence). The commu-nication between the test system racks and the host PC is performed by the GTWIF cards utilizing standard Ethernet.
5) *Solution Methodology:* A test system utilizes Dommel's electro attractive tran- sients program (EMTP)- type calculation [4], [8] to discretize every one of the segments of the circuits, including detached ele-ments, for example, breakers and deficiencies. Dynamic sources are mod-eled as proportionate sources with a few sorts of impedances, including positive and zero groupings. The system arrangement performs constant decay of the induction grid that enables ceaselessly changing conductance components to be spoken to in the circuit. Then again, a Type-B test system likewise utilizes a nodal induction based solver called ARTEMiS-SSN [42]. In this test system, models are based upon the Simulink and SimPowerSystems stages, where default trapezoidal or in reverse Euler solver/coordination calculations accessible in MATLAB/Simulink for discrete arrangement could be utilized. These solvers, in any case, are not intended for entirely constant recreation, in light of the fact that the arrangement time of each progression changes extensively. The ARTEMiS-SSN solvers implement entirely fixed time-step reproduction for these models and are successful for systems under 100 three-stage transports [41]. ARTEMIS- SSN is a nodal permission solver that utilizes a fixed- advance higher request discretization/arrangement calculation and utilizations the insertion strategy, permitting extremely exact discovery of exchanging occasions. It likewise precomputes the nodal friend lattices, got from their particular state-space conditions, joined with online refactorization of the nodal permission network and along these lines furnishes a quicker recreation contrasted and the SimPowerSystems solvers. Notwithstanding the EMTP-type arrangement, both Type-An and Type-B DRTS offer the cross breed arrangement method, where part of the system in detail is fathomed utilizing an EMTP-type sim-ulation while thinking about its collaboration with an a lot bigger system, which is reproduced utilizing a transient steadiness solver. Type-B DRTS additionally permits the continuous phasor reenactment of systems with in excess of 10 000 transports for each center [43]. Regardless of the reenactment type (EMTP or phasor), it is required to address the synchronizing of discrete occasions that happens amid the time-venture of reproduction. Despite the fact that this is a major test for DRTS, various strategies have been distributed [44]– [47], and such test systems apply reasonable techniques in individual cases.
6) *Inputs And Outputs:* A test system utilizes Dommel's electro attractive tran- sients program (EMTP)- type calculation [4], [8] to discretize every one of the segments of the circuits, including detached ele-ments, for example, breakers and deficiencies. Dynamic sources are mod-eled as proportionate sources with a few sorts of impedances, including positive and zero groupings. The system arrangement performs constant decay of the induction grid that enables ceaselessly changing conductance components to be spoken to in the circuit. Then again, a Type-B test system likewise utilizes a nodal induction based solver called ARTEMiS-SSN [42]. In this test system, models are based upon the Simulink and Sim Power Systems stages, where default trapezoidal or in reverse Euler solver/coordination calculations accessible in MATLAB/Simulink for discrete arrangement could be utilized. These solvers, in any case, are not intended for entirely constant recreation, in light of the fact that the arrangement time of each progression changes extensively. The ARTEMiS-SSN solvers implement entirely fixed time-step reproduction for these models and are successful for systems under 100 three-stage transports [41]. ARTEMIS- SSN is a nodal permission solver that utilizes a fixed- advance higher request discretization/arrangement calculation and utilizations the

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C. Open-Source Or Noncommercial Real-Time Simulators

Outside the exclusive world, there are some constant sim- ulators worked in numerous labs that left research ventures for filling an in-house need. One such minimal effort ongoing test system known as virtual proving ground (VTB-RT) was created at the University of South Carolina. While a fundamental way to deal with ongoing augmentation in VTB was proposed a couple of years back [49], another, further developed procedure has been created as a team with RWTH Aachen University in Germany [50]. This first ongoing augmentation depends on the very same solver received for the work area rendition, while the new form depends on a reproduction technique explicitly created for constant recreations [51], [52].

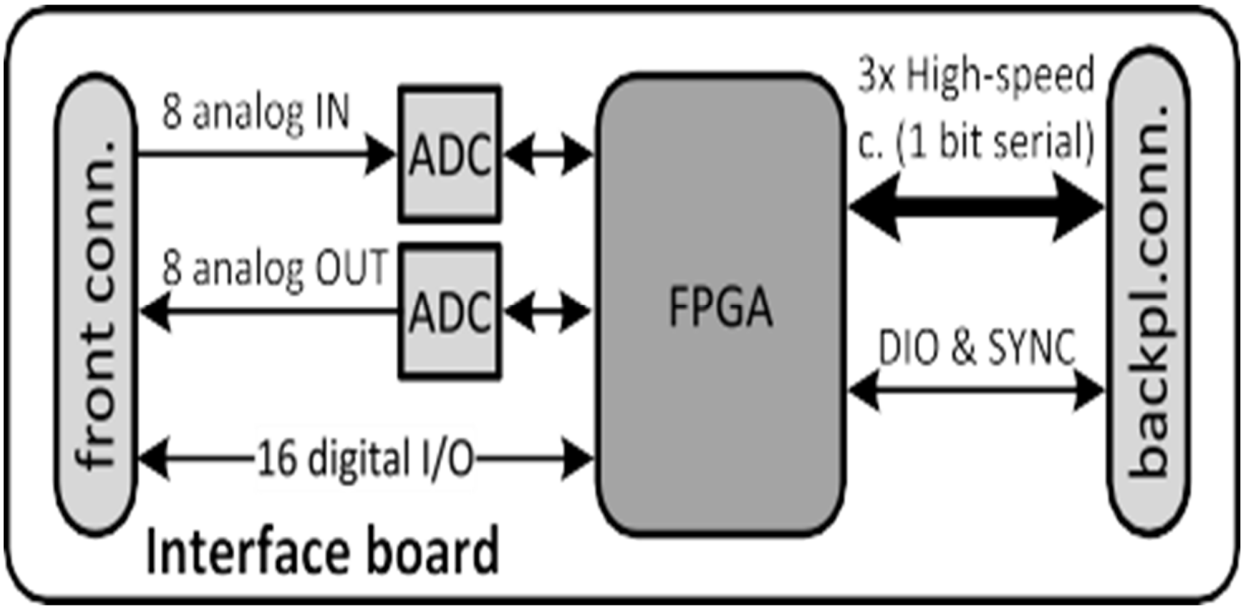

FIGURE 6. DSP cluster-based architecture of VTB-RT simulator.

TABLE 1. Summary of salient features of RTDSs reported in the literature.

Real-Time Simulator	Hardware	OS and Application Software	Communication, Protocols, Inter-facing and I/C	Modeling and Solution	Application	Other

RTDS from RTDS Technologies Inc. [13], [14], [36]	PowerPC RISC processors are implemented in cards (PB5), GTFPGA	Host OS: Windows Target OS: VxWorks Application software: RSCAD	Optical fiber, fast back plane, global bus hub, Gigabit Ethernet, DNP3, IEC61850, TCP/IP C37.118, analog and digital I/O, third party I/O through GTNET	EMTP -type library of component models, small time-step models for some components, Dommel's algorithm based Nodal solver	Real-time simulation of power systems, power electronics, control systems, testing of equipment through HIL simulation	Allows multi-rate simulation
eMEGAsim from OPAL-RT Technologies Inc. [23], [38]	Multi-core CPU, FPGA, commercial-of-the-shelf motherboard	Host OS: Windows Target OS: Linux based (QNX, RedHat) Application software: Matlab/Simulink, RT-Lab suite containing tools for EMTP type and Phasor analysis	Shared memory, Gigabit Ethernet, Dolphin networking, IEC61850, C37.118, DNP3, FPGA-based analog & digital I/O terminals, supports third party I/Os	Simulink and in-house tool boxes, code (C/C++, Matlab, Fortran) wrapped with S-function, discrete Simulink solvers, vendor specific solvers such as ARTEMIS-SSN	Real-time simulation of power electronics, power systems, control and automotive systems, multi-domain simulation, HIL testing and simulation	Multi-rate simulation, ePHASORsim transient stability extension available, EMT models can be implemented on FPGA cards [48], multi-domain as it supports all Simulink block-sets
HYPERSIM [27], [29]	CPUS are used with SGI's NUMAlink processors interconnect architecture, can parallelize up to 2500 cores, FPGAS can be interfaced	Host OS: Windows Target OS: Linux based Application software: Hypersim software suite	Gigabit Ethernet, IEC 61850, standard PCIe interface with DSP based A/D and D/As	GUI based component library is available through which system model is built, state-space solution method is used with multiple integration rules	Real-time simulation of power systems with power electronics, control systems, HIL testing	Implementable in eMEGAsim platform for smaller scale transmission systems, automatic task mapping to available processors
dSPACE [26]	CPU	Host OS: Windows Target OS: QNX ROS	Gigabit Ethernet, PCIe based communication with other hardware and I/O uses proprietary dSPACE protocol, IOCNET	Simulink, Stateflow, AUTOSAR, C coded models	Mainly used for real-time control and rapid prototyping for automotive engineering, aerospace, and industrial control	---
VTB [49]-[52]	DSP cluster or multi-core CPU/FPGA	Host OS: Windows Target OS: Linux	---	Modified resistive companion	Power system	Multi-physics possible
xPC Target [53]	CPU, FPGA	Host OS: Windows Target OS: Optimized Real-time Kernel	Analog and Digital I/O modules are supported through PMC, PCI, PCIe, cPCI, and PC104 protocols, serial, TCP/IP, UDP/IP, CAN, J1939, ARINC 429, and MIL-STD-1553	Simulink and Stateflow for model development, Simulink Coder, HDL coder, C	Rapid prototyping, real-time testing of applications and HIL simulation.	Multi-physics
rtX from ADI [54]	CPU	Host OS: Windows Target OS: QNX RTOS Application software: AdvantageDE	I/O interfacing through PCI, PXI, PCIe, PMC etc.	GUI based Advantage DE can be interfaced with Simulink, SystemBuild, C, Fortran, ADEPT, ALTIA	Power system simulation for avionics and maritime industries, aircraft simulation, shipboard simulation	---
Typhoon RTDs [55], [56]	FPGA	Host OS: Windows Target OS: FPGA	FPGA based Analog and Digital I/Os, IEEE 1284C, Ethernet RJ45	Typhoon schematic editor, SpiceShuttle, Matlab.	Testing of power electronics controller	---

VI. CONCLUSION

The primary goal of this team paper is to feature the present condition of the innovations utilized in the continuous reenactment industry for power framework applications. It has abridged the most notable highlights of constant reproduction stages with applications identified with power and vitality sys-tems. In spite of the fact that various continuous test systems are accounted for in Table 1, just a couple of them are fit for recreating substantial frameworks. The remaining are either appropriate for little frameworks or to fill in as a constant controller. Accordingly, the attributes of three primary ongoing test systems (i.e., RTDS, eMEGAsim, HYPERSIM, and VTB) are examined in detail, though those of whatever remains of the test systems are recorded in the outline table. The vast majority of the constant test systems are fit for interfacing outer equipment to perform HIL tests and examinations. Albeit intended for power frameworks applications, huge numbers of these continuous test systems are appropriate for performing cosimulation utilizing multirate / multiphysics reproduction. With constant client support, these test systems can be utilized to suit any unique needs of the customers. In the following stage, the team will take a shot at a comparative paper that will condense the utilizations of continuous test systems.

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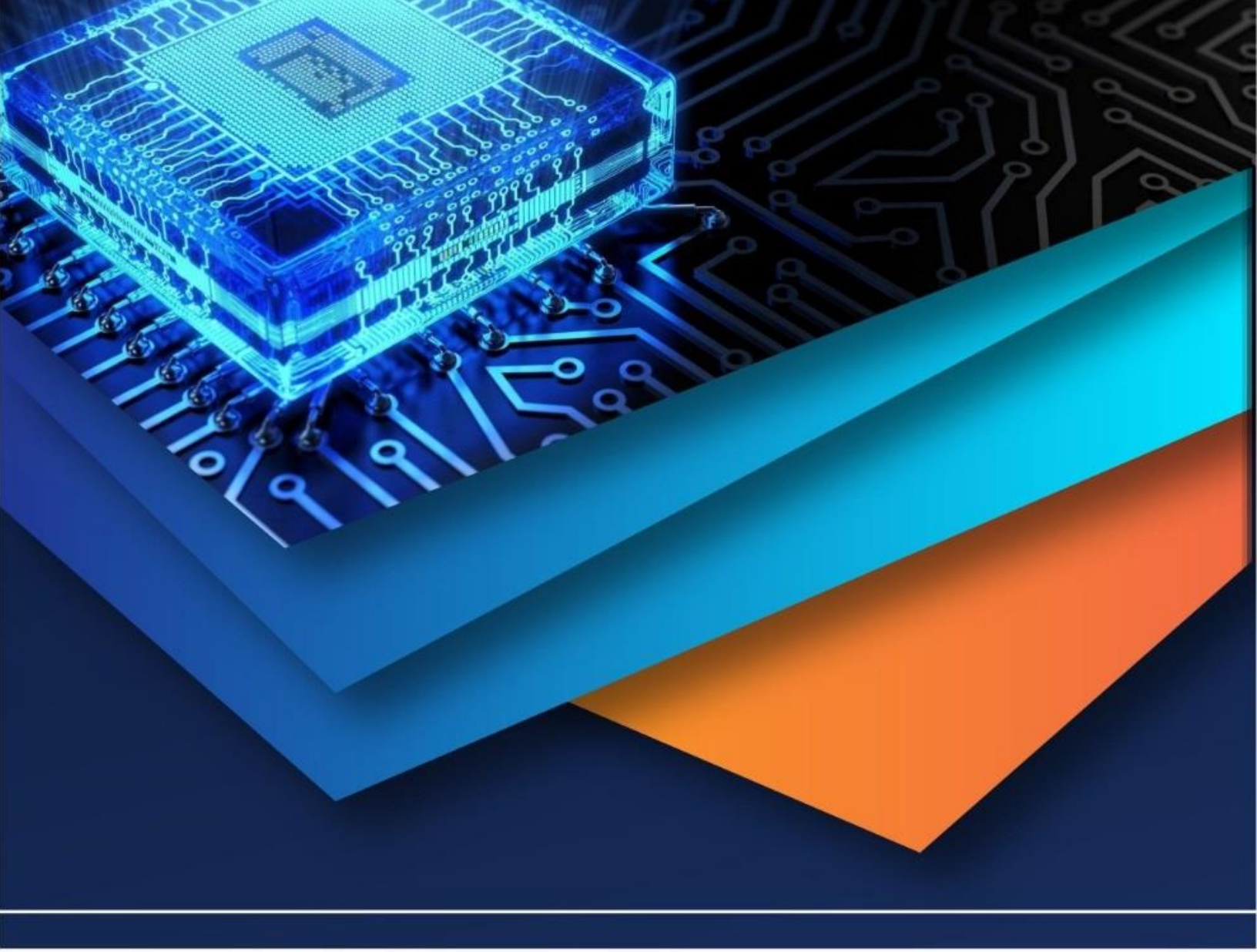

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