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Performance Analysis of Vedic Multiplication Technique using FPGA

Gaikwad Minal Nivrutti[1], Bendkule Priyanka Devram[2], Sonawane Punam Pandit[3], Mr.Rana S. Mahajan[4]
[1, 2, 3] *Students of Electronics & Telecommunication, Sir Visvesvaraya Institute of Technology, Maharashtra, India*
[4] *Assistant Professor, Department of Electronics & Telecommunication, Sir Visvesvaraya Institute of Technology, Maharashtra, India*

Abstract — today, it is necessary to increase the speed of multiplier as the need of high speed processors is increasing. Multiplier is a main block of any processor. Conventional processors need great hardware resources and take more time in multiplication operation. This paper present a high speed multiplier based on ancient popular Vedic mathematics. Implementation is done on digital circuits. Vedic multiplication is accomplished in the same way as that of normal multiplierusing digital hardware. In this paper a comparison of concerned multipliers in 8, 16 and 32bits multiplications is performed. 8 bit and 16bit urdhva algorithm shows 50% improvement in delay than that of nikhilam, whereas 100% better than that of binary multiplier. 32bit nikhilam multiplier gives 52% improvement in delay than that of urdhva multiplier and 16% better than that of binary multiplier .multiplication is an important factor in arithmetic operations and is carried out in variation of digital signal manage applications. As multipliers take a long time for execution so there is a need of fast multiplier to save the execution time. This paper describes the multiplication using ancient Indian Vedic mathematics multiplication techniques. Vedic mathematics is the ancient system of mathematics which has a unique technique of calculations based on 16 sutras. The techniques described in this paper are nikhilam sutra, urdhva tiryakbhyam and karatsuba-of man and the performance analysis of these techniques is obtained. Modalism tool is used for simulation and the results obtained are compared on the basis of time delay of multiplication. This paper also describes the deliberateness and the fastness of different multiplier techniques Compared with each other.

Keywords--- Vedic mathematics, binary multiplier, urdhva triyagbhyam, nikhilam, Vedic multiplier, speed.

I. INTRODUCTION

Veda is the Sanskrit word which means knowledge. The word Vedic is derived from the word Veda. The concept of ancient Vedic Mathematics was brought by Sri Bharati Krishna Tirthain 1965. This concept is based on sixteen sutras or principles or aphorisms. It is a system of reasoning and mathematical working based on ancient Indian teachings called Veda. This method is very fast, efficient and easy to learn and use. It simplifies arithmetic and algebraic operations (multiplication, divisibility, complex numbers, squaring, cubing, and square and cube roots).With the latest technological developments in the field of computers and signal processing applications, the need for high speed processing has increased. Speed, area and power are very important factors to be considered and to improve the performance of any processor. The multiplier is a hardware block of any computing system. Multipliers are the commonly used architectures inside the processor. Multipliers hold a significant role in different DSP applications such as digital _altering, digital communication and Fast Fourier transform. The amount of circuitry involved is directly proportional to the square of its resolution. For multiplication, algorithms performed in DSP applications latency and through put are the two major factors for delay consideration. Real delay of any computation of a function is latency. Throughput is the measure of how many multiplications can be performed in a given period of time. Multiplier is not only a high delay block but also a major source of power dissipation .Hence this reason to minimize power consumption, it is of great interest to reduce the delay by using various delay optimizations. Data processing applications, digital signal processors and microprocessors in specific integrated circuits use the arithmetic operations of two binary numbers. Thus multipliers and Binary adders are important building blocks in VLSI Circuits. A huge set of components have been used in high performance systems such as ALU, filters, microprocessors, digital signal processors, etc. Multiplier is necessary because most of the DSP calculations involve the use of multiply accumulate operations. It is one of the most essential hardware blocks in image scheming, signal processing and arithmetic operation. In case of higher order multiplication, a huge number of adders are to be used to perform the partial product operation. The need of low power and high speed processor requires high speed multiplier. The Vedic multiplication technique is based on 16 Vedic principles. With technological advancement, a lot of researchers have been tried to design multipliers which other either of the following regularity of layout, low power consumption and not only less area but also combination of these in a multiplier. The Vedic mathematics is concerned with the Vedic mathematical formulae and it uses in application to various branches of mathematics and is considered very close to the way a human mind works.

II. OBJECTIVE AND AIM OF WORK

The primary Goal of this project is the use of Vedic mathematics lies in the fact that it reduces the typical calculation in the conventional mathematics to very simple once. Vedic mathematics is a several effective algorithms, ancient Indian Vedic mathematics, which has utilized for multi-plication to improve speed, area parameters of multipliers. After implementing the sutra it has been observed that Vedic multiplication is efficient in terms of speed.

III. BLOCK DIAGRAM

A technique called Vedic Mathematics for designing the multiplier that is fast as compared to other multipliers based on mathematical techniques that have been in practice for a long time. A processor's speed depends prominently on its multiplier as multipliers are used in various fields where processing of some signal is essential. Here, a high-speed 88 bit multiplier is designed and analysed which is based on the Vedic multiplier mechanism. This architecture is diverse from the conservative method of employing product of two numbers accomplished by the process of add and shift. The proposed method is efficient and fast, wherein the processing involves the vertical and crossed multiplication of precedent Vedic mathematics. It incorporates the partial products followed by additive result that too in a single step. The method and architecture decreases the complexity of the design of multiplier. The projected Vedic multiplier is coded in a high level digital language (VHDL) followed by synthesisation using EDA tool, XilinxISE12.2i. Finally, a comparison is made between results based on Vedic methodology and stereotyped multipliers. Surprisingly, the performance is found superior in terms of delay and thereby efficiency too. Since, Vedic mathematics technique exhibits low time processing thereby the present work will be helpful in preceding a step towards high speed multipliers and processors. The passage of time, multipliers have been proven as an essential component while designing microprocessors and other applications where processing of a signal is in foreground. Undoubtedly, assortments of adders are needed in realizing partial product and addition to accomplish a high order multiplication. High speed processors and hence we require high speed multipliers. Since a processor depends on its multiplier, multiplication is the key arithmetic procedure for the improvement of fast processor. A reduction in time delay along with power consumption is the important requirement for innumerable applications as well. Earlier multiplication comprises a succession of addition and subtraction followed by shifting the operands. By now array multiplication algorithm and booth multiplication algorithm are used in the digital hardware. The word VEDIC is a consequential of VEDA comprising accumulation of knowledge at single platform. Furthermore, it exhibits 16 Sutras that deals with several subdivisions including arithmetic, algebra, geometry and many more. Jagadguru Swami Sri Bharati Krishna Tirthaji in between 18841960, projected the concept of this ancient methodology that became very popular to achieve high speed processing of the data.

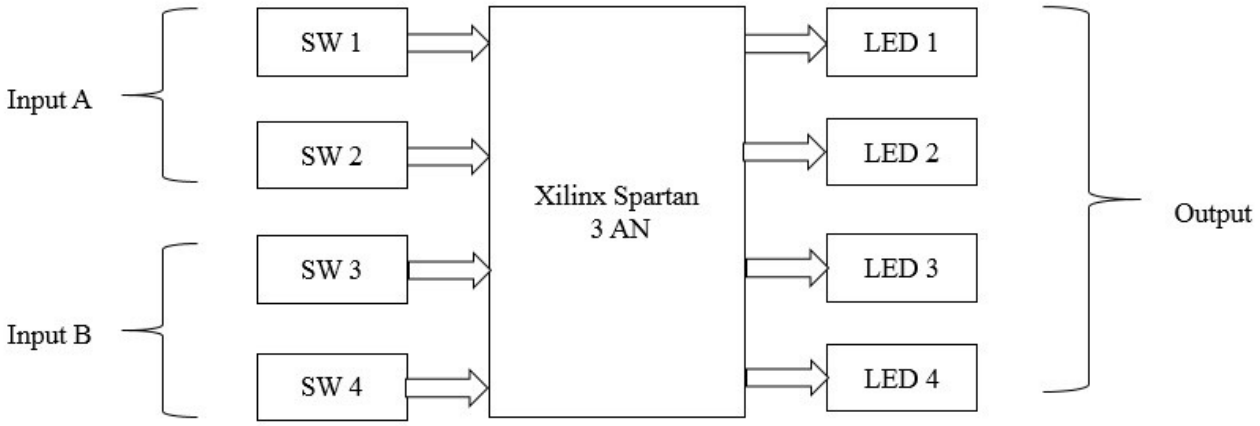

Fig. 1 Block Diagram

A. Spartan 3

The Spartan-3E family of Field-Programmable Gate Arrays (FPGAs) is specifically designed to meet the needs of high volume, cost-sensitive consumer electronic applications. The five-member family offers densities ranging from 100,000 to 1.6 million system gates. The Spartan-3E family builds on the success of the earlier Spartan-3 family by increasing the amount of logic per I/O, significantly reducing the cost per logic cell. New features improve system performance and reduce the cost of configuration. These Spartan-3E FPGA enhancements, combined with advanced 90 nm process technology, deliver more functionality and bandwidth per dollar than was previously possible, setting new standards in the programmable logic industry.

Because of their exceptionally low cost, Spartan-3E FPGAs are ideally suited to a wide range of consumer electronics applications, including broadband access, home networking, display/projection, and digital television equipment. The Spartan-3E family is a superior alternative to mask programmed ASICs. FPGAs avoid the high initial cost, the lengthy development cycles, and the inherent inflexibility of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary, an impossibility with ASICs.

B. Switch

A switch is an electrical component that can "make" or "break" an electrical circuit, interrupting the current or diverting it from one conductor to another. The mechanism of a switch removes or restores the conducting path in a circuit when it is operated. It may be operated manually, for example, a light switch or a keyboard button, may be operated by a moving object such as a door, or may be operated by some sensing element for pressure, temperature or flow. A switch will have one or more sets of contacts, which may operate simultaneously, sequentially, or alternately. Switches in high-powered circuits must operate rapidly to prevent destructive arcing, and may include special features to assist in rapidly interrupting a heavy current. Multiple forms of actuators are used for operation by hand or to sense position, level, temperature or flow. Special types are used, for example, for control of machinery, to reverse electric motors, or to sense liquid level. Many specialized forms exist. A common use is control of lighting, where multiple switches may be wired into one circuit to allow convenient control of light fixtures. Switch is a manually operated electromechanical device with one or more sets of electrical contacts, which are connected to external circuits. Each set of contacts can be in one of two states: either "closed" meaning the contacts are touching and electricity can flow between them, or "open", meaning the contacts are separated and the switch is no conducting. The mechanism actuating the transition between these two states (open or closed) are usually (there are other types of actions) either an "alternate action" (flip the switch for continuous "on" or "off") or "momentary" (push for "on" and release for "off") type.

C. Nikhilam Sutra

The formula simply means: all from 9 and the last from 10.

The formula can be very effectively applied in multiplication of numbers, which are nearer to bases like 10, 100, 1000i.e. to the powers of 10. The procedure of multiplication using the Nikhilam involves minimum number of steps, space, time saving and only mental calculation.

The difference between the number and the base is termed as deviation. Deviation may be positive or negative. Positive deviation is written without the positive sign and the negative deviation, is written using Rekhank (a bar on the number). Now observe the following table.

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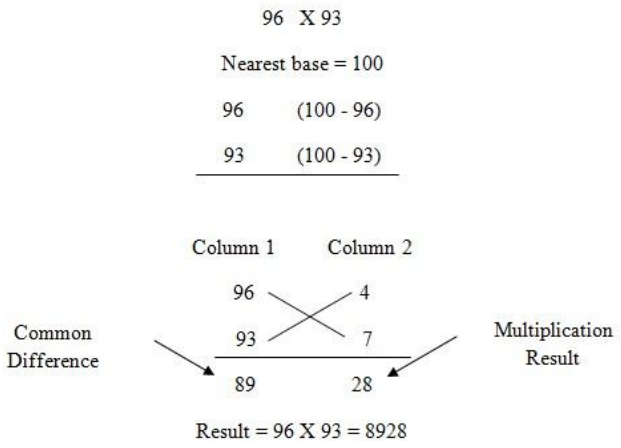


Fig. 3 Nikhilam Sutra

D. Urdhav Multiplier

Urdhava Tiryakbhyam (Vertically and Crosswise), is one of Sixteen Vedic Sutras and deals with the multiplication of numbers. The sutra is illustrated in Example 2 and the hardware architecture is depicted. In this example two decimal numbers (31 x 35) are multiplied. Line diagram for the multiplication of two, three and four digit numbers using Urdhava Method. The digits on the two ends of the line are multiplied and the result is added with the previous carry. When three or more lines are present, all the results are added to the previous carry. The least significant digit of the number thus obtained acts as one of the result digit and the rest act as the carry for the next step. Initially the carry is taken to be zero. In case, if there is a carry in (ad+bc) term, that is added to ac. From the Example 2, it is observed that all the partial products are generated in parallel. So the speed of the multiplier is higher compared to array multiplier.

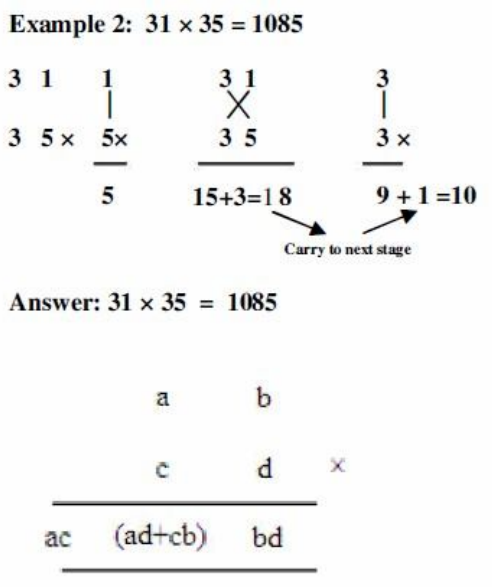
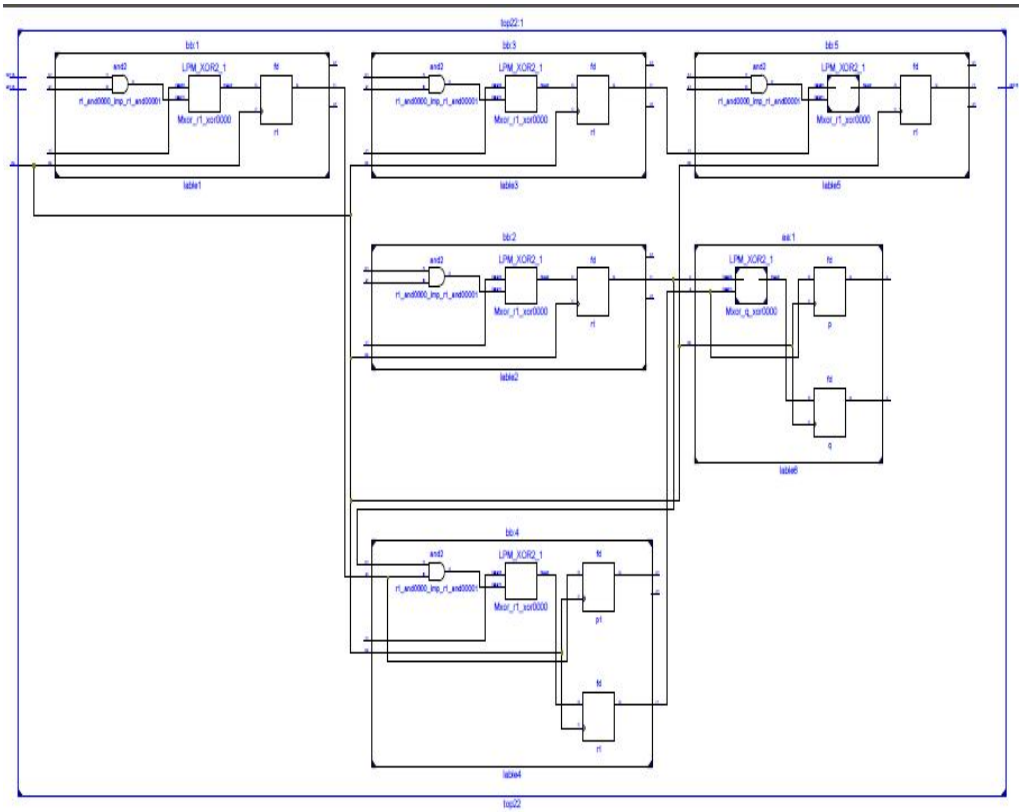


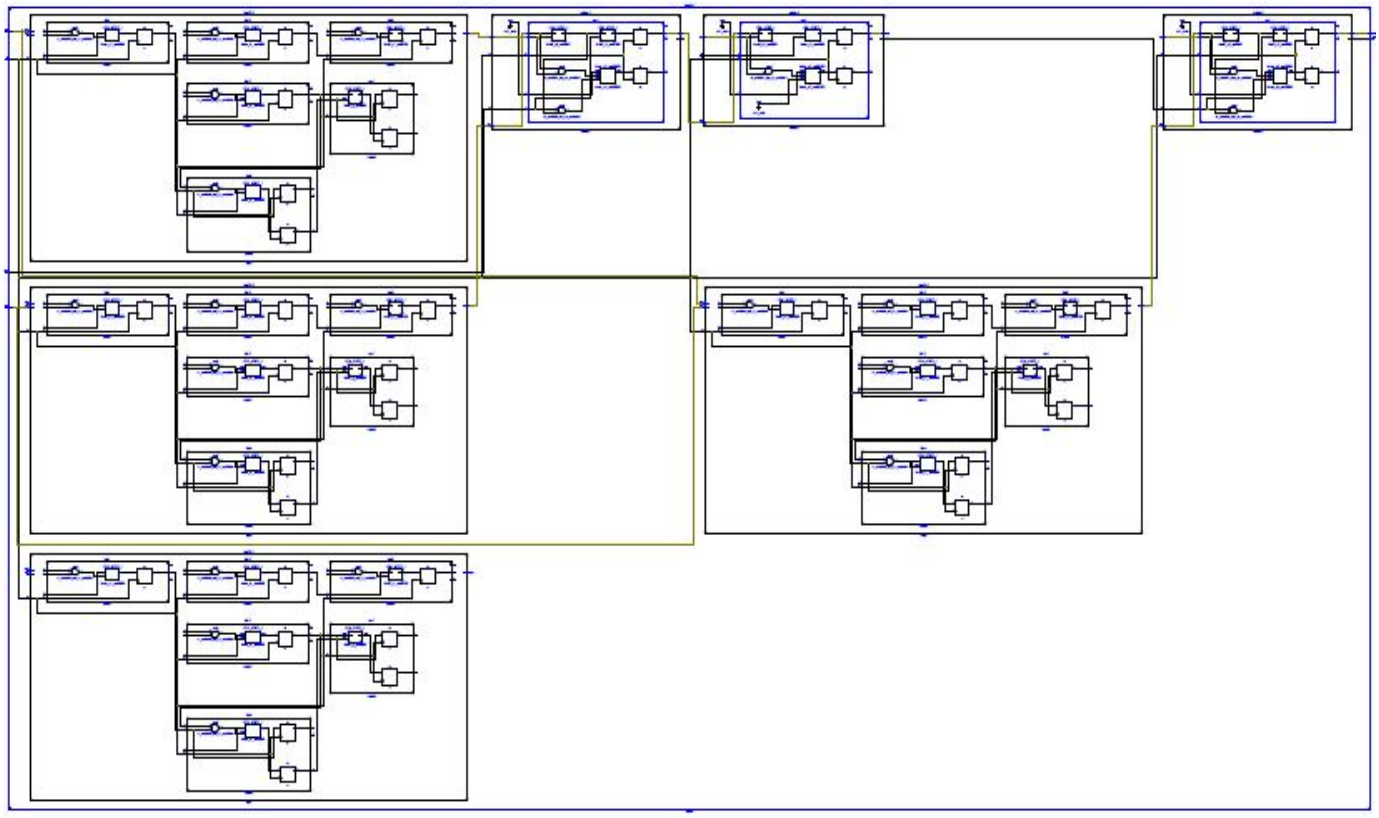
Fig. 3 Urdhav A Multiplier

IV. CIRCUIT DIAGRAM

A. RTL Schematic of 2 Bit Urdhva



B. RTL Schematic of 2 Bit Urdhva



V. CONCLUSIONS

Using the algorithm of Vedic mathematics speed of multiplication can be increased to improve the processing speed. In this multiplier by using Urdhva and Nikhilam sutra's. We observed that Vedic multiplication is efficient in terms of speed.

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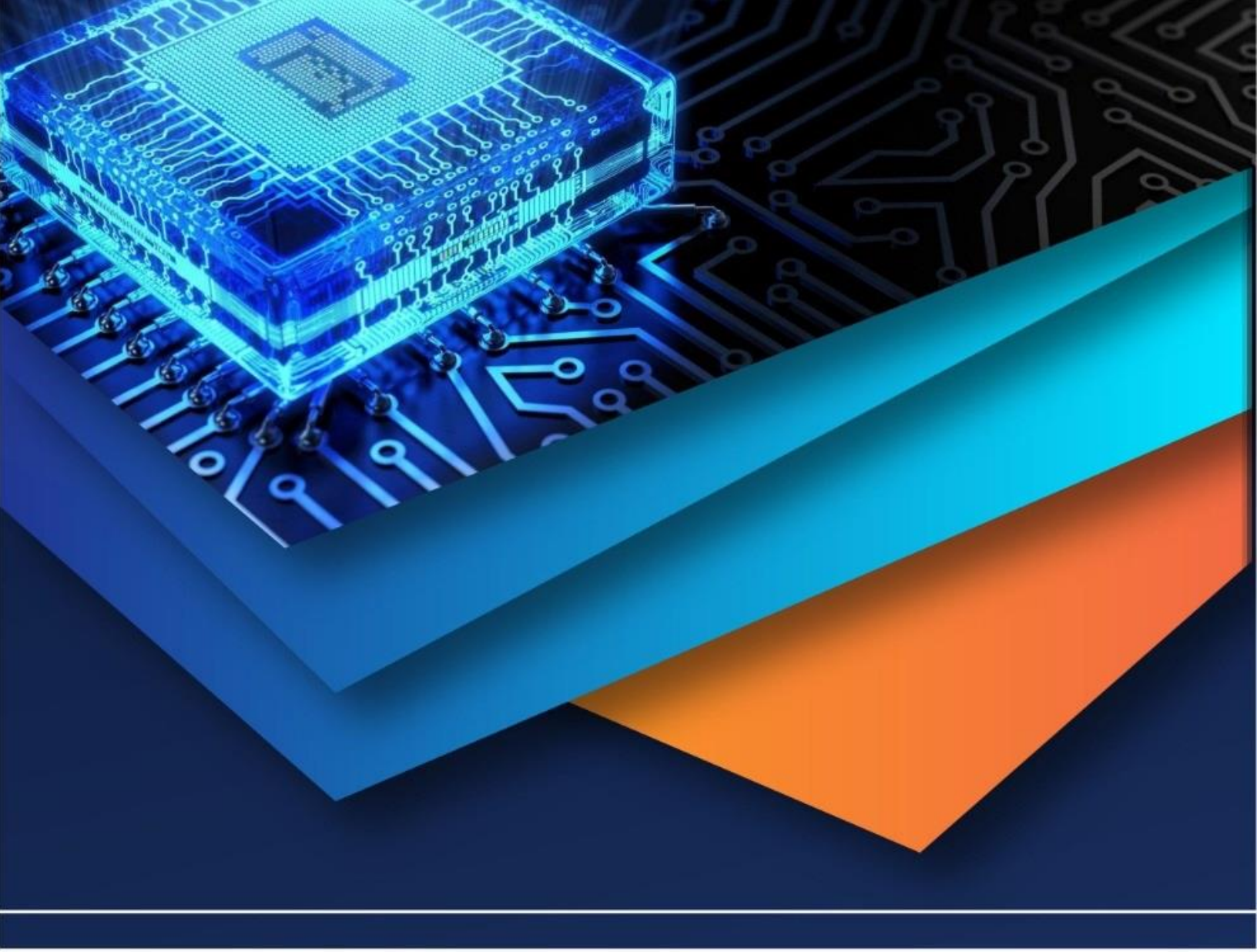

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