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Area and Power Efficient MSIC Test Pattern Generation for BIST

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Abstract-This paper proposes a technique to generate the multiple test patterns varying in single bit position for built-in-self-test (BIST). The conventional test patterns generated using LFSR have an absence of correlation between consecutive test vectors. So, in order to improve correlation between the subsequent test vectors, test patterns were produced using binary to thermometer code converter. The methodology for producing the test vectors for BIST is coded using VHDL and simulations were performed with ModelSim 10.0b. 100% fault coverage is achieved with less number of test patterns. The Area utilization, power and delay report were obtained with Xilinx ISE 9.1 software. The area reduction of 62%, power reduction of 13% is achieved while generating test patterns using binary to thermometer code converter when compared with the patterns generated using Reconfigurable Johnson counter and LFSR.
Keywords-Built-in-self-test (BIST), Test Pattern Generator (TPG), Multiple Single Input Change Vector (MSIC), Linear feedback shift registers (LFSR), Thermometric code.

I. INTRODUCTION

Testing plays a crucial role in any kind of production. The results of the testing indicate whether the necessary specifications and requirements of the final product are satisfied. Testing is a fundamental element in VLSI circuits due to the occurrence of imperfections. In mass production, every chip is subjected to manufacturing testing because defects might be caused by material defects, malfunctions of equipment and design errors. External testing is performed by automatic test equipment (ATE). ATE realizes the test by transporting and applying the test patterns and by evaluation of responses which are transported back to ATE. The skilful approach is to reduce the cost and time required for testing. Internal testing is performed using Built-In-Self-Test (BIST). BIST performs testing, every time before they start-up. Built-in-self-test (BIST) technique is used to inspect the standard of VLSI circuits. BIST is used to curtail the complication in testing the circuits. BIST approach incorporates the experimentation on the circuit that is to be tested. BIST logic is comprised of pattern generator for generating the test patterns, circuit under test on which the test is performed and response analyzer to report the flaw. For the purpose of pattern generation, automatic test pattern generator is used. The test patterns generated using ATPG is exercised on the circuit to determine the presence or absence of the fault at some location of the circuit. The former BIST architecture uses LFSR for producing the test pattern. The shortcoming of producing patterns using LFSR is enormous toggling in CUT [1], which leads to unnecessary power dissipation. A qualitative survey on various low power testing techniques and its methodology has been explained in [2]. Low-power external testing techniques and Low-power BIST methodologies to manage the problems occurring with power were categorized. In order to curtail the subsequent test transition, the scan chains are ordered and then reordered. During the test cycle some cells will be ordered and then scan chain will be reordered to reduce the number of transitions [3]. The demerits of this technique were excessive power dissipation and reduced life time. Girard et al. analyzed the energy reduction using simulated annealing algorithm [4]. Wang and Gupta employed two distinct LFSR with varying speed to shrink the changeover of input bits [5]. Corno et al. developed a test pattern generator for minimizing the power requirement in combinational circuits [6]. The input clock pulses to the LFSR were adjusted for minimizing the power. Rather using single clock pulse two distinct clock pulses were produced [7]. The data path consists of module with larger size and results in increased complexity. So in [8] the deterministic patterns have been produced for the purpose of testing data paths. In [9] Bonhomme et al introduced the gating of clocks to minimize the power dissipation. The first clock controls the odd scan cell and the next clock pulse controls the even scan cell. The construction of two non overlapping clock pulses becomes a hectic task. Laoudias.C et al in [11] constructed the ring generator for the purpose of producing test vectors. The results obtained are compared with the forecasted result. S. Bhunia et al. in [11] placed additional transistors at the ground path to obstruct the toggling of bits at the input. In order to curtail the power dissipation partial gating is proposed in [12]. The rest of the paper is organized as follows: In Section II, the Existing Methodology is presented. In Section III, the Proposed Methodology is presented. In Section IV, the simulation results and analysis is presented. Conclusion is given in Section V.

II. EXISTING METHODOLOGY

The Existing technique generates the test pattern using Johnson counter and the seed vector. Reconfigurable Johnson counter generates the Johnson vector and Linear Feedback Shift Registers generate seed vector. Test patterns were generated by performing Exclusive-or operations between Johnson counter and seed vector [14]. The vectors obtained were applied to the scan chain.

A. Generating Test Vectors

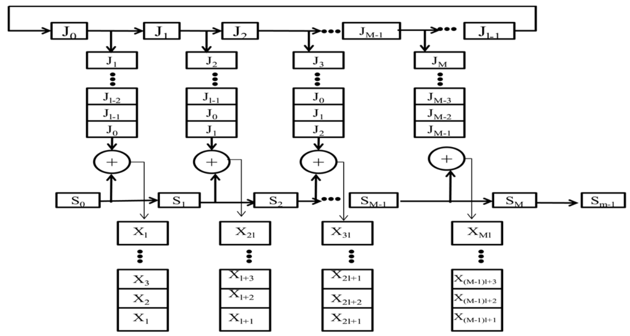

Fig.1 MSIC pattern generation [14]

Let us consider m primary inputs, M scan chains and *l* scan cells. Fig.1 shows pattern generation technique for BIST. The seed vector is produced using LFSR with the primitive polynomial, and the Johnson vector is produced using 8-bit Johnson counter. During the first clock cycle, the Exclusive-or operation is performed between Johnson vector and seed vector and the results obtained were applied to the first scan cell in the scan chain. For the next clock cycle the toggled result corresponding to former flip flop is feedback as an input. The Exclusive-or operation is performed between the Johnson vector generated in second clock cycle and seed vector generated using primitive polynomial. The result corresponding to the second clock cycle was applied to the second scan cell in the scan chain. The procedure is repeated by performing the Exclusive-or operation between Johnson vectors and Seed vectors until the required test length is obtained.

B. Reconfigurable Johnson Counter

Reconfigurable Johnson counter is utilized to produce the Johnson vectors. In case of Johnson counter, the toggled result corresponding to former flip flop is fedback and Reconfigurable Johnson counter operates in three modes.

1) Initialization: Reconfigurable Johnson counter is initialized by setting the value of RJ_Mode to 1 and Init to 0. The CLK2 is clocked until the flip flops are initialized to a known value.

2) Circular Mode: The circular shift operation can be performed by assigning the values of Init and RJ_mode to 1.

3) Normal Mode: The select input of the multiplexer RJ_MODE is assigned to the value 0. The Q_8 output corresponding to D_8 flip flop is fedback.

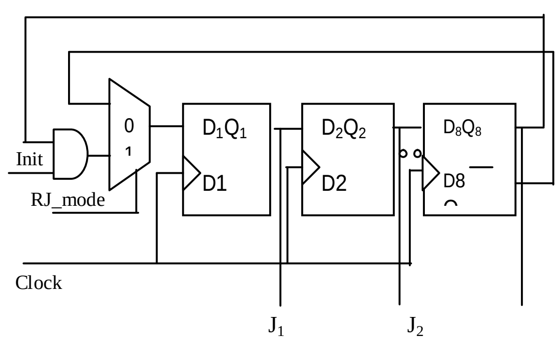

Fig.2 Reconfigurable Johnson counters [14]

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III. PROPOSED METHODOLOGY

Area, Delay and Power are the challenging parameters in VLSI. The need for the portable devices is increasing rapidly. In order to have better optimization, the patterns were generated using binary to thermometer code converter. The produced patterns were tested on the circuit under test. The response obtained is compared with the known result to verify the correctness of the circuit. The test patterns generated were applied on multiplier circuit. The exact functioning of the circuit is verified by comparing with the known result. The patterns produced have the ability to detect the faults in a combinational circuit. The circuits are designed to generate the test patterns with less number of toggles between successive bits. The subsequent test transitions between the successive vectors were curtailed to minimize the power requirements.

A. Binary To Thermometer Code Converter

The test patterns were generated using binary to thermometer code converter to have reduced number of transitions with minimum gate count. The block diagram of binary to thermometer code converter is as shown in Fig.3. Three bit binary up down counter is used. The results of binary counter are converted into thermometer code using binary to thermometer code converter. The eight bit results produced from binary to thermometer code converter were tested on multiplier circuits. Fig. 4 indicates the logic diagram corresponding to binary to thermometer code converter.

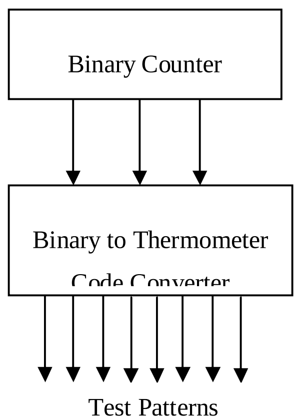

Fig.3 Block Diagram of Binary to thermometer code converter

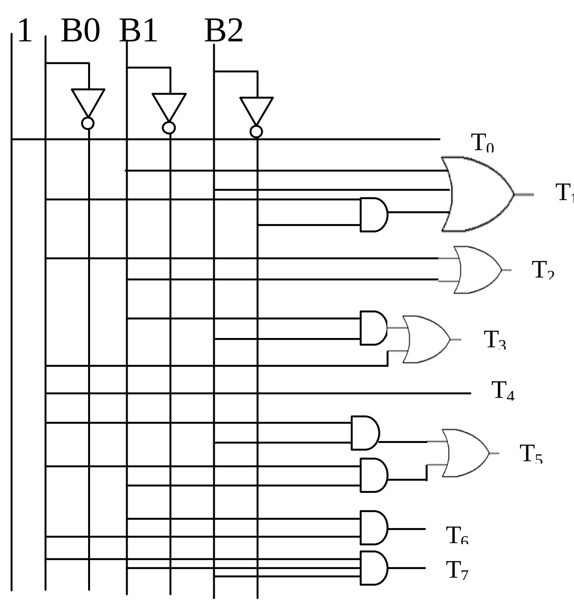

Fig. 4 Logic diagram of binary to thermometer code converter

IV. SIMULATION RESULTS AND ANALYSIS

The test pattern generation for BIST is implemented using front end ModelSim 10.0b software and Xilinx ISE 9.1 software. The design is coded in VHDL and simulations were performed using ModelSim 10.0b software. The test patterns generated were tested on 4*4 Multiplier circuit. The analysis of area, delay and power are performed using Xilinx ISE 9.1 software.

A. Binary To Thermometer Code Converter

The result of binary to thermometer code converter is as shown in the Fig. 5. For each binary value, corresponding thermometer code is generated.

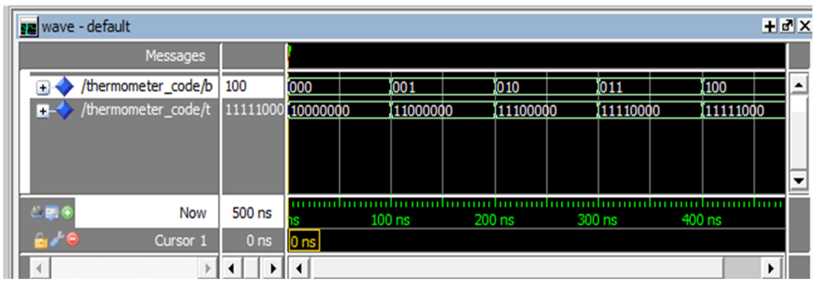

Fig. 5 Binary to thermometer code converter

B. Testing Of Multiplier Using Binary To Thermometer Code Converter

The simulation result for testing multiplier circuit by applying test patterns generated using binary to thermometer code converter is shown in the Fig.6. count_out is the required test pattern. The output signal ref_out is the expected result and test_out is the output after injecting the test patterns. Here v is assigned with value “000110” indicating s-a-0 fault at fourth input bit of multiplier. When the vectors of ref_out and test_out are equal, then the pattern is incapable of detecting the fault at that position. Here the pattern “11111000” is applied on the multiplier circuit and the expected result of the multiplier circuit ref_out is “01111000”. But the result obtained after injecting s-a-1 fault at fourth input bit of multiplier circuit, test_out is “01110000”. The results of ref_out and test_out obtained by applying the pattern “11111000” are different. Hence the pattern “11111000” is capable of detecting s-a-0 fault at fourth input bit of multiplier.

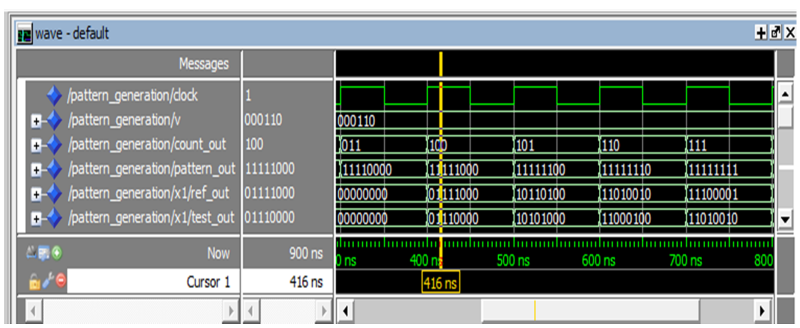

Fig. 6 Testing of Multiplier using binary to thermometer code converter

C. Analysis Report

In [15], the test patterns were generated using gray counter, decoder and accumulator architecture. For implementing the testing on multiplier circuit using gray counter, decoder and accumulator architecture 142 gates were required. The total power estimation is 36.75 mW and the delay is 4.116 ns. The total number of patterns required to cover all possible stuck-at-faults is 10. Analysis of area, power, test length and delay for generating test patterns using binary to thermometer code converter is as shown in Table1. For implementing the testing on multiplier circuit using binary to thermometer code converter 120 gates were required. The total power estimation is 36.35 mW and the delay is 2.780ns. The total number of patterns required to cover all possible stuck-at-faults is 8. In order to differentiate the various test pattern generation techniques for BIST, the comparison table is reported in Table.1. The comparison chart of Area overhead, Power, Test length and Delay for the pattern generation using reconfigurable Johnson counter and binary to thermometer code converter is shown in Fig.4.

TABLE 1

COMPARISON TABLE

	Reconfigurable Johnson counter & LFSR[14]	**Binary to Thermometer Code Converter**
Area (Gate count)	312	120
Power (mW)	41.79	36.35
Test length	12	8
Delay (ns)	11.171	2.780

V. CONCLUSION

The test pattern generation for BIST to attain 100% fault coverage using binary to thermometer code converter is proposed. Three bit up down counter and binary to thermometer code converter have been developed to generate the test patterns with optimized area, delay, power and test length. The single input change patterns generated to improve the correlation between the successive test patterns reduce power requirements. This technique to generate the multiple test patterns varying in single bit position for BIST schemes is coded using VHDL and simulated using ModelSim 10.0b. The gate count and power consumption of the test pattern generation were analyzed using Xilinx ISE 9.1 software. Area reduction of 62%, delay reduction of 75%, power reduction of 13% and test length reduction of 33% are achieved while generating test patterns using proposed binary to thermometer code converter.

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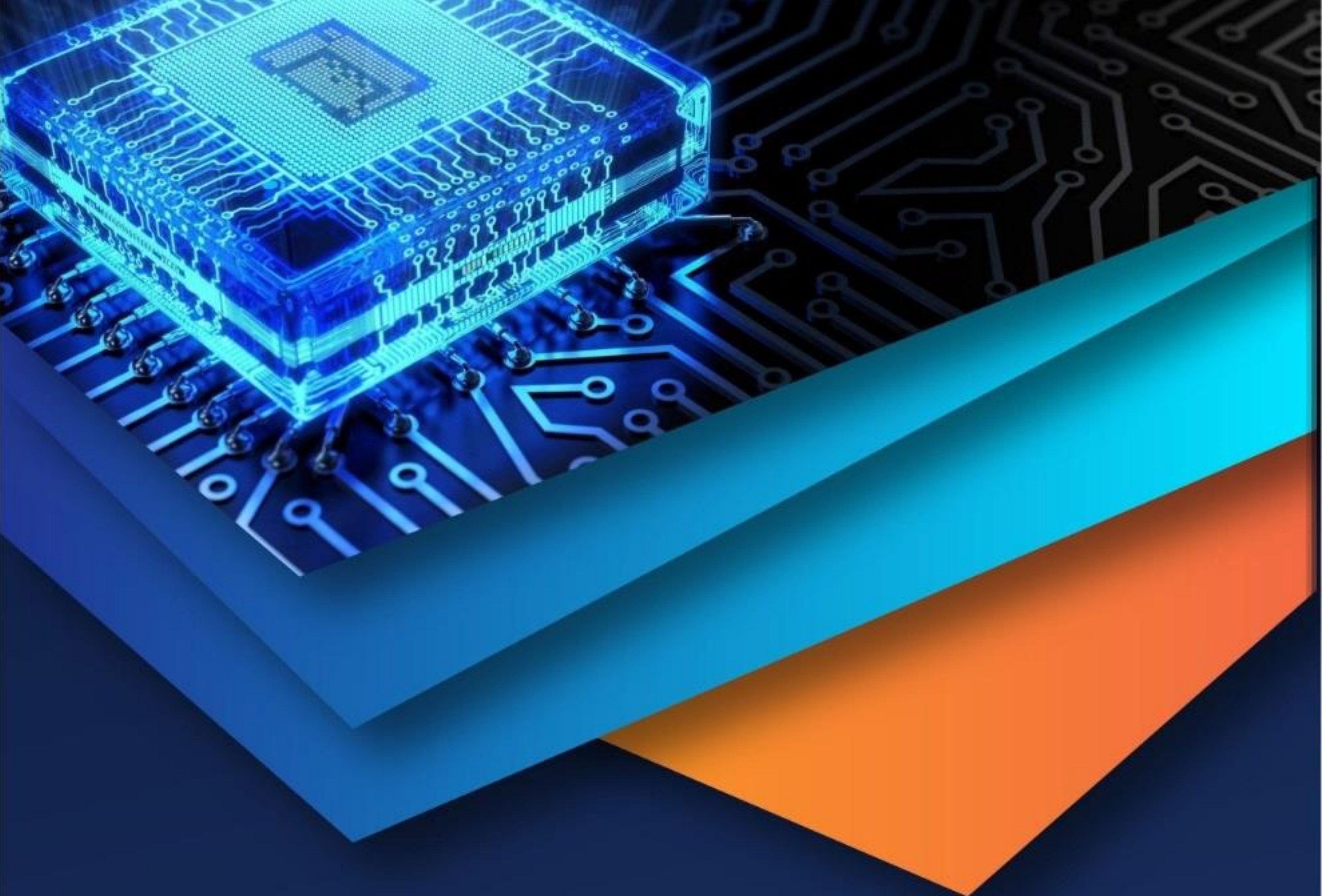

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