iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 7 **Issue:** IV **Month of publication:** April 2019

DOI: https://doi.org/10.22214/ijraset.2019.4630

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.177
Volume 7 Issue IV, Apr 2019- Available at www.ijraset.com

Design and Testing Parallel Prefix Adders using Reconfigurable LFSR in FPGA

Soujanya Munnur[1], Konda Deepika[2]
[1, 2]*Electronics and Communication Engineering Department, JNTUH University*

Abstract: ***The main criteria of this paper is to design Reconfigurable Linear Feedback Shift Register (LFSR) for very large scale integration(VLSI) of Integrated Circuit(IC) testing .Comparability to the Automatic Test Equipment(ATE) the Logic Built In Self Test(LBIST) has take into popularity. This logic built which helps in built testing with the help of additional hardware construction indoors the circuit. Thus doesn't contains the test pattern but they generate by the testing circuits. By this can out down the testing cost substantially. LFSR is mostly used as a test pattern generate for IC testing. To improve the fault coverage of IC testing in logic BIST using Reconfigurable LFSR. It is configurable to generate the maximum length of the pattern depending on the feedback polynomial that provide as per requirement. In this paper, the proposed reconfigurable LFSR of four structural represented in modular, standard, hybrid and complete LFSR is simulated in different sizes (8,16,32,64) in Xilinx Spartan 3E with an application of Parallel Prefix Adder (konge stone) of 16-bit.This simulation results shows the increasing of speed***

Keywords: Terms-PRPG, Reconfigurable LFSR, Primitive Polynomials, Parallel prefix adder(konge stone),speed

I. INTRODUCTION

The design of the IC has became complicated for vlsi chip in testing. The advance in fabrication technologies, it has become exceedingly authoritative and the faults that occur such as stuck at faults and bridge faults are difficult to test in VLSI. This lead to a new technology of testing called Logic Built in Self Test. LBIST in system-on-a-chip (SoC) i.e., inbuilt testing that used to test the quality of structural integrity. It supply fault coverage of 90 to 95 % or more, using only a clock and a "test-mode" signal as inputs. Outputs are simplified since a good/bad test can be simplified to a single output signal [1]

LBIST is one that can be used for several applications to Design For Test (DFT). It is one of legion types of built-in self-test. It typically tests a wide range of logic structures wired in a highly randomized manner, and it reduces more complex test circuitary testing but it also reduces the cost of testing.

The structure of Logic BIST, the PRPG acts as a test pattern generator and MISR acts as the output response analyzer . The test pattern that has provided by the PRPG are consider as input to the circuit under test and the corresponding MISR output are compared with golden signature by using comparator to check wheather circuit is fault free or not.[2]

This LFSR uses D-flipflops, XORs and multiplexers (MUXes). In contrast to the traditional scheme with D flip-flops and XORs only, this structure uses a MUX at the output of the XOR gate. The presence of the XORs in all positions with the presence of the MUXes would make the signals of the MUXes be variable coefficients of the characteristic equation. Hence, inserting the multiplexers makes the LFSR reconfigurable.[3]select

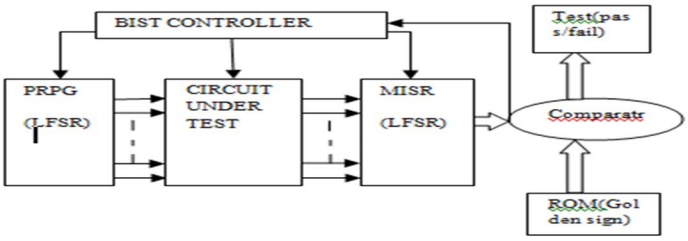


Fig:1 LFSR Architecture

This paper is an n-bit reconfigurable LFSR that generates sequence of maximum length or less has been implemented. This proposed design provides flexibility in both the feedback and size.

In this design we can insert XOR gate at required place by the primitive or non-primitive polynomials[4]. The multiplexers are added to load the initial values. It simulated and synthesized using verilog on Xilinx Spartan3E for implementation.

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.177
Volume 7 Issue IV, Apr 2019- Available at www.ijraset.com

II. ESCRIPTION OF RECONFIGURABLE LFSR

The arrangement of taps for feedback in an LFSR can be expressed in finite field arithmetic as a polynomial mode where each clock signal is advanced. This means that the coefficients of the polynomial must be 1's or 0's. This is called the feedback polynomial or characteristic polynomial[5]. The degree of polynomial 'n' over the Galois Field (GF)(2) define internal structure of an n-bit LFSR. [7]

Characteristics polynomial is given by

$m(x) = 1+_{h1}x+h^2x^2+\ldots\ldots\ldots h_{n-1}x^{n-1}+h_nx^n$

Different types of LFSR includes 1)Standard LFSR 2)Modular LFSR 3)Complete LFSR 4)Hybrid LFSR

A. Standard LFSR

Standard LFSR is also called as external Xor LFSR. To provide a new output the concatenation of feedback polynomial to represent the tap position. Then the output of n flipflop is given as the Xor input to provide single output.

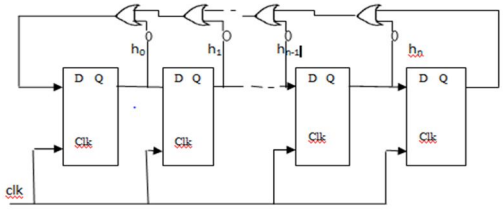


Fig:2 n-bit Standard LFSR

B. Modular LFSR

Modular LFSR is also called as internal Xor LFSR. This provides the same as the established one,which contains only one Xor gate connection of tap in feedback polynomial between 2flipflop(ff) .In this the o/p of the every ff is fed immediately to the next ff, Modular LFSR is faster execution than standard LFSR which can generate maximum length of sequence 2n-1.

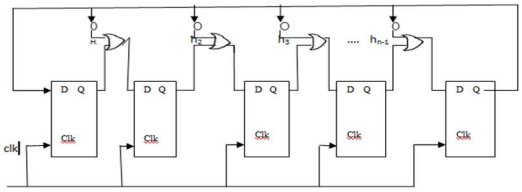


Fig:3 n-bit Modular LFSR

C. Complete LFSR

Complete LFSR can be constructed from standard LFSR by inserting an XOR gate into the last stage of the LFSR, and a NOR gate with n-1 inputs is used as a zero-detector. Thus a complete LFSR could generate 2n patterns for a primitive polynomial feedback. LFSR has included all the zeros into a clocked state condition.

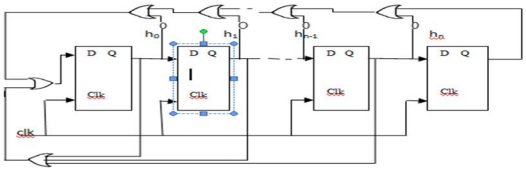


Fig:4 n-bit Complete LFSR

D. Hybrid LFSR

In this the number of Xor is reduced comparing to the standard and modular LFSR. Architecture of Hybrid LFSR. from 'm' XOR gates to (m-1)/2 in hybrid form of m(x) and q(x) terms of a polynomial over GF (2) f(x) = 1+m(x) +q(x) and there exists an j interger of $q(x) = x^j m(x)$, where j<1.

$f(x) = 1+m(x)+x_jm(x)$

It makes use of a feedback structure from j^{th} output stage. A modular structure is utilized from first to $(j-1)^{th}$ registers. Hybrid LFSR is more efficient in terms of area, number of gates and speed.

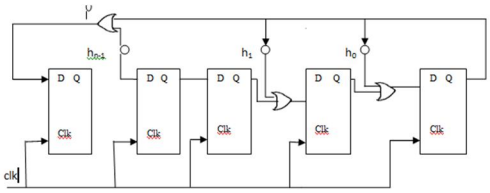


Fig:5 n-bit Hybrid LFSR

III. PROPOSED METHOD

This paper is about the design of a N-bit reconfigurable LFSR which generates 2^{n-1} states includes all the values of zero. This programmable LFSR increases the randomness of the output. By this insert of Xor gate between the flipflop(ff) which provides the PN sequence and the presence of the multipliers makes the structure reconfigurable[8].

In this ,the standard, modular, complete LFSR's as well as the hybrid LFSRs are made programmable for n-bit. The complete LFSR uses the design structure of standard LFSR except an additional circuitary is added. This circuitary consists of NOR gate which take all the ff output as input and pass through an Xor gate. The output of the Xor gate is given as feedback in the reconfigurable LFSR. By this we can generate all the 2^{n-1} exhaustic pattern and improve fault coverage[6]. Hybrid LFSR reduces number of Xor gate by this we can reduce the energy by 64% when the d-ff is idle. And it can increase the accuracy of the testing.

In this paper, the parallel prefix adder are tested i.e., konge stone of 16-bit with programmable n-bit reconfigurable LFSR. This parallel prefix adder are faster adders and used for high performance architecture structure in industries. This can reduce the number of shifting process and increases the speed. Parallel prefix adders will reduce the power consumption rather than other adders.

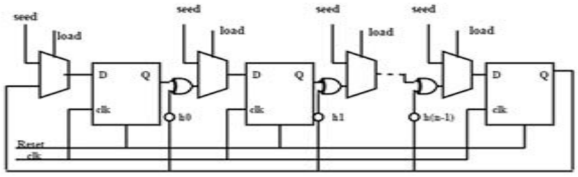


Fig:6 Proposed Architecture of n-bit Reconfigurable LFSR

IV. SIMULATION AND SYNTHESIS RESULTS

The proposed design of Reconfigurable LFSR is described in Verilog HDL, simulatedbin 17.4 RTL and software tool used for synthesis in FPGA in Xilinx ISE. The figure shows below,the results after simulation of 64-bits of standard LFSR, modular LFSR,complete LFSR and hybrid LFSR. The simulation results of 64-bit in 4 different modules i.e., standard LFSR, modular LFSR, complete LFSR and hybrid LFSR as shown in the figures.

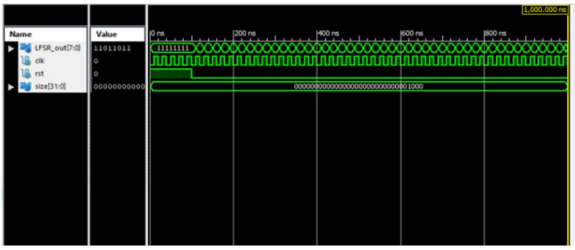


Fig:7 Simulation results of standard LFSR of 64-bit

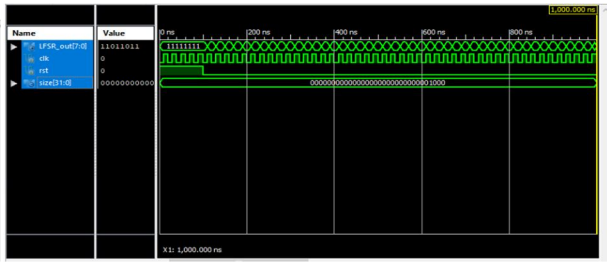


Fig:9 Simulation results of complete LFSR of 64- bit

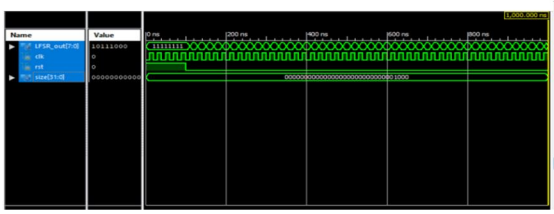


Fig:8 Simulation of modular LFSR of 64-bit

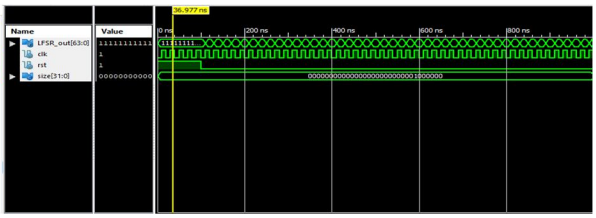


Fig:10 Simulation results of hybrid LFSR of 64-bit

In this paper ,the IC testing of Parallel prefix adder i.e., Konge Stone (KS) of 16-bit is tested with reconfigurable LFSR The simulation results of 16-bit as shown in below figure.

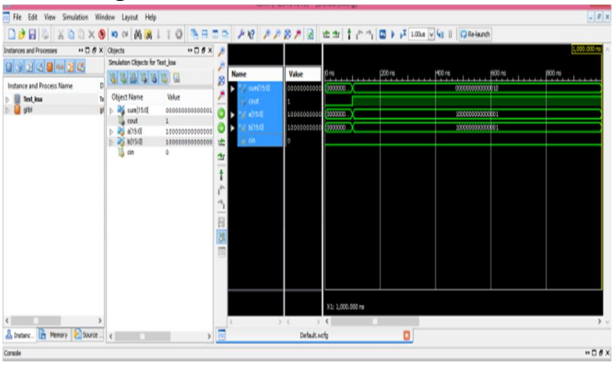


Fig:11 Simulation result of 16-bit KS

The implementation of Reconfigurable Hybrid LFSR is most efficient than the starndard LFSR in terms of nuber of gates ued and had greater speed of execution.

Parameter Analysis for different 16-bit LFSR

PERFORMANCE PARAMETER	STANDARD	MODULAR	COMPLETE	HYBRID
NUMBER OF SLICES	9	9	11	9
NUMBER OF FLIPFLOPS	16	16	16	16
DELAY	1.997NS	2.342NS	3.968NS	2.106NS
SPEED(GHZ)	1.153	1.373	0.789	1.188
POWER	8.31	8.11	8.68	8.13
MAX FREQUENCY OF OPERATION(MHZ	378.62	509.61	211.75	378.65

Parameter Analysis for different 32-bit LFSR

PERFORMANCE PARAMETER	STANDARD	MODULAR	COMPLETE	HYBRID
NUMBER OF SLICES	18	19	20	16
NUMBER OF FLIPFLOPS	32	32	32	32
DELAY	1.998NS	2.535NS	4.134NS	2.342NS
SPEED(GHZ)	1.444	1.373	0.630	1.188
POWER	14.53	14.62	15.22	14.47
MAX FREQUENCY OF OPERATION(MHZ	368.68	509.67	244.78	378.65

Parameter Analysis for different 64-bit LFSR

PERFORMANCE PARAMETER	STANDARD	MODULAR	COMPLETE	HYBRID
NUMBER OF SLICES	37	39	41	37
NUMBER OF FLIPFLOPS	64	64	67	65
DELAY	2.021NS	2.536NS	5.072NS	2.535NS
SPEED(GHZ)	1.458	1.373	0.493	1.883
POWER	30.47	30.09	32.33	30.53
MAX FREQUENCY OF OPERATION(MHZ	368.68	509.61	222.52	378.65

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.177
Volume 7 Issue IV, Apr 2019- Available at www.ijraset.com

V. CONCLUSION

This paper represents a reconfigurable Logic BSIT structure where all the components in the design to be programmable. This design that which self-test the circuitary with varying configurable. The PRPG and MISR structure made reconfigurable by adding multiplexers and improve the flexibility in the position of of tap insertions which determines the feedback polynomials and the patterns generated. For MISR, XOR gates were added to every flip-flop inputs depending on the number of primary outputs of the CUT. Comparator and ROM were also designed to compare and store any number of inputs with varying size.

The main objective of this project is to design the Reconfigurable n-bit LFSR By using the standard LFSR, modular LFSR ,complete LFSR and hybrid LFSR's are made to be programmable. This can reduce the number of shifting process and increases the speed. By using the design of the Reconfigurable LFSR the Parallel Prefix Adder is testing. The Parallel Prefix Adder will reduce the power consumption rather than the other adders. The main criteria of this project is to increase the speed, reduce the power consumption and also delay.

REFERENCES

[1] Ramesh Bhakthavatchalu, Deepthy G R, Sreenivasa Mallia S, HariKrishnanR, ArunKrishnan, Sruthi.B, "32-bit Reconfigurable Logic-BISTDesign Using Verilog for ASIC Chips," Recent Advances in IntelligentComputational Systems (RAICS), pp. 386–390, 2011.

[2] Ramesh Bhakthavatchalu, Sreeja Krishnan, Vineeth V, Nirmala DeviM., "Deterministic Seed Selection and Pattern Reduction in LogicBIST," VLSI Design and Test, 18th International Symposium on, 2014.

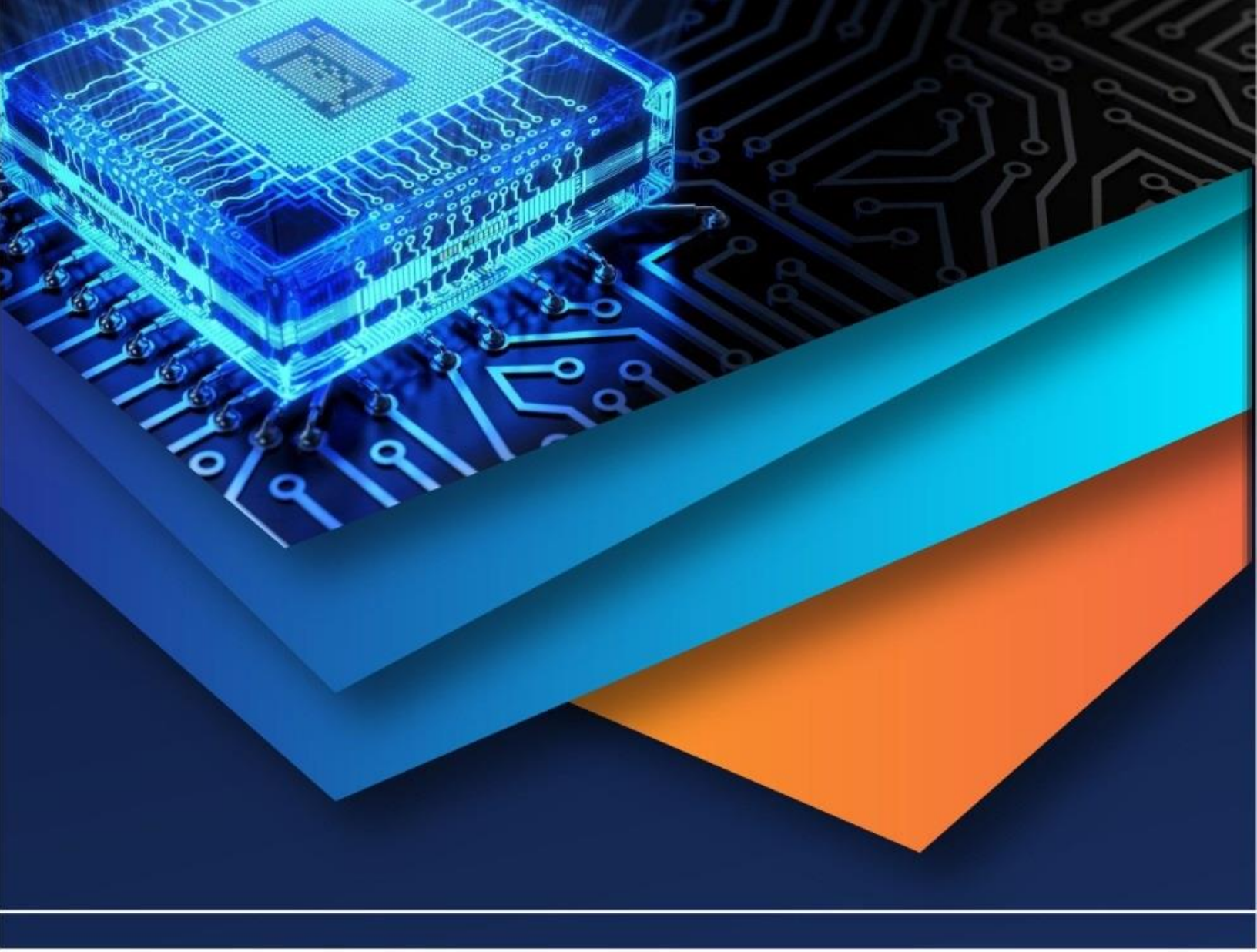
[3] Nisha Haridas, M. Nirmala Devi, "Efficient Linear Feedback ShiftRegister design for Pseudo Exhaustive Test Generation in BIST", 20113rd International Conference on Electronics Computer Technology,vol. 1, pp: 35-354, 2011

[4] Amit Kumar Panda, Praveena Rajput, Bhawna Shukla, "FPGA Implementationof 8, 16 and 32 Bit LFSR with Maximum Length FeedbackPolynomial Using VHDL," Communication Systems and NetworkTech-nologies (CSNT), 2012 International Conference on, pp. 769 –773, 2012.

[5] Lama Shaer, Tarek Sakakini, Rouwaida Kanj, Ali Chehab; AymanKayssi, "A low power reconfigurable LFSR," 2016 18th MediterraneanElectrotechnical Conference (MELECON), pp. 1–4, 2016.

[6] Devika K N and Ramesh Bhakthavatchalu'Design of Reconfigurable LFSR for VLSI ICTesting in ASIC and FPGA'International Conference on Communication and Signal Processing, April 6-8, 2017, India

[7] V.Nagarajan, "FPGA Based Reconfigurable Measurement Instrument with Functinality defined by user" International conference on Advances in Engineering and Technology, EGS Pillai Engineering College, may 2011.



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY