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Optimal Design of Reconfigurable Arbiter Algorithm used in On-Chip S.O.C.

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***Abstract:** This paper presents reconfigurable arbiter is placed in arbitration to the enhancement of the data transfer and reduce delay, latency and bandwidth b/w master core and slave cores. It provides high performance in real-time application on-chip S.O.C. The performance of arbitration in individual process was the earlier stages of the arbitration technique. In the processing of arbitration technique in a single step-by-step process the transfer of data from one multiple master to multiple core's causes delays. The simulations were done using XILINX 14.5.*
***Keywords:** Arbiter, Technique, Cyclic, S.O.C., Reconfigurable, Xilinx Tool 14.5 version.*

I. INTRODUCTION

The reconfigurable arbiter is important and plays a major role in the performance and execution of multiple tasks at a partial interval of time. Arbiter is a component to which multiple master and multiple slaves are connected. Nowadays developing silicon chip industry has entered in multi-million gate chips. The 5thgeneration process is over-a-head of industries to design chips in multi-functionalities on one board. The multiple functionalities are nothing but the execution of applications in a single processors w/o any interruption in on system-on-chip (SOC). This generation has great handling of multiple tasks at a short interval of time. The multiple tasks mean having a number of i/p (inputs) slots to assign to o/p (outputs) slots in b/w single arbiter controls the whole process and work simultaneously on them. The topologies of previously shared buses are (1) static priority, (2)time division multiple access, (3)Round Robin, (4)lottery bus architectures. These topologies executing order is step-by-step manner. The data which request by the master is to travel along and reach its own path which is suitable to it. Till that annual time process of execution increases bandwidth, latency, delay, and area. The main reason for the proposal of reconfigurable arbitration is co-ordination of topologies in a single arbiter. These arbitration technique helps to increase rapidly data transfer by selecting a suitable topology by priority selection based method. By this method, the area, bandwidth, latency, and delay will be reduced. This runs automatically by arbitration technique. The Group of topologies present in arbiter has importance to each other. We describe it one by one.

Selection Method	Arbitration
00	Static Priority
01	T.D.M.A
10	Round Robin
11	Lottery Bus

TABLE 1: Priority selection method.

The priority selection based method arbitration is a scheduling mechanism. Each arbitration is assigned to a priority value.

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II. BLOCK DIAGRAM

Block diagram of a Reconfigurable Arbiter architecture representation is shown in Fig 1. Here a Block Diagram is the design that is an integrated circuit design functional block. The main important factor is priority selection method used for data transfer.

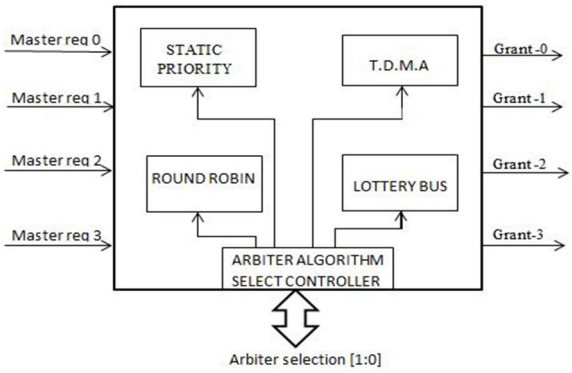

Fig 1: Reconfigurable arbiter architecture.

III. LITERATURE REVIEW

We have discussed some of the issues related to the design of S.O.C with regard to the inter process communication of Various bus architectures and protocols have been review[1]. Currently, on-chip communication networks are mostly implemented using shared interconnects like buses [2]. Hence in the future research, it is focused to design an arbiter that dynamically schedules the requests by various masters occurring simultaneously and thus improving the performance of a multiprocessor with respect to latency and bandwidth[3]. If some masters make little use of the bus it also provides a more fair distribution of bandwidth to the remaining masters[4]. The bandwidth regulator utilized to dynamically monitor the bus communication and thus can precisely control the bandwidth allocation[5]. A multi-processor system-on-chip includes embedded processors, digital logic and mixed-signal circuits combined into a heterogeneous multiprocessor[6]. This mix of technologies creates a major challenge for MPSOC design teams[7].

IV. RELATED WORK

Arbitration: it is a mechanism is to ensure one master request to access one slave at one time.

A. Static Fixed Priority Algorithm

The static fixed priority based arbitration is common to schedule.it will select the highest priority grant will be executed. If this process continues in this way its lead to starvation of lowest priority elements. The advantages of this technique are implantation easy and low area. Disadvantage if masters with high priority request frequently it will lead to starvation [1].

B. Time Division Multiple Access (T.D.M.A)

The Time division is an arbitration technique which has a cyclic (round) wheel in which every slot is placed in a particular bit in a wheel. It divides wheel into no of timing slots. The request made by the master to particular M1slot is reserved and to move next slots until all sequential slots are completed. If it does not wait for any slot request it moves to next slot in a wheel. TDMA lend its time with the lowest priority only during idle time. The advantage of this to implement a few execution requests in a particular time [2]. The disadvantage of this misleads of data transfer instead of reserved slots moves to other slots and low bandwidth. If request opts by the master it granting occurs after travelling all the time slots completed and returns to its previous position.

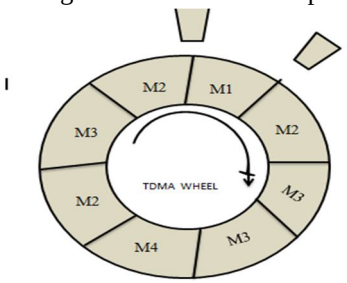

Fig.2: T.D.M.A Architecture.

C. Round Robin Algorithm

This type of algorithms works fast in data transfer. RR has a more efficient way of handling of random traffic in arbitration technique [3]. It can reallocate slots which were incomplete and keep forwarding request which is ready to take.it gradually decreases time and starvation among slots. The transfer length is short in RR and reduces delay, latency in a transfer of data. Among all the 3(three) algorithms R.R works more effectively. The fair arbitration has done in this algorithm. The request from the master core to slave core granting takes place with maximum access time and equal bandwidth achieved with limited transfer length. It doesn't wait for any slot whenever turn ends either unused or used moves to other components [4].

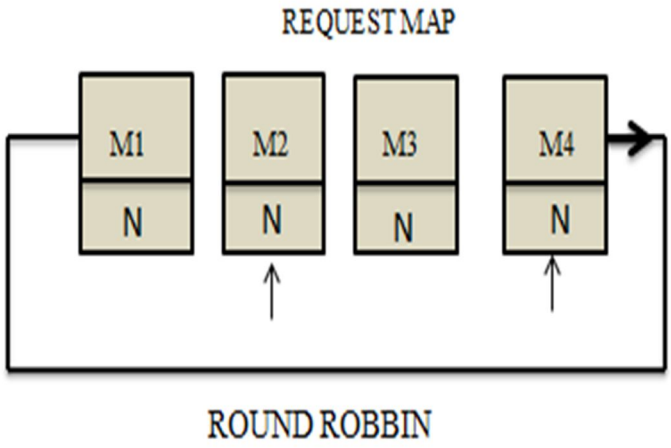

Fig 3: Round Robin Architecture.

D. Loterry Bus Algorithm

The algorithm depends upon lottery manager in which the number of the request is taken from masters such as r0,r1,r2,r3,r4 and they allot tickets to the requests such as t0,t1,0t2,t3,t4. The processing of ticketing which-ever it picks is granted from the slaves to master to transfer data [5]. which owned by lottery manager. It is a random number is generated which response to one of its ticket or almost near to ticket is having the highest priority to be granted likely. It is totally probability based distributions. It reduces delay (starvation) between master and slave [6]. The addition of request and tickets are done in random based generation method and granting is applied to it. The advantage of this algorithm FIFO (first-in-first-out) method which comes first serves to it [7].

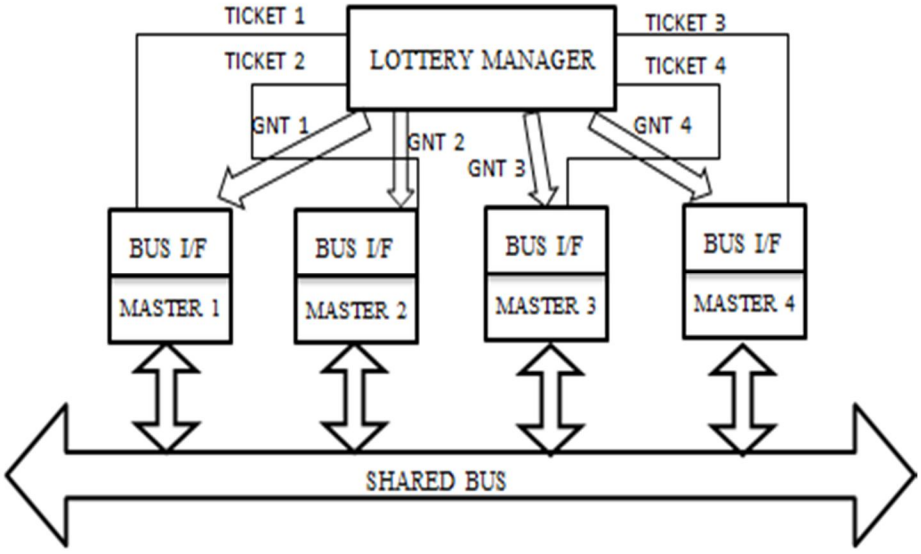

Fig 4: lottery Arbiter for shared Bus.

V. SIMULATION AND RESULTS:

The Reconfigurable arbitration proposed in this work is implemented using Verilog on Xilinx ISE tool of version 14.5. The simulation wave form results of arbitration is shown in the below waveforms.

Fig.5: simulation waveforms for static priority.

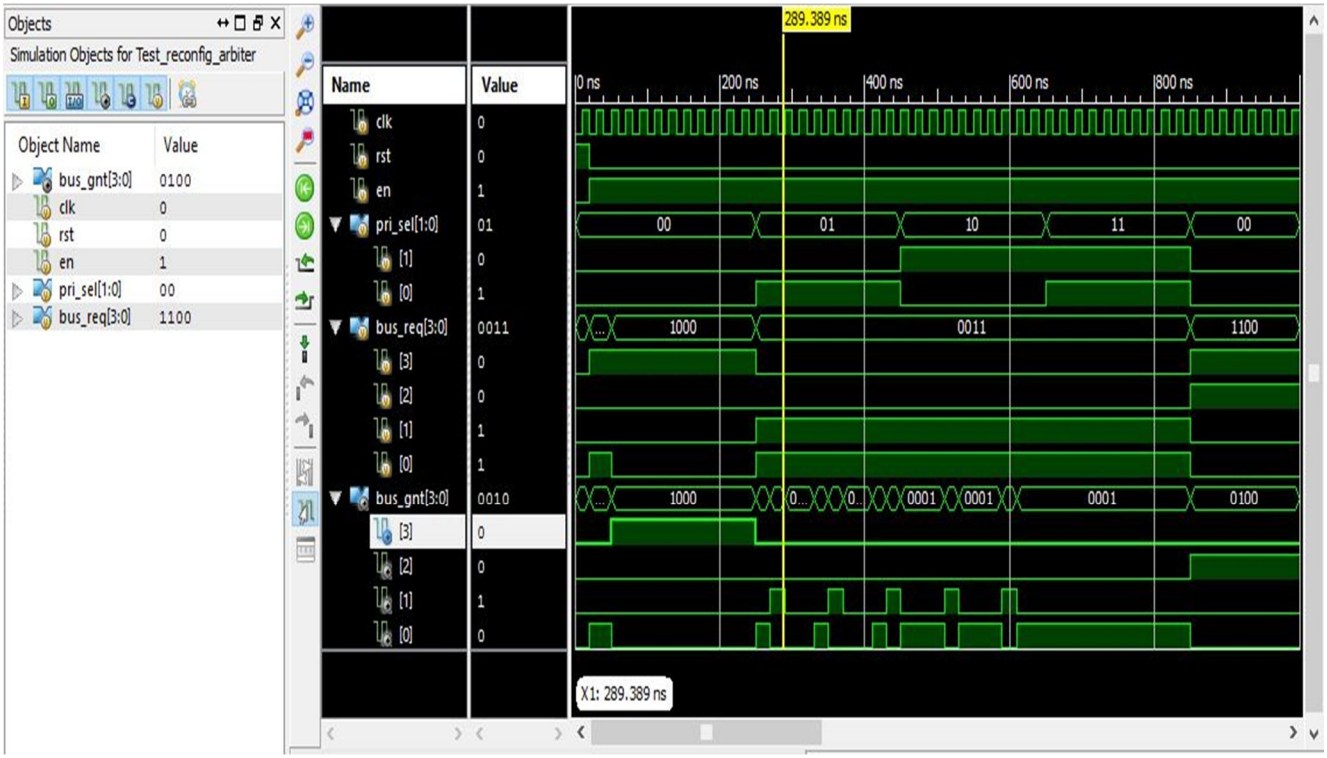

Fig.6: simulation waveforms for T.D.M.A.

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Fig.7: simulation waveforms for a round robin.

Fig 8: simulation waveforms for lottery bus.

TABLE 2: Area and delay for different techniques comparing with the reconfigurable arbiter

PARAMETRES	AREA				DELAY(ns)
	No of slices	No of LUT'S	No of IO'S	No of IOB'S	
Static priority	2 OUT OF 8672	3 OUT OF 17344	8	8 OUT OF 190	6.376
Time division multiple access	3 OUT OF 17344	6 OUT OF 17344	11	11 OUT OF 250	6.458
Round robin	7 OUT OF 8672	15 OUT OF 17344	11	11 OUT OF 250	3.590
Lottery bus	14 OUT OF 8672	27 OUT OF 17344	10	10 OUT OF 250	9.138
Reconfigurable arbiter	27 OUT OF 8672	52 OUT OF 17344	13	13 OUT OF 250	2.905

As we observed from the following table that reconfigurable arbiter has less delay and area.

VI. CONCLUSION

In this, we have come to know about reconfigurable arbiter and it uses. How effectively utilization of bus speed of data transfer. It's performances and it's working among critical traffic cyclic period. Handling of data to be transferred to it through priority selection method. And also compare the performance with various arbitration. I hope future work and research may depend upon various arbitrations that must reach requirements of the User and various techniques are obtained to be calculated.

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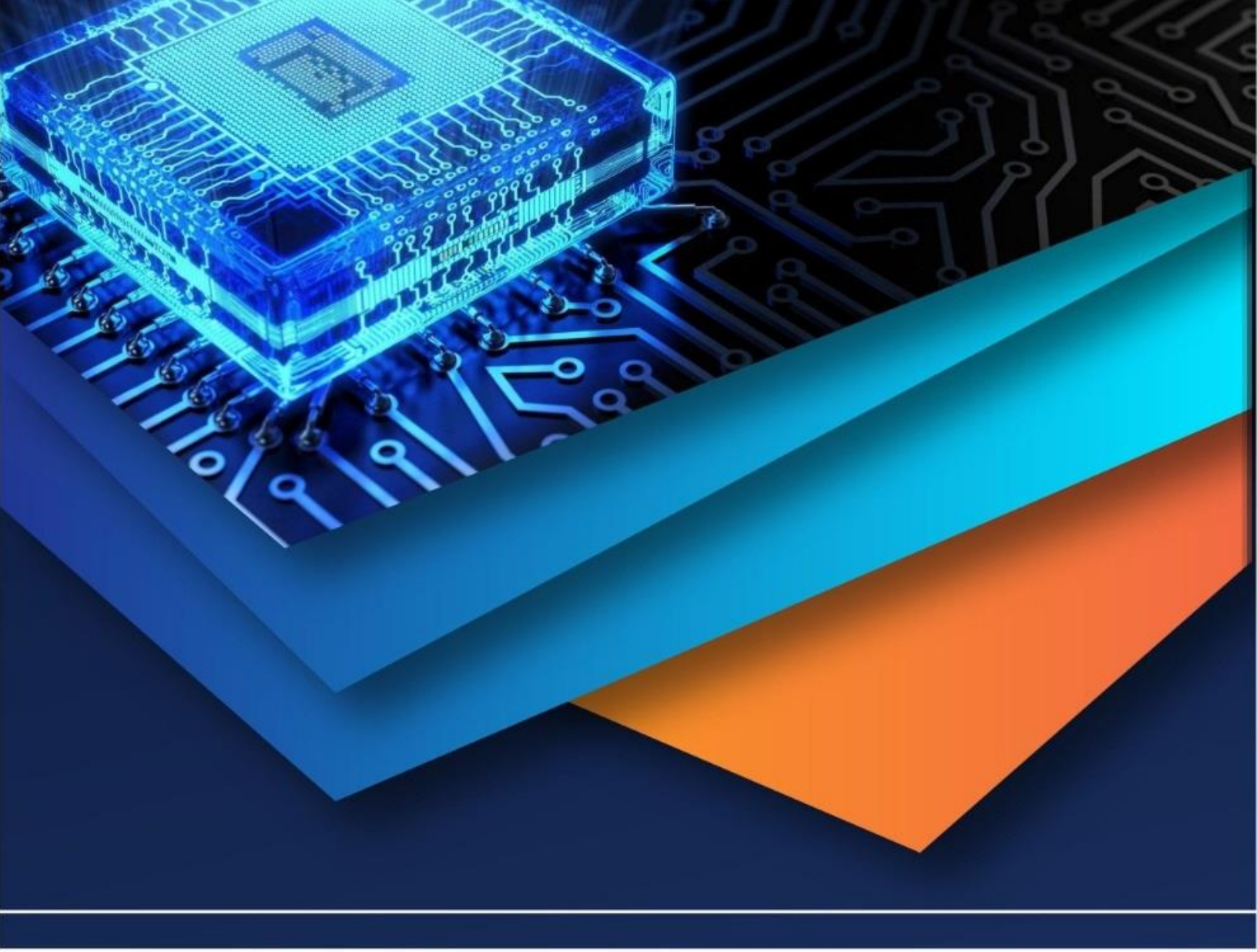

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