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Design and Simulation of Novel TG8T SRAM

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Abstract: ***Static Random-Access Memory (SRAM) has become a major component in many VLSI Chips due to their large storage density and small access time. SRAM plays a major role in the microprocessor world, but as the technology is developing day by day, leakage parameters and delay are the most common problems for SRAM cell which is in general designed for very low power application. Transmission gate is used to further reduce leakage current penetrating in the 8T SRAM cell. Comparative analysis is performed by using transmission gate. This project represents a method to design a variability aware SRAM cell. The proposed TG8T SRAM cell architecture is similar to standard 6T SRAM cell and the only exception is that they possess full transmission gates which replace an access pass transistor. Here an 8T SRAM is designed using transmission gate and its parameters (i.e. delay and power) are compared with the existing SRAM designs. This is performed using cadence virtuoso tool at 180nm technology.***

Keywords: SRAM, Transmission Gate, delay

I. INTRODUCTION

The handy devices such as hand held mobile devices and special digital assistants are gaining more attractiveness as well as making changes in every phase of our daily lives. On chip cache represent a major portion of the chip and is expected to increase further in both moveable devices and high-performance processors. The proposed TG8T SRAM cell architecture is corresponded to the standard 6T SRAM cell; the only exception is that they possess full transmission gates which replace an access pass transistor. Here an 8T SRAM is designed using transmission gate and its parameters (i.e. delay and power) are compared with the existing SRAM designs. This is performed using cadence virtuoso tool at 180nm technology.

II. PROPOSED DESIGN

TG8T SRAM uses differential operation and does not possess as much architectural changes except adding a PMOS in parallel with each access NMOS in conventional 6T SRAM cell shown by N3 and N4, by this we make it TG8T SRAM cell and such combination of both NMOS and PMOS is known as Transmission Gate. The transmission gates are used because when input signal is applied to transmission gate, it passes either Strong 0 or Strong 1 unlike imperfect switches (NMOS and PMOS) because NMOS passes either Strong 0 or weak 1 and PMOS passes either Strong 1 or weak 0. Since NMOS transistors pass only 0's and PMOS transistors pass only 1's, the output is always strongly driven and the levels are never degraded. This is called fully restored logic gate and simplifies circuit design consistently and reduces leakage power and increases speed. An additional control WLB is required for switching the access PMOS. The WLB and WL (word line) are non-overlapping opposite signals. Hence, during read and write operation, to retrieve the data from cell all access Field Effect Transistors can be swapped simultaneously. But, during hold mode all access FETs remain shot off.

A. Design of TG8T Sram

TG8T SRAM consists of 8 MOSFET transistors in which four transistors are used as two inverter circuits and remaining four are used as two transmission gates as shown in fig 1.

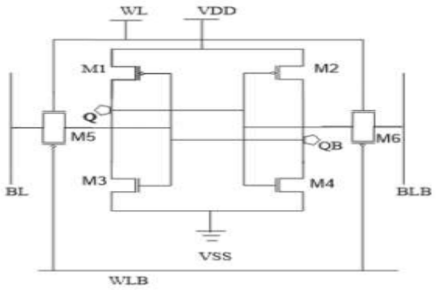

Fig 1: Circuit diagram of TG8T SRAM.

It also consists of two word lines namely word line (WL)and word line bar (WLB). It has bit lines namely bit line (B) and bit bar line (BB). B, BB, WL, WLB lines acts as input to the circuit. The output is observed at Q and QB. The design specifications are shown in table 1.

Parameter	WL	WLB	B	BB
voltage 1 (volts)	0	1.8	0	1.8
voltage 2 (volts)	1.8	0	1.8	0
Period	90ns	90ns	100ns	100ns
Pulse Width	30ns	30ns	50ns	50ns

Table 1: Design Specifications of TG8T SRAM.

The schematic view of TG8T SRAM with above specifications is designed as shown in fig 2 in virtuoso.

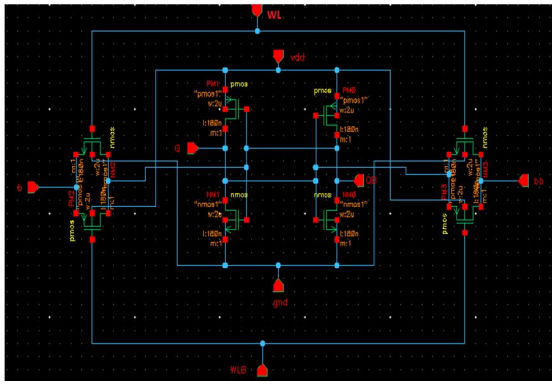

Fig 2: Schematic view of TG8T SRAM using virtuoso.

B. Working of tg8t sram cell

The working of TG8T SRAM cell consist of two operation i.e. write and read operation. When we performing a write operation ,both the bit lines are at opposite voltages which represent if bit line BL is at high then BLB is at low and vice versa (BL=1 and BLB =0 or BL =0 and BLB =1). When WL becomes high and also WLB =0 which enables NMOS and PMOS transistors M5 and M6 then data writes on the output nodes Q and QB of back to back connected inverter.

When the read operation is performed which is just opposite to the write operation, both the bit lines are at high voltages also behave as an output and WL is raised to high and WLB at 0. Since one of the output nodes (Q and QB) is at low then one of pre-charged bit lines start discharging and at that instant data is going to be read.

III. SIMULATION RESULTS

A. Output Graphs

The figure 3,4 and 5 shows the simulation graph of TG8T SRAM, dealy and power. WL, WLB, B and BB are the input lines which mean word line, word line bar, bit line and bit line bar respectively. Q and QB are the output lines.

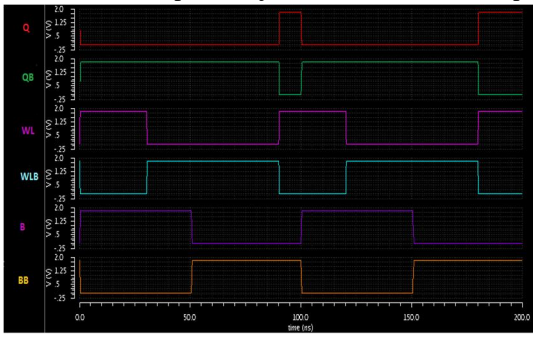

Fig 3: Simulation Result of TG8T SRAM.

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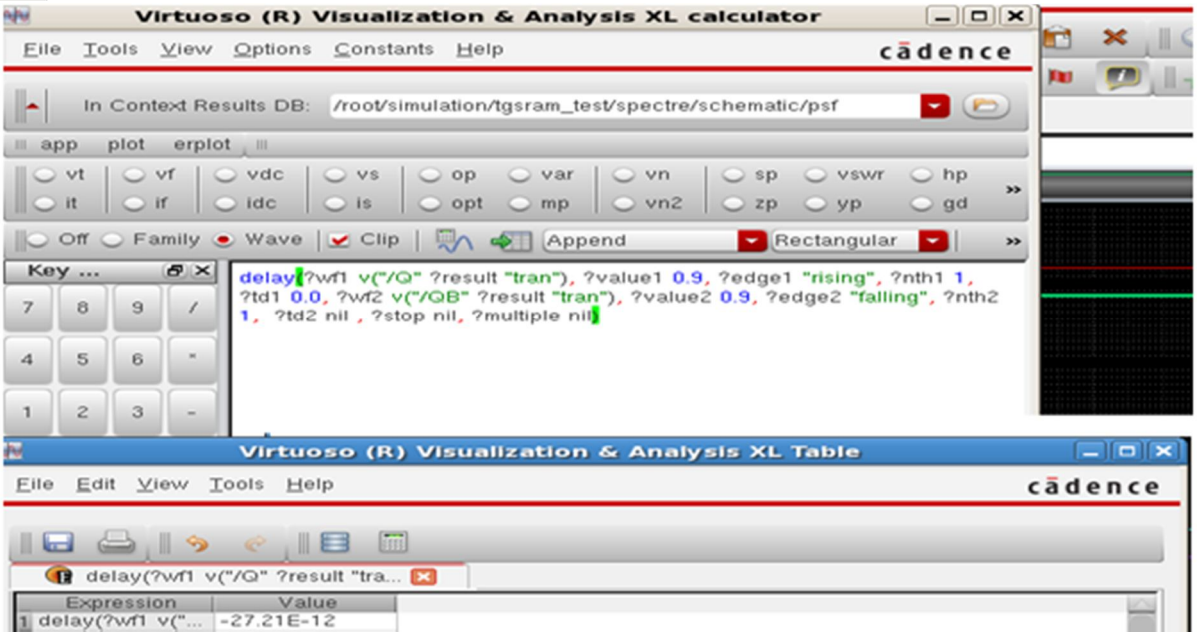

Fig 4: Delay of TG8T SRAM Cell.

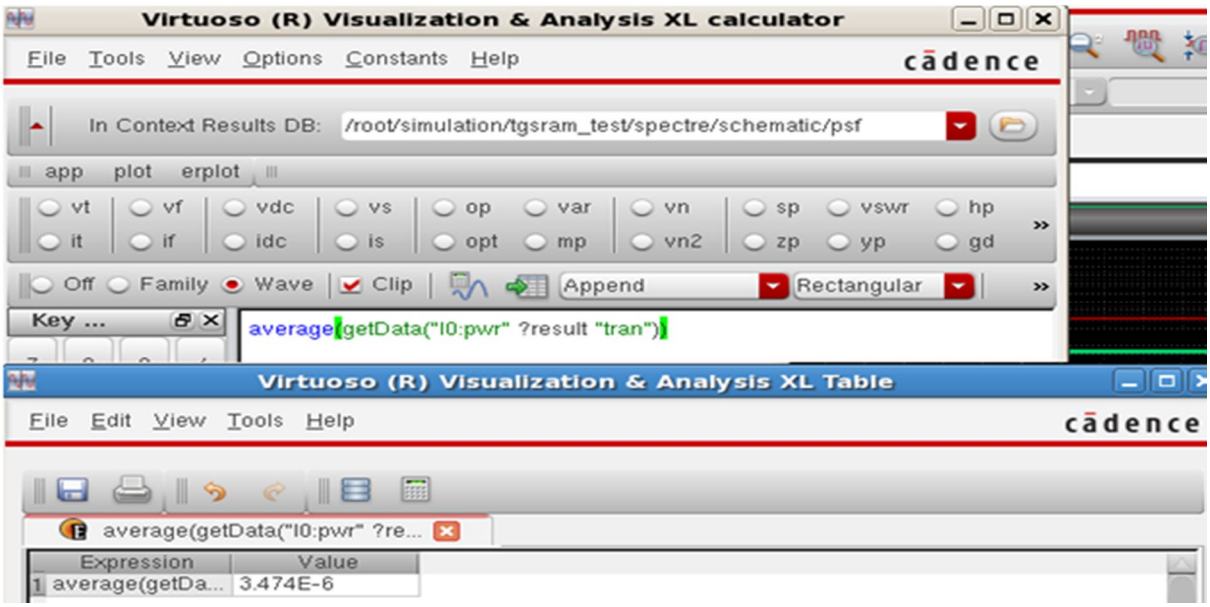

Fig 5: Power of TG8T SRAM Cell.

B. Comparative Analysis

Here the delay and power outputs of 6T SRAM, 8T SRAM and TG8T SRAM are compared and tabulated as shown in table 2.

SRAM	DELAY(sec)	POWER (W)
6T SRAM	99.88 E-9	2.616 E-6
8T SRAM	-62.99 E-12	2.54 E-6
TG8T SRAM	-27.21 E-12	3.474 E-6

Table 2: Comparative Analysis.

The table 2 shows the comparison of 6T SRAM and 8T SRAM with TG8T SRAM. It is crystal clear that the delay of TG8T SRAM is very less compared to existing SRAMs which implies speed of proposed design is faster than others. The bit line leakage problems are also less.

The power of proposed designed is slightly higher than standard 6T SRAM which is the major drawback of this project. Since there is a possibility of changing threshold voltage of CMOS transistors, we can overcome the above drawback using SYNOPSIS tool.

IV. CONCLUSION

An 8T SRAM cell is designed using Transmission gate in 180nm CMOS technology and its parameters are compared with the existing SRAM cells. The proposed design has improved parameters with the benefit of high speed operation as delay is decreased by 9.99E-8 leading to reduced leakage parameters. The results show major enhancement in the design parameters over standard 6T SRAM cell and 8T SRAM cell signifying its strength and functionality.

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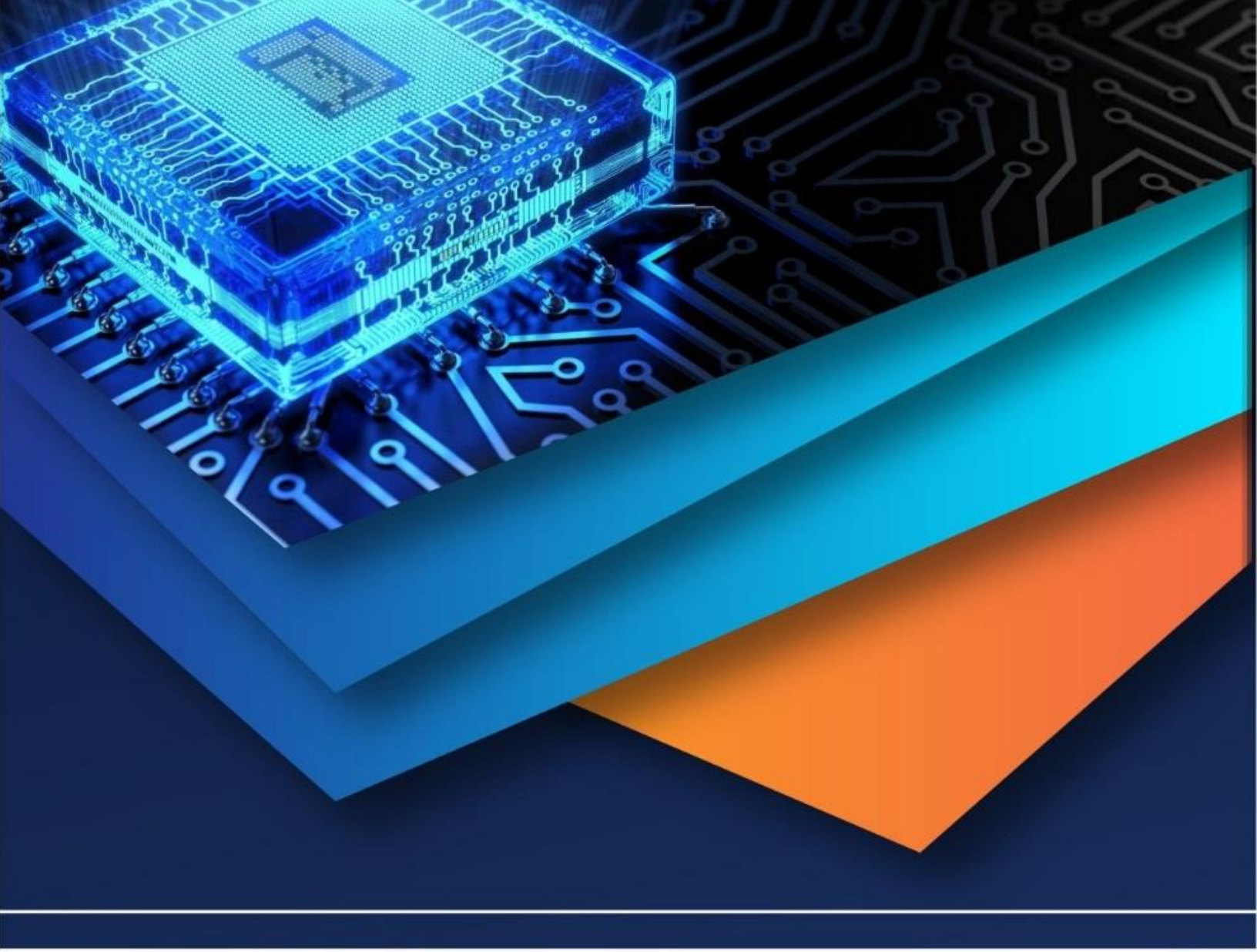

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