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Comparative Analysis of D Flip-Flops Using Different Technologies

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Abstract: ***The field of digital electronics has been directly towards to the low power digital system. The use of very large scale integration technology in high performance computing, wireless communication, consumer electronics has been rising at a very fast rate. The challenge for VLSI technology is growing in leakage power consumption. Wide utilizations of memory storage systems in modern electronics triggers a demand for high performance and low area implementation of basic memory component and one of the most state holding element is D Flip Flop. In this paper analysis of power and delay is done for D flip flop using different technologies like C2MOS, POWER PC, TSPC, SAER DFF,etc***
Keyword s: D flip-flop; propagation delay; C2MOS, TSPC, POWER PC etc.

I. INTRODUCTION

In the past, the major concerns of VLSI designers were area,cost, performance and reliability. Low power dissipation
became a highly design concern and become more important as we move to all mobile computing and communications. The latest advancement in computing technology has set up a goal for high performance with low power consumption for vlsi designers. Flip-flops or the data storage elements are almost an essential component of every sequential circuitry. Among various flip-flops, D flip-flop is commonly used. It captures the value of the D input at a particular predefined portion of the clock pulse (rising or falling edge of the clock) and its output is not affected at other parts of the clock. From the timing perspective, delay produced by flip-flops consumes a large part of the cycle time while the operating frequency increases. Over the past 4 decades CMOS technology have gone under drastic scaling with the view of integration ,density, high speed and low power dissipation.. Flip flops are important state holding and timing elements in digital circuits. The performance of D flip flop is much important to conclude the performance of the whole circuit. With increasing use of mobile devices, consumer electronics market demands a stringent constraint on reducing power consumption. Designers are striving for small area, low power and higher speed due to increasing demand of portable devices.. The need for comparing different design is the main motive of this paper.

II. D FLIP-FLOP TOPOLOGIES

A. Transmission gate (TG) based D flip-flop

Fig. 1 shows the D flip-flop designed using four CMO transmission gates and four inverters. First stage is the master
stage which is positive level sensitive and the second stage is
the slave stage which is negative level sensitive. During the positive clock pulse master follows the input while slave stores the previous input at the output (Q). When clock (C) changes from ‘1’ to ‘0’ or inverted clock (C!) from ‘0’ to ‘1’,slave becomes transparent and allows the previous input to
pass through to the output, and at that time there is no effect of
input on master as it is opaque.

B. True single phase clock (TSPC) D flip-flop

Fig. 2 shows true single phase clock (TSPC) D flip-flop. When clock(C) = ‘0’, first input inverter is on and the inverted D-input reaches node H. The second (dynamic) inverter is in the pre charge mode as MN3 is off and node X is charged up to *V*DD. As can be seen during this low phase MP4 and MN4 are also off, therefore the last inverter holds its value and the output is stable during the low phase of the clock. During high phase the input inverter is opaque so the previous inverted D input is stored on H. Second inverter evaluates since MN3 is on this time i.e. if H is high X discharges and if H is low then X remains high because in that case both MP3 and MN2 will be off, also MN4 is on. So, the D-input loaded during the falling pulse reaches output Q and is maintained till another rrissing edge is encountered. In this if transistors are placed closer to *V*DD and ground then the operation is faster.

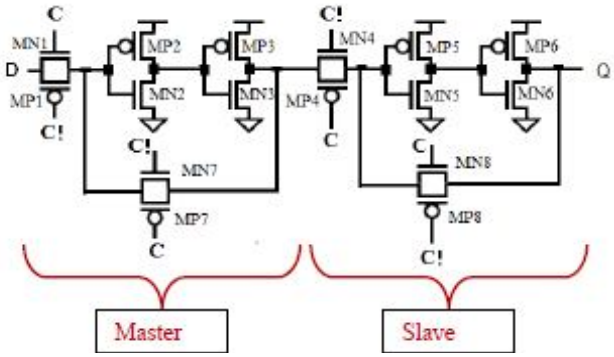

Fig. 1. Sixteen-transistor (16T) transmission gate (TG) based static D flipflop

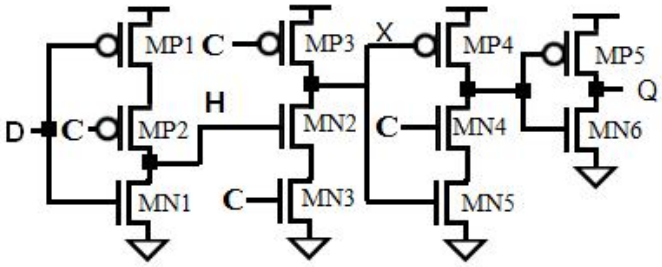

Fig. 2. Eleven-transistor (11T) true single phase clock (TSPC) dynamic D flip-flop.

C. Clocked CMOS D Flip-Flop

Fig. 3 shows the clocked CMOS D flip-flop. In this circuit also clock and inverted clock are used. It also consists of master and slave stages. Master follows the D-input when clock (C) = '1'. At that time slave is opaque but its regenerative feedback loop is transparent therefore the output at Q is stable. When clock= '0' master is opaque but its regenerative feedback loop is transparent therefore storing the previous D-input. This time slave is on and this D-input stored by the master is reflected at the output and is maintained till another falling edge is encountered.

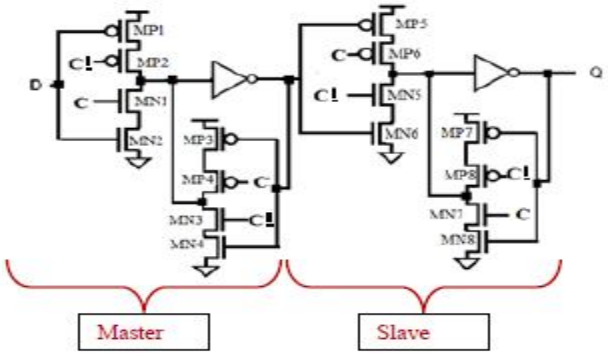

Fig. 3. Twenty-transistors (20T) clocked CMOS D flip-flop.

D. Novel Sense Amplifier Energy Recovery flip-flop (SAER)

Sense amplifier energy recovery flip-flop (SAER) [1] [2] is used to recover energy in a clock network and works on the basis of dynamic logic. This flip-flop generally consists of a pulse generator in the first stage and storage element in the second stage. It improves both the area as well as power efficiency, when compared to the conventional flip-flop. Optimization is achieved by adopting an adiabatic 2N-2N2P buffer that replaces the SR latch in conventional Figure 4 depicts the schematic diagram of the novel SAER flip-flop. is replaced by the adiabatic 2N -2N2P buffer circuit. The 2N-2N2P buffer proves to be more efficient when compared tothe CMOS logic. It also has a latch as an in-built circuit that is used for the purpose of storage. Feedback of data is also provided by the buffer which is one of the main features of SR flip-flops. Initially, when the clock is low, PMOS_1 and PMOS_2

will be pre charged to Vdd. This causes the four transistors present in the cross coupled inverter structure to be in a pre-charged state. There is no direct connection to the ground as NMOS_3 will not be conducting. In case of differential inputs, any one of the inputs will be high which makes the summing up voltages of NMOS_4, NMOS_5, NMOS_6 to be in pre-charged condition. As a result, when the clock is low initially, all the transistors will be in pre charged condition. When clock goes high, the data is captured in the 2N -2N2P buffer and it will be maintained until the end of the cycle. The transistor NMOS_5 is used to provide static operation. The operation is the same as the conventional SAER flip-flop with an increased area and power efficiency.

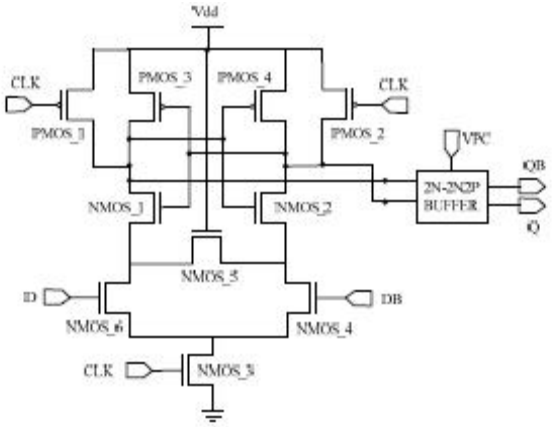

Fig. 4. Novel SAER-DFF.

E. Push-Pull D Flip-Flop

In Fig. 6 one extra TG and an inverter are added between the outputs of master and slave latches to get push-pull effect at the slave latch. This helps the input and output of the output inverter to be driven to the opposite logic values during switching. This additional path adds four extra MOSFETs but reduces the "clock to output" delay from two gates in conventional D flip-flops to one gate. To compensate for that increase in the number of MOSFETs, two TGs are removed from the feedback paths as it was in the case of Fig. 1. This circuit is comparatively faster than the rest.

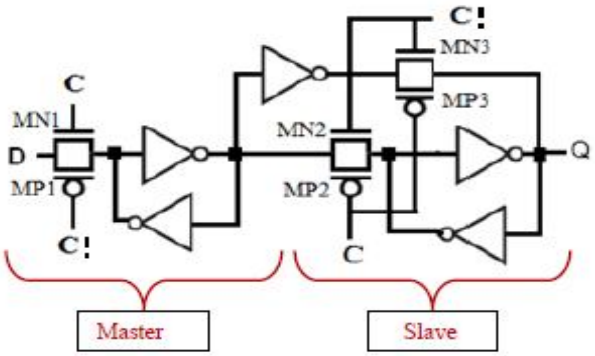

Fig. 5. Sixteen-transistors (16T) push-pull D flip-flop.

F. Data Transition Look-Ahead D Flip Flop

Figure.6, shows the proposed data transition look ahead D flip flop. The transmission gates TG4 and TG5 (DL) do the data transition look ahead. It compares the hold data at the output with the respective input data and enables the flip flop to write the data, accordingly. The DL block act as an XNOR gate. For example, when D = Q = 1, the clock is inactive and transmission of data is not required. But, when D = 1, Q = 0, the clock is enabled and data gets transmitted. Clock control block consists of the transmission gate TG6 followed by an NMOS transistor. The clock control signal [2] depends on the DL's output. The input to the clock control is given by the external clock CSP and divides into CK and CKN. DLDFF is triggered by the positive edge of the clock. When an input data *D* is the same as the hold data *Q*, the DL circuit makes P1 low. This turns the transmission gate in the clock control circuit off. As a result, CK and CKN do not transmit. CK and CKN transmit only when *D* and *Q* are different. When *D* changes to a value different from *Q*, P1 first changes to high. Next, when CSP rises, CK also rises and changes. Then, P1 changes back to low because *D* and *Q* are the same again. This immediately makes CK low. Therefore, a DLDFF consumes less power than a conventional one, when is low because CK is inactive when there are no data transitions.

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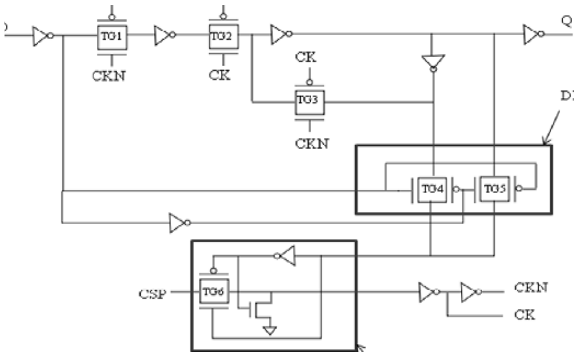

Fig.6. Data Transition Look-Ahead D Flip Flop

G. Power PC

The main advantage of POWER PC D flip flop is short circuit path and low power feedback.The circuit diagram of D Flip flop using POWER PC is shown in figure 7.

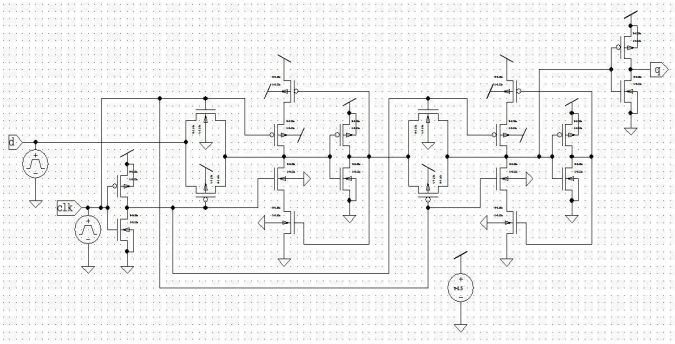
Fig. 7. Power PC based DFF

H. 6 Transistor D-Flip-Flop based on GDI Technique

The GDI technique is of more important because it uses only couple of transistors to construct a design. As the operation involves only two transistors, it could show better results in terms of Power Dissipation, Speed as well as the area occupied. This technique is most predominant for designing circuits in MOSFET technology. A basic GDI cell contains four terminals – G node (the common gate input of the n MOS (Negative channel Metal-Oxide Semiconductor) and p MOS (Positive channel Metal-Oxide Semiconductor) transistors), P node (the outer diffusion node of the p MOS transistor), N node (the outer diffusion node of the n MOS transistor), D node (the common diffusion of both transistors). P, N and D may be used as either input or output nodes, depending on the circuit structure shown in Fig.7. Multiple-input gates can be implemented by combining several GDI cells .GDI enables simpler gates, lower transistor count, and lower power consumption in many implementations. This technique allows reducing power consumption, propagation delay, and area of digital circuits while maintaining low complexity of logic design. The overall area and complexity of the circuit is minimized using GDI technique. Most of the functions which are complex (6-12 transistors) in CMOS, are very simple (only 2 transistors per function) in GDI design method.

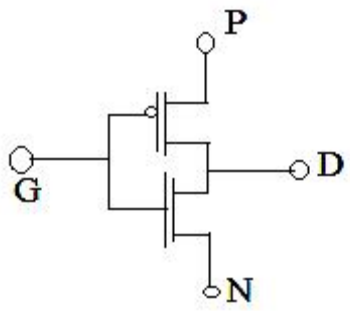

Fig. 7. Basic GDI Cel

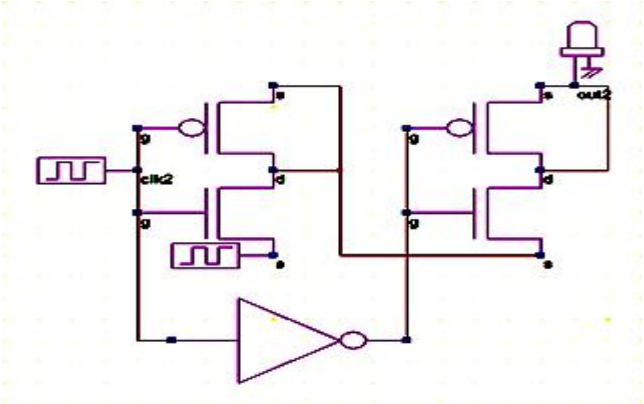

Fig. 8. 6 transistor D-Flip-Flop using GDI technique

III. RESULTS AND DISCUSSION

D-ff type	POWER DISSIPATION (μW)	Propagation delay (ns)
Transmission gate (TG) based D flip-flop	.48	19
True single phase clock (TSPC) D flip flop	.53	.29
Clocked CMOS D Flip-Flop	.52	4.17
Novel Sense amplifier energy recovery flip-flop (SAER)	.572	34.81
Push-Pull D Flip-Flop	2.48	8.5
Data Transition Look-Ahead D Flip Flop	.684	1.107
Power PC	.09	30
DFF based on GDI	2.43	2.78

IV. CONCLUSION

This work analyses and compares various known and less known D flip-flop circuits. The considered circuits can be employed for designing other complex memory and sequential
circuits. It is concluded from power dissipation comparison that power pc has lowest power dissipation and in propagation delay comparison TSPC has least propagation delay . So it is better to use TSPC logic style to design a system where fast speed is required and power PC flip flops for power conservative circuits.

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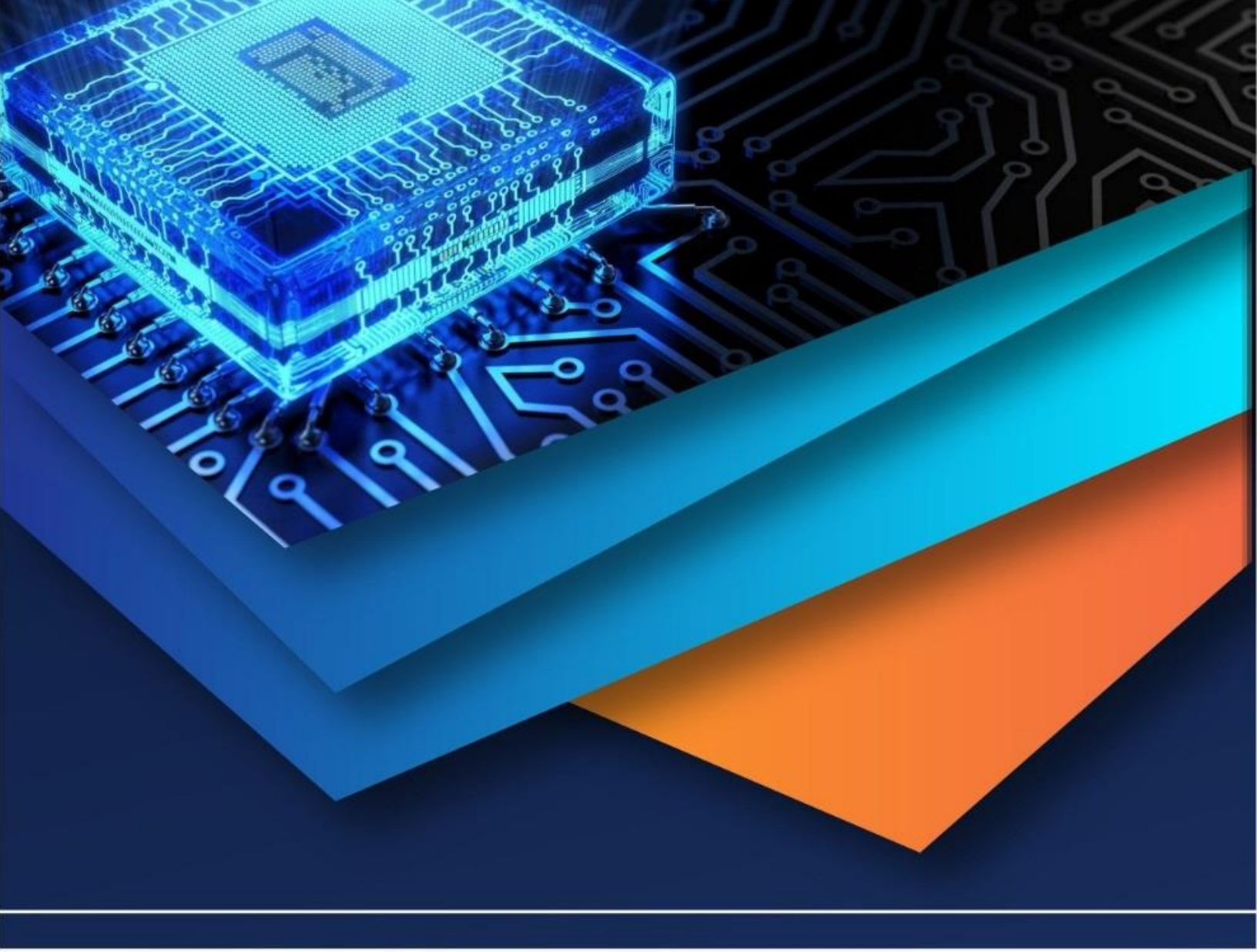

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