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Voltage Level Shifter Circuits in 45nm CMOS Technology - A Review

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Abstract: This paper demonstrates different voltage level shifter circuits in 45nm CMOS technology. In digital electronics the level shifter is also called as logic level shifter. It is a circuit used to translate signals from one logic level or voltage domain to another logic level or voltage domain. It allows compatibility between different blocks of system-on-chip (SoC) designs with different voltage requirements. The level shifter circuits are compared in terms of voltage shifting level, power dissipation and delay. The input signal is set to 0.3V. The dual supply voltages VDDH is set to 1.1V and VDDL is set to 0.3V. Simulations have been carried out in cadence® EDA tool.

IndexTerms: Level shifter, DCVS, Current mirror, Wilson current mirror, Dual current mirror, Cadence, Subthreshold to above threshold level conversion.

I. INTRODUCTION

The voltage scaling technique can reduce the power dissipation of a CMOS circuit, because of the direct proportionality between the supply voltage and power dissipation[1]. This creates an interfacing problem between different digital blocks inside an SoC. A level shifter circuit helps to solve this issue. There might be the need for a large number of level shifters in a single SoC. Hence power dissipation, propagation delay and area considerations are the main concerns in the design of a level shifter. The basic level shifter circuit is of four types[2]; dual supply level shifter (DSLS), single supply level shifter (SSLS), pass transistor half latch, pre-charge circuit.

Among these types of level shifter designs DSLS has been widely used in digital circuits because of its wide range voltage conversion. Sometimes SSLS also be used because of its compact layout. Pass transistor half latch and Pre-charge circuits are not preferred in industry because it can provide a small range of voltage conversion. The pre-charge circuits requires a clock synchronizer, implementing clock synchronizer itself consume more power. Thus this paper concentrate only on DSLS.

The differential cascode voltage switch (DCVS) logic based six-transistor design is considered as the traditional DSLS design and it was implemented for the first time in SoC. In subsequent years, a number of different designs are proposed by VLSI circuit design experts for level shifters. Which includes; 8 transistor (8T) DCVS Level shifter, 10 transistor (10T) DCVS level shifter, advanced DCVS level shifter, current mirror based level shifter, wilson current mirror based level shifter and dual current mirror based level shifter. The classification of level shifter designs is given in figure 1.1.
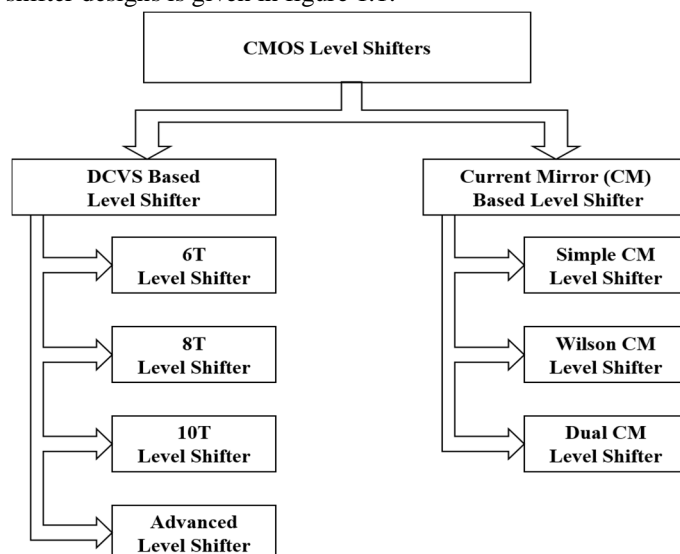

Figure 1.1 Classification of level shifter designs

II. LEVEL SHIFTER CIRCUITS

In this section all the above mentioned level shifter designs are demonstrated. The circuit diagram, transient response, calculated power and delay values are included in this section, for each level shifter design. The circuit diagram of conventional 6T DCVS based level shifter[2] is given in figure 1.2. The circuit consists of cross coupled PMOS transistors (Q1 and Q2) and two NMOS transistors (Q3 and Q4) driven by input signal IN. The circuit has critical issues at the voltage difference between low supply voltage (VDDL) and high supply voltage (VDDH) gets to be large. When the input is low, transistors Q3 and Q4 are OFF and ON respectively, then OUT is pulled down, causing M1 turns increases to VDDH, resulting Q2 turns OFF and OUT drops to the ground level. Voltage at OUT is determined by the drive currents for pull-up transistor Q2, also pull-down transistor Q4. If the drive current of Q2 is larger than Q4, OUT can not be discharged. The conventional 6T level shifter in 45nm technology can provide only a voltage conversion of 0.3V to 0.7V and the performance parameters can be improved to a better extend. The transient response of 6T level shifter is given in figure 1.3. The power dissipation and propagation delay of 6T based level shifter obtained during the preliminary analysis is 545.8 pW and 23.8 pS, respectively.
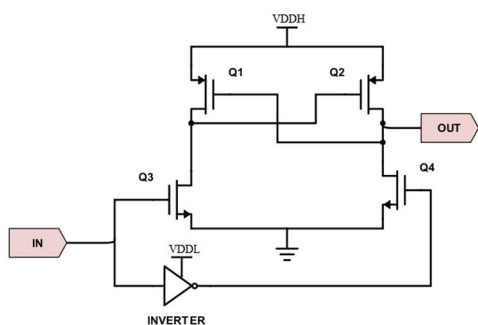

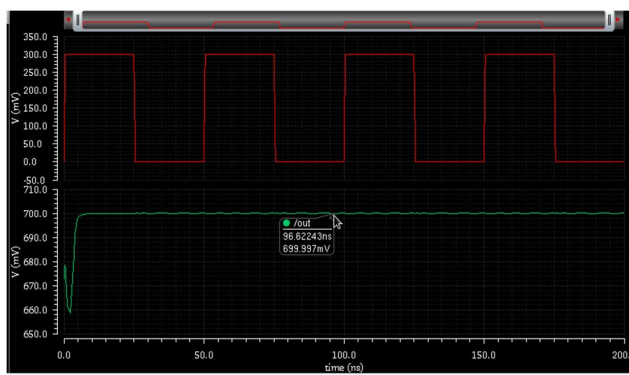Figure 1.2 Circuit diagram of 6T DCVS based level shifter

Figure 1.3 Transient response of 6T DCVS based level shifter

The 8T level shifter[3] is a modification of conventional 6T level shifter. The working of 8T level shifter is also based on DCVS concept. Circuit diagram for the conventional 8T level shifter is given in figure 1.4. The circuit consists of two cross coupled PMOS transistors (Q1 and Q2) and two NMOS transistors (Q3 and Q4) supplied with input signal and compliment of input signal. The performance of 8T level shifter in terms of power dissipation and propagation delay is improved compared to the conventional 6T level shifter. The voltage conversion levels of 8T level shifter is still remains the same (0.3V to 0.7V). In 8T level shifter circuit the input inverter section operating at VDDL and the cross coupled PMOS section and output inverter section operating at VDDH. When input is high, transistor Q3 and transistor Q2 turns on and thus rises voltage at node A1 and node A2 is pulled down to ground. Also this turns on transistor Q5 and OUT rises to VDDH. But, there is contention problem arises at node A1 and A2, between pull-down network operating at VDDL and pull-up network operating at VDDH. Thus, 8T level shifter cannot operate correctly when difference between values of VDDH and VDDL is large. The 8T DCVS based level shifter shifts 0.3V to 0.5V during the preliminary analysis. The transient response is given in figure 1.5. The power dissipation and propagation delay of 8T DCVS based level shifter obtained during the preliminary analysis is 548.9 pW and 46.7 pS, respectively.
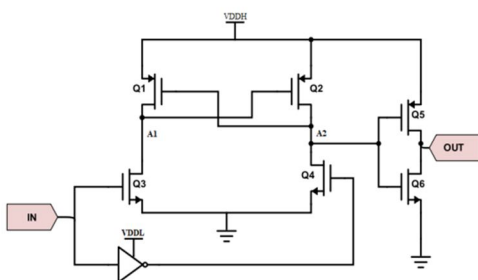

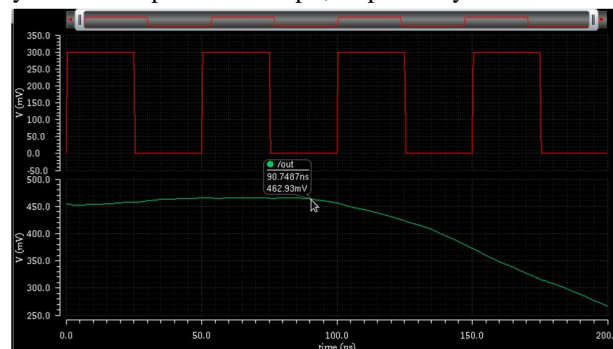Figure 1.4 Circuit diagram of 8T DCVS based level shifter

Figure 1.5 Transient response of 8T DCVS based level shifter

The 10T level shifter[4] is also a modified version of conventional 6T level shifter. The working of 10T level shifter is also based on DCVS concept. Circuit diagram for the conventional 10T level shifter is given in figure 1.6. The gate source voltage (Vgs) of transistor Q3 and transistor Q4 supply latching voltage on node A1 and A2. This voltage is used for cross coupled transistors Q1 and Q2 to create a positive feedback action which result in a fully VDDH voltage in node A1. When input is low, transistors Q3 and Q2 are turns on and transistors Q4 and Q1 are turns off. At this time if input switches to high, following procedure will take place. transistor Q3 off, transistor Q4 on, transistor Q1 on, it results A1 to switch from low to high and transistor Q2 turns off. Finally, the transition time from low voltage to high voltage is decided by the current driving capability of transistor Q1. Pull-down NMOS transistor has to overcome the PMOS transistor latch action before the output change its state, so the size of transistor Q3 and Q4 are much larger than transistor Q1 and Q2. The 10T level shifter has a large delay because it suffers from contention between the pull-down transistors (Q3 and Q4) and the pull-up transistors (Q1 and Q2). The contention problem gives rise to an increase in both delay and power dissipation. In particular, when the VDDL changes, the problem of current contention gets severe. The 10T DCVS based level shifter shifts 0.3V to 0.7V during the preliminary analysis. Transient response is given in figure 1.7. The power dissipation and propagation delay of 10T DCVS based level shifter obtained during the preliminary analysis is 2.3 nW and 210 pS, respectively.
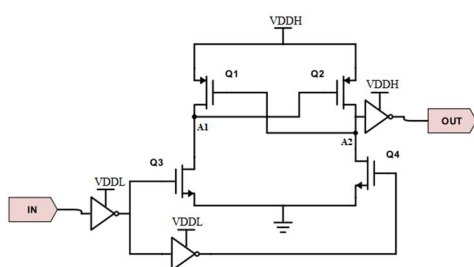

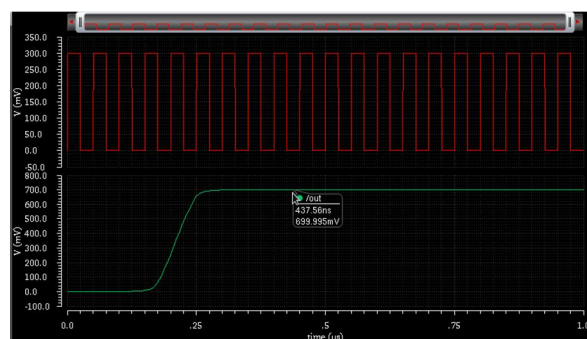Figure 1.6 Circuit diagram of 10T DCVS based level shifter

Figure 1.7 Transient response of 10T DCVS based level shifter

The advanced DCVS based level shifter[5] is a modified version of conventional 10T level shifter. The working of advanced DCVS level shifter design is also based on DCVS concept. Circuit diagram for the advanced DCVS level shifter is given in figure 1.8. This circuit contains a new regulated cross-coupled (RCC) pair for pull-up part. This technique regulates the strength of the pull-up network and reduces the charge or discharge time of the critical internal nodes, which consequently increases the switching speed and reduces the dynamic power dissipation. The advanced DCVS based level shifter shifts 0.3V to 1.1V during the preliminary analysis. The transient response is given in figure 1.9. The power dissipation and propagation delay of advanced DCVS based level shifter obtained during the preliminary analysis is 99.9 pW and 250 pS, respectively.
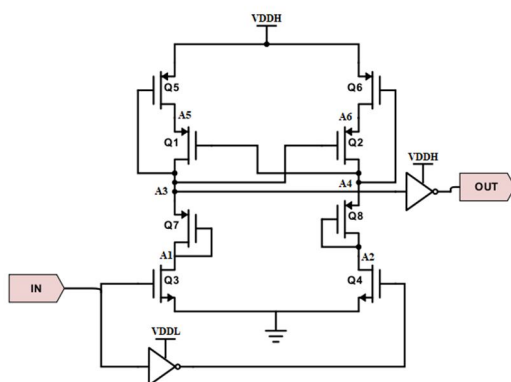

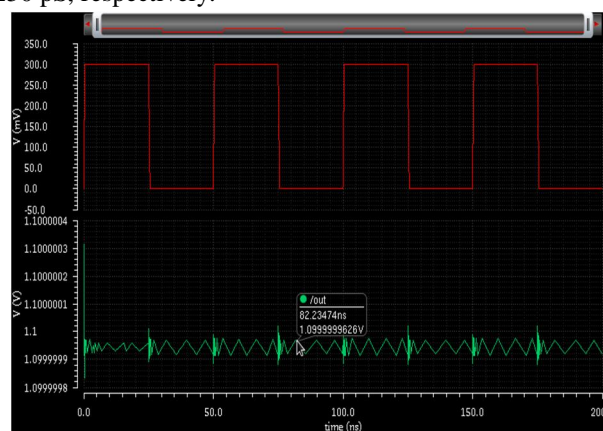Figure 1.8 Circuit diagram of advanced DCVS based level shifter

Figure 1.9 Transient response of advanced DCVS based level shifter

The generalized circuit diagram for current mirror based level shifter[6] design is given in figure 1.10. It consists of a basic current mirror composed of transistor Q1 and Q2. The pulldown network contains two NMOS transistors (Q3 and Q4), and they are fed with differential input signal. A current mirror is designed to copy a current through one active branch by controlling the current in another active branch of a circuit. It keeps the output current constant regardless of loading. A current mirror level shifter provides a fast level shifting even for ultra-low input signals (VDDL). The major advantage of this type of level shifter is that, it has low current contention because there is no overlap between the pull-up network and pull-down network. However, a problem of static current through Q1 and Q3 arises, which causes large standby power. To solve this problem, several level shifter circuits have been previously proposed, such as reducing the strength of the pull-up network by limiting their currents. Other solutions propose multi-stage level shifters and feedback control to reduce the standby power. This will result in larger delays compared to single stage design. The multi-stage level shifters always have large areas and power overheads due to complex control mechanisms. The current mirror based level shifter shifts 0.3V to 1.1V during the preliminary analysis. The transient response is given figure 1.11. The power dissipation and propagation delay of current mirror based level shifter obtained during the preliminary analysis is 4.4 nW and 165 pS, respectively.
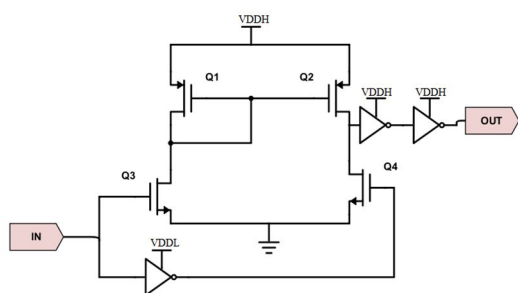

Figure 1.10 Circuit diagram of current mirror based level shifter
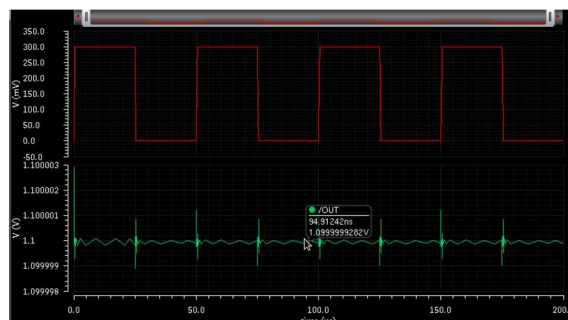

Figure 1.11 Transient response of current mirror based level shifter

To resolve the static current problem of current mirror based level shifter, researchers proposed wilson current mirror[7] based level shifter design. The generalized circuit diagram for wilson current mirror based level shifter is given in figure 1.12. The Wilson current mirror based level shifter uses a feedback transistor Q5 to prevent the static current. When the static current is cut off, the voltage swing at node A1 is reduced. This results in high static current at the first output inverter (I2). The speed of the fall transition decreases drastically due to the input inverter (I1) and the charge sharing from node A2 to A3 via Q5. The feedback control PMOS connected with the internal node creates a floating voltage at the internal node. This also results in the large static current on the output of the inverter (I2) and attenuates the circuit robustness. The revised wilson current mirror based level shifter proposes an input controlled diode chain to avoid the voltage swing issue for eliminating the static current, but it also induces large area and slow transition speed. A self-controlled current limiter can be effectively use to reduce the standby current. However, this also results high delay and large area. The wilson current mirror based level shifter shifts 0.3V to 1.1V during the preliminary analysis. The transient response is given in figure 1.13. The power dissipation and propagation delay of wilson current mirror based level shifter obtained during the preliminary analysis is 50.2 pW and 265 pS, respectively.
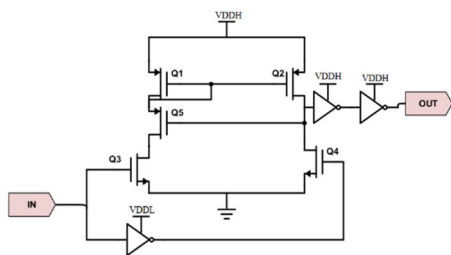

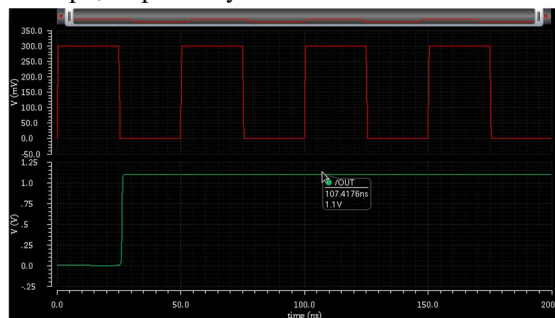Figure 1.12 Circuit diagram of wilson current mirror based level shifter

Figure 1.13 Transient response of wilson current mirror based level shifter

Currently, the researchers focusing on dual current mirror based level shifter[8] concept. The generalized circuit diagram for conventional dual current mirror based level shifter is given in figure 1.14. This conventional design consists of two current mirror sections and a DCVS section. The strength reduction of the pull-up network is done using two current mirror sections, the primary current mirror section (Q1 and Q2) and secondary current mirror section (Q3 and Q4). This will limit the currents applied to the pull-up transistors (Q9 and Q10). Thus the pull-down transistors (Q11 and Q12) would be able to overcome the mentioned current contention at the nodes (A1 and A2) and therefore discharge the output nodes to ground even for the input voltages lower than the threshold voltage. To avoid the static power dissipation, the current mirrors are turned on only during the transition times, in which the logic level of the input signal is not corresponding to the output logic level. Hence there is no current contention between the pull-up network and the pull-down network of this dual current mirror based level shifter design. Thus, this level shifter design is not only capable to convert extremely low levels of the input voltages, but also its transition times and power dissipation considerably decrease due to the fact that the strength of the pull-up device is decreased when the pull-down device is pulling down the output node to ground. The conventional dual current mirror based level shifter shifts 0.3V to 0.7V during the preliminary analysis. The transient response is given in figure 1.15. The power dissipation and propagation delay of conventional dual current mirror based level shifter obtained during the preliminary analysis is 7.55 uW and 5.1 nS, respectively.
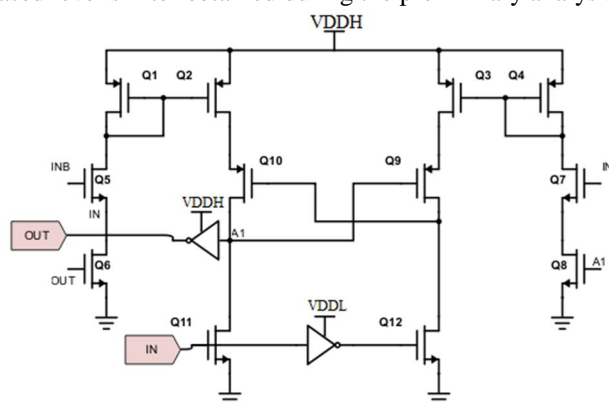

Figure 1.14 Circuit diagram of conventional dual current mirror based level shifter

Figure 1.15 Transient response of conventional dual current mirror based level shifter

III. COMPARISON

The circuits given here have been simulated in 45nm technology with input signal 0.3V. The obtained voltage shifting level, power dissipation and delay are tabulated for comparison and given in table 1.1. The comparison table also mention the major drawback in each level shifter design.

Table 1.1 Comparison of different level shifter circuits

Reference	Technology	Design Type	Pull-up Section	Pull-down Section	Voltage Shifting Levels	Power Dissipation	Total Delay	Major Drawback
[2]	45nm	DCVS	DCVS	NMOS Logic	0.3V to 0.7V	Moderate	Low	Contention Current
[3]	45nm	DCVS	DCVS	NMOS Logic	0.3V to 0.5V	Moderate	Low	Contention Current
[4]	45nm	DCVS	DCVS	NMOS Logic	0.3V to 0.7V	High	Moderate	Contention Current
[5]	45nm	DCVS	RCC pair	NMOS Logic	0.3V to 1.1V	Low	Moderate	Contention Current
[6]	45nm	Current Mirror (CM)	CM	NMOS Logic	0.3V to 1.1V	High	Moderate	Standby Current
[7]	45nm	Wilson CM	Wilson CM	NMOS Logic	0.3V to 1.1V	Low	Moderate	Floating Voltage
[8]	45nm	Dual CM	Dual CM	NMOS Logic	0.3V to 0.7V	High	Large	Leakage Current

IV. CONCLUSION

In this paper, various CMOS level shifter circuits have been compared in terms of voltage shifting levels, power dissipation and delay. The simulation results show that the Wilson current mirror based level shifter design is better than other conventional level shifter designs. The wilson current mirror based level shifter shifts 0.3V to 1.1V during the preliminary analysis. The power dissipation and propagation delay of wilson current mirror based level shifter obtained during the preliminary analysis is 50.2 pW and 265 pS, respectively. The conventional dual current mirror based level shifter design is the worst, because it is in development stage. The conventional dual current mirror based level shifter shifts 0.3V to 0.7V during the preliminary analysis. The power dissipation and propagation delay of conventional dual current mirror based level shifter obtained during the preliminary analysis is 7.55 uW and 5.1 nS, respectively. Currently, the researchers are focusing on dual current mirror based level shifter designs to optimize the power dissipation.

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