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Universal Reversible Combinational Circuit Design using Quantum Dot Cellular Automata

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Abstract— Quantum-dot cellular automaton (QCA) is a novel step towards the VLSI design by replacing the traditional CMOS Technology. It might bypass the transistor paradigm to molecular –scale or nano scale computing. In QCA paradigm, information is represented with the polarization of Quantum dots in a QCA cell. A very low power stimulus such as photon or light or very small voltage can change the polarity of QCA cell. In case of reversible logic circuit like combinational and sequential circuit, the total computation done with less power dissipation. Reversible logic synthesis in QCA had been proved to be very efficient Low power design for nanotechnology. In this paper, we proposed Reversible Logic Gate which is proved to be universal reversible logic gate by means of implementing all basic reversible logic (AND, OR, NOT, NOR, NAND, XOR and XNOR) gates. An important metric for evaluating reversible circuit is Garbage count. Hence Garbage minimization issue had also been addressed in our proposal. Here we had shown that our URLG implements all logic gates with reduced garbage output compared to previous proposal. Logic synthesis of 4*4 RLG using URLG being discussed and compared with previously reported HNG gate.

Keywords— QCA, Majority Voter (MV), Reversible Logic Gate, URLG, Garbage count.

I. INTRODUCTION

Low power design is become primary goal of Very Large Scale Integration (VLSI). Traditionally classical logic circuit which is found to be 'irreversible logic circuit' dissipate heat energy in an order KTln2 joules per bit of Information that is lost, where K is Boltzman's constant and T is absolute Temperature at which the computation is performed. Bennett shows that in case of Reversible logic computation KTln2 joules energy will not dissipate [23]. Hence Reversible logic design naturally gets priority to design combinational as well as sequential circuit. In this Low Power design era Reversible circuit design is applicable for VLSI in CMOS, Quantum computing, DNA computing as well as Quantum dot cellular automata (QCA). In QCA, Limited progress had been noticed using QCA, a few bunch of proposal had been found. In Quantum computing we found there are many proposal on Reversible Logic Gate (RLG) design like Fredkin Gate [18], Feynman Gate [16], Toffili Gate [17]. Very recently Haghparast and Navi Proposed NFT Gate for Nanotechnology based system [19]. In this proposal, it also addressed 'Garbage Minimization' problem for implementing all basic logic gate. HNG [19] proposed for 4*4 Reversible Logic Gate.In this paper, we explore a 'Universal Reversible Logic Gate' (called URLG) that implements all basic gate in QCA like AND, OR, NOT, NAND, NOR, XOR and XNOR. It also addressed the 'Garbage Minimization' problem. We make a comparison with NFT in context of Garbage count; as a result we show a maximum minimization of garbage output ever reported. We also proposed effective design 4*4 RLG using 3*3 URLG as a basic building block.

II. BASIC QCA

Quantum dot cellular automata consist of four quantum dots positioned at four corners of cell and two mobile electrons confined within the cell. In QCA logic state is determined by the polarization of electrons rather than voltage level as in CMOS technology. The two stable polarization of electrons P= +1.00 and P= -1.00 of a QCA cell represents logic '1' and logic '0' respectively, shown in Fig.1 QCA required four phased clocking signal. The four phases are relaxed, switch, hold and release. In the relax phase there is no inter-dot barrier. In the switch phase, barrier is slowly become high and cell attends definite polarity depending on the input. Electrons are polarized due to columbic effects. The polarity retains in the hold phase. The barrier is slowly getting lowered and cell release the polarity in the release phase.

III. REVERSIBLE LOGIC GATE

To avoid energy dissipation in irreversible logic gate, RLG proved to be promising area of study [23]. There are several proposals had been made which are (A) Feynman (FG) [16] (B) Toffoli gate (TG) [17] (C) Fredkin gate (FRG) [18] (D) NFT Gate [19] commonly performed as reversible logic gates shown in Fig.2 to Fig.5.

Definition 1: If a reversible gate has k input and therefore k outputs, Input Vector Iv is mapped with output vector Ov such that mapping is bijective i.e. the one-to-one mapping between Iv and Ov. The corresponding reversible gate is known as RLG k*k gate.

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Definition 2: Garbage output refers to the no's of output added to make n*k function reversible, which output is/are not used for further computations.
Definition 3: Constant Input preset value of input that ware added to n*k function to make reversible.
Example1: A 2-input 2-output function given by formula (X, Y)□(X',X Y) or truth vector [2,3,1,0] is reversible.

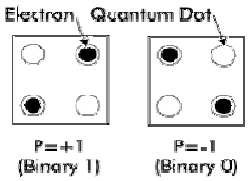

Fig.1. QCA Polarized cell

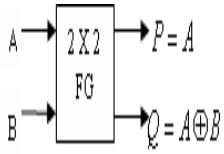

Fig. 2. Feynman Gate

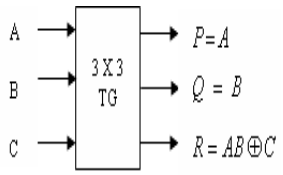

Fig. 3. Toffoli Gate

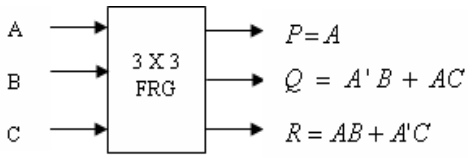

Fig.4. Fredkin Gate

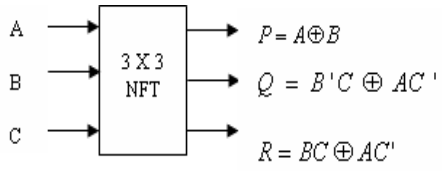

Fig.5. NFT gate

IV. SCOPE OF WORK

As we discussed early, that Reversible logic gate design is emerging technology in low power computing. Landauer shows in [12] that in case of irreversible circuit design each bit of information lost in the form of heat energy and generate KTln2 joules of heat energy. Bennett shows that in case of reversible circuit design the above energy will not be dissipated [23]. There are several proposals had been found in Quantum Computing on reversible logic gate design, few are [12][13][14]. But there are very few proposals had been found in QCA [19][20]. Very recently Haghparsat and Navi proposed a NFT Quantum Gate [19] focusing on important metric in reversible logic design 'Garbage count' for designing basic gate. The 'Garbage count' issue is applicable for Quantum Computing as well as QCA design. So 'Garbage minimization' must be focused in the research work. Haghparsat and Navi also reported 4*4 HNG gate [19]. Hence it may be scope of work to design a universal reversible gate (3*3) by which we can address the 'Garbage minimization' issue and also able to synthesis 4*4 or any k*k RLG using that reversible gate in QCA.

V. PROPOSED URLG

Reversible Logic Gate design proved to be promising technique in low power era. Power dissipation due to irreversible circuit had been addressed in [12]. In this paper our centre of attention is to design molecular QCA gate which is proposed to be universal Reversible gate (called as URLG). Using our proposed URLG we can able to design all basic reversible logic gate like

AND, OR, NOT, NAND, XOR and XNOR. The important metric for Reversible Logic Design is Garbage count had been addressed in [19]. We had shown that best 'garbage minimization' is achieved with respect to all counterparts. We also demonstrate Reversible Latch using proposed URLG.

A. Characterization of URLG

Proposed 3*3 Universal reversible logic gate is defined by mapping function f: M□M is one to one i.e. bijective. The Input vector Iv (A, B, C) and output vector Ov=(P=C (AB),Q=B,R=C (A+B)). where' ' denotes XNOR. The truth table of URLG is shown in Table 1.The URLG had been design using 8 MV's and 2 NNI. The four numbers of clocking zones are required for designing our URLG in QCA. The block diagram of URLG gate with D0 to D3 clocking zones is shown in Fig.14 and the symbol diagram is shown in Fig. 6.

B. Implementation of Combinational Basic Reversible gate

The URLG can be used as building block for implementing different basic logic gate. In Fig.7 Shows one URLG can implement both AND & OR gate with only one garbage output. The constant input C=+1.00, the output 'P' act like AND and output 'R' act like OR gate. If the constant input C change to '-1.00'(i.e. binary 0) the circuit acts like NAND & NOR gate, the output 'P' act like NAND and output 'R' act like NOR gate which is shown in Fig. 8. It implies that practically we can achieve four basic gates using single URLG by altering constant input C. The garbage output is only one for four basic gates, which is best proposal than the exiting proposal. The Fig.9, Fig.10 Shows implementation of XNOR and XOR gate. In case of XNOR we required only one URLG with two garbage output and constant input B=-1.00(i.e. binary 0). On the other hand XOR can be implemented by using two URLG as shown in Fig. 10. The three constant input are polarized as describe in figure and four garbage output for implementing XOR gate. The comparison made with recently made proposal by Haghparast and Navi [8] is shown Table 2. The result is concluded in terms of garbage minimization and no's of URLG used to better than the exiting counterpart.

Table 1 Truth table for 3*3 URLG

Input of 3*3 URLG			Output of 3*3 URLG		
A	B	C	P	Q	R
0	0	0	1	0	1
0	0	1	0	0	0
0	1	0	1	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	0	0	1
1	1	0	0	1	0
1	1	1	1	1	1

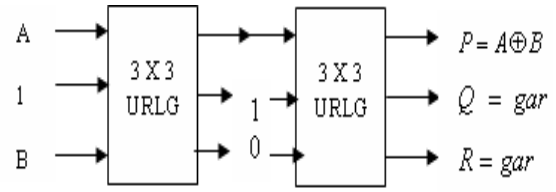

Fig. 6. 3*3 URLG. '$\otimes$'denotes XNOR operation.

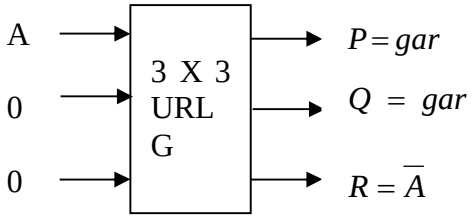

Fig. 7. Reversible AND, OR gate using URLG

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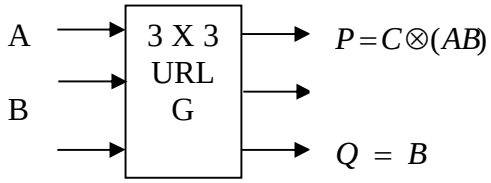

Fig.8 Reversible NAND, NOR gate using URLG

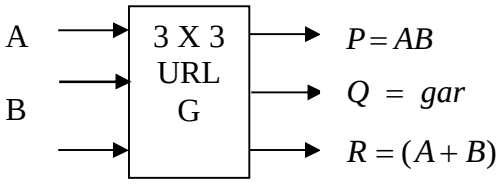

Fig. 9. Reversible XNOR gate using URLG

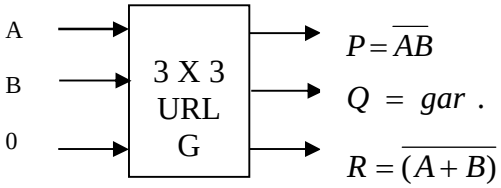

Fig. 10. Reversible XOR gate using URLG

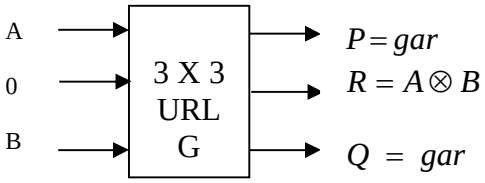

Fig. 11. Reversible NOT gate using URLG

VI. IMPLEMENTATION OF 4*4 RLG

We introduce 4*4 RLG synthesis using URLG as shown in Fig.12.The input vector Iv(A,B,C,D) and the Output Vector Ov=(P=C (AB),Q=B,R=C (A+B), S=C D).Hence we prove that our proposed URLG truly a Universal Reversible Gate.

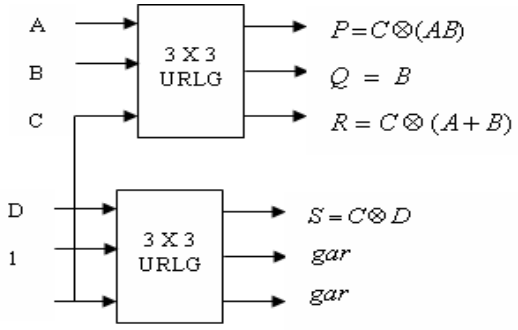

Fig. 12. 4*4 RLG synthesis using URLG.' ' denotes as XNOR operation.

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VII. SIMULATION RESULT

The design of URLG was verified with simulator QCADesigner V2.0.3 [22]. In the bi stable approximation we used following parameter: QCA cell size 18nm * 18 nm, Dot size= 5nm2, number of sample =42800, convergance tolerance=0.001000, radius of effect=41nm, relative permittivity =12.9 clock high=9.8e-22 and clock low=3.8e-23, layer separation =11.5000nm. In our QCA Layout we have the goal of remarkable design of URLG. Simulation result verified our proposed URLG.

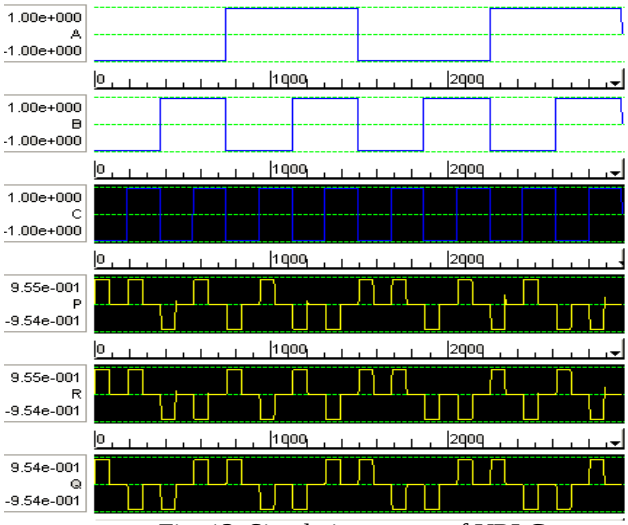

Fig. 13. Simulation output of URLG.

VIII. RESULT AND DISCUSSION

The proposed Universal reversible logic gate is more efficient and effective gate design in QCA. First, we compared with early reported gate NFT [8] with respective to garbage count and No's of gate required to implement all basic gates, the result shows in Table 2.We found 37.5% garbage minimization improvement compared with NFT, which is maximum minimization of garbage ever reported in QCA literature.It also be proved to be useful building block for designing 4*4 reversible gate as shown in Fig. 14, similarly it also achievable any size (k*k) Reversible gate. Hence the Evaluation suggests that the name 'Universal Reversible Logic Gate' is truly a Universal gate.

IX. CONCLUSION

In this paper, we explore a testable Universal Reversible logic gate (URLG) which is proved to be Universal gate. We also compared with very recently proposed NFT and achieved 37.5% improvements in garbage minimization with respect to NFT as shown in Table 2.URLG is also applicable for design sequential circuit and is a basic building block for 4*4 RLG. Hence we came to conclusion that our proposed testable URLG design must be promising step towards the goal of low power design in nanotechnology.

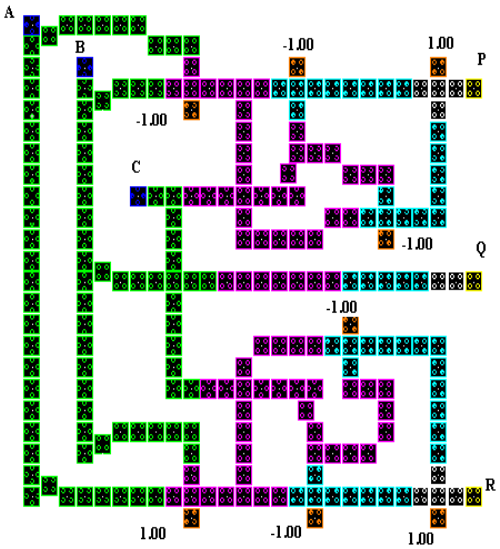

Fig.14. 3*3 URLG Implemented with QCA Designer [22].

Table 2. Comparison with our Proposed URLG and NFT

Basic Logic Gate Design	Using NFT [8]			Using URLG			Improvement
	No's of NFT	No's of MV	No's of Garbage output	No's of URLG	No's of MV	No's of Garbage output	
AND +1 OR	2	26	4	1	10	1	Over all 25 % improvement in using No's of RLG and 37.5% improvements in Garbage count.
NAND+NOR	3	39	6	1	10	1	
EXOR	1	13	2	2	20	4	
EXNOR	2	26	4	1	10	2	
NOT	-!	-	-	1	10	2	
Total	8	104	16	6	60	10	

1 both gates are implemented with single gate. Hence no extra URLG required. ! NOT gate implemented with NAND gate.

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