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Effect of Bandgap Variation on DGTFET

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Abstract: ***The physics model and electrical characteristics of the silicon and germanium based tunneling double gate field-effect transistor are discussed for low power logic applications using two dimensional device simulation. Ge has a property of high band-to-band tunneling rate as compared to Si, the Ge-DGTFET suffers from uncontrolled off-state leakage current I_{off} rather than its higher on-state current I_{on}. It is also shown increasing I_{on} with a steeper subthreshold swing SS, source doping concentration is increased to reduce the bandgap and this will narrow the tunneling width. Device design and physics model presenting the impact of Electric field, surface potential model, gate work function,Source Doping and gate oxide variation on the performance of Ge- DGTFET and Si-DGTFET are discussed. The simulations have been carried out on Sentauras TCAD tool.***

Keywords: BandGap,BTBT,Ambipolar Current,Analytical model

I. INTRODUCTION

Scaling down of MOSFETs to the nanoscale level, power dissipation factor is a vast concern. Reducing the supply voltage (V_{DD}) is very difficult due to the exponentially increasing sub-threshold leakage current, which accompany a transport mechanism followed by charge carrier diffusion over a thermal barrier which is limited to 60mV/dec turn-off in the best condition. To allow reduction in supply voltage , novel transistor structures need to be investigated. Whereas such transistor structure is the TFET, in which transport is illustrated by tunneling through a source barrier instead of diffusion over the barrier[1-7]. Many recent studies have been performed investigating different DGTFET structures. However, one big concern with DGTFETs is that they may not exhibit high driven currents due to a high tunneling resistance.Here we have experimentally demonstrated Silicon based DGTFET and Germanium based DGTFET exhibiting record high drive currents, somehow comparable to conventional MOS, showing that the a small bandgap material can significantly reduce the tunnel width. Another problem with DGTFET is that they exhibit ambipolar behavior, which leads to high off-state leakage current. TFETs are essentially a gated *p-i-n* diode, which accomplished the gate-controlled BTBT between the source and the channel to realize steep subthreshold swing. Furthermore, excellent short channel effects and extremely low I_{off} are achieved by its reverse biased *p-i-n* diode configuration. However, one major drawback of the Si TFET is that its on-state current is lower than that of CMOS transistors and below requirement set in the International Roadmap for Semiconductor(ITRS)[8-10]. The important factor here is the bandgap(E_g) of Si. Materials whose Eg is smaller than Si or having a higher BTBT rate, such as germanium, are required to further increase the Ion. Using Ge in TFETs could lead to excessive I_{off}.
Here we also present Germanium-source DGTFET which extends the benefits of tunneling furthermore by inserting a small bandgap material (i.e. Ge) in the source region of the device to enhance the tunneling current[17]. It will be experimentally observed that the planar Ge-source DGTFET can achieve a high I_{on}/I_{off} current ratio ($I_{ON}/I_{OFF} > 10^6$) for low supply voltage operation[10]. We have also developed a complete Band structure information, drain current model, surface potential model, electric field model and includes all transitions. Using TCAD simulator, we have studied the Si and Ge based DGTFET configurations, in their ability to solve the ambipolar problem and achieve high ON-currents and low OFF-leakage[11-15].

II. DEVICE STRUCTURE AND PHYSICS-

A novel n-type DGTFET is proposed with a thin silicon layer and another with germanium layer, which is isolated from the substrate by a thin dielectric layer of HfO_2. The basic design represents a gated p-i-n diode structure. Tunneling phenomenon takes place in this device between the intrinsic and p^+ regions. The parameters using for design of these devices are explained here. The doping concentration taken for both device is 10^{20} , 10^{16} and ,10^{18} atoms/cm^3 for the source, channel, and drain regions, respectively along with thickness of silicon/Germanium layer(T_{si}) = 10 nm and gate oxide (T_{ox}) = 2 nm and length of source ,channel and drain are respectively 30 nm,40 nm,30 nm. Doping has been optimized in order to create the maximum ON current, and a low OFF current. It is desirable for any tunnel device to have a high source doping but a lower drain doping. The work function chosen for the gate contact is 4.2 eV, corresponding to a metal gate stack.

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The schematics diagram of Si-DGTFET and Ge-DGTFET is shown in Fig.1. Operation of the device is performed in reverse Biased region. For simulation of n-DGTFET source should be kept grounded and positive voltage is applied to drain region and voltage is applied to the gate, the n-region is referred to as the drain and the p^+ region as the source. Applying gate voltage zero, the width of the energy barrier between the channel region and the p^+ region is wider (the minimum for allowing the process of tunneling), and hence the device is in the OFF-state. But when a increase in the positive gate voltage applied , the bands in the channel region are pushed down and, tunneling barrier will become narrower which will allow tunneling current to flow.

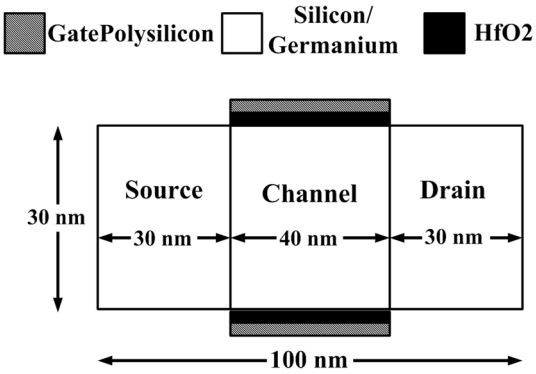

Fig.1 Basic structure of Si/Ge-DGTFET

While operating device tunneling mechanism also observed in which electrons travel from the valence band to the conduction band by tunneling across a potential barrier[16-18]. Mathematically tunneling probability expressed as-

$$T(E) = \exp\left(-\frac{4\lambda\sqrt{2m}Eg^{3/2}}{3\hbar(Eg+\Delta\Phi)}\right) \quad \text{……..(1)}$$

where m = reduced effective mass of the particle (electron)

E_g = energy band gap of the semiconductor in region where the tunnel barrier is formed

$\hbar$ = reduced Plank's constant

λ = length of tunnel path

$\Delta\Phi$ = energy difference between valence band of source and conduction band of channel

To increase on current, Ge is chosen to replace Si as the device layer due to its smaller bandgap which is .66ev for Ge and 1.12ev for silicon[18]. The physics behind this is explained by the energy band diagrams for both Si and Ge DGTFET. During the operation process in on state of device tunneling of charge carriers start to occur near the source from the valence band to the conduction band toward the channel when V_{GS} is kept positive. Tunneling barrier width for different V_{GS} determines the amount of electrons that could tunnel across from source to channel[19-20]. When a width is kept narrow more electrons could tunnel through the barrier. In the Si TFET, the tunneling barrier width is more whereas in the Ge DGTFET, width is less due to the smaller bandgap of Ge, thus contributing to increased source-side BTBT rate and I_{on} as shown in fig.3.

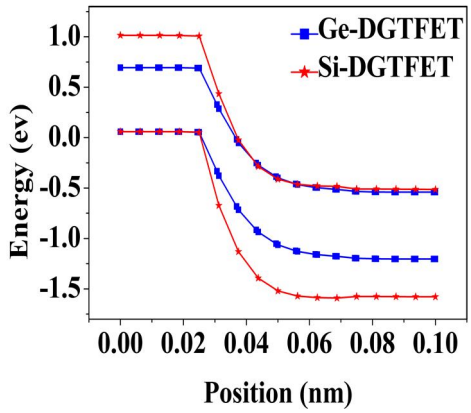

Fig.2 Band Diagram for Si and Ge-DGTFET

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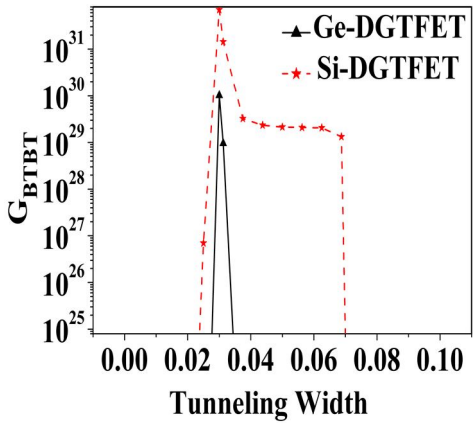

Fig.3 BTBT rate for Si and Ge-DGTFET

A. Electric field

The electric-field distribution across the channel length can be obtained by differentiating the electrostate potential.
The lateral electric field can be written as-

$$E_X = -\frac{\partial \phi(x,y)}{\partial x} = \frac{\partial \phi_S(x)}{\partial x} = K(Ae^{x} - Be^{-kx})$$

…….(2)

The vertical electric field can be written as-

$$Ey = -\frac{\partial \Phi(x,y)}{\partial y} = C_1(x) - 2yC_2(x)$$

…….(3)

B. Drain Current

Current flow mechanism in DGTFET is due to band to band tunneling of charge carriers from valence band to conduction band of channel region.The tunneling generation rate (T) can be calculated using Kane's model[19] . The total drain current computed by integrating the band to band generation rate over the volume of the device.

$$I_{DS} = q\pi r^2 \iint T(r,z)drdz \qquad \text{…….(4)}$$

Kane's Model has been expressed as-

$$T(E) = A_{KANE}\frac{|E|^2}{\sqrt{E_g}} e^{\left[-B_{KANE}\frac{E_g^{3/2}}{|E|}\right]} \qquad \text{…….(2)}$$

Where,

$$A_{KANE} = \frac{q^2\sqrt{2m_{tunnel}}}{h^2\sqrt{E_g}}$$

$$B_{KANE} = \frac{\pi^2 E_g^{3/2}\sqrt{m_{tunnel}/2}}{qh}$$

$$\frac{1}{m_{Tunnel}} = \frac{1}{m_h m_o} + \frac{1}{m_e m_o}$$

$|E|$ is the magnitude of Electric Field where $|E| = \sqrt{E_r^2 + E_z^2}$ and E_g is the bandgap,M_o is the rest mass of an electron, m_e and m_h are the electron and hole effective masses respectively.

III. RESULTS AND DISSCUSSION-

This section presents the variation of gate voltage , variation of gate oxide , variation of doping concentration ,electric field and surface potential profiles of Si/Ge DG-TFET based on 2D poisons equation .

A. Effect of Surface Potential and Electric Field-

Surface Potential and electric field variations for germanium and silicon DGTFET is shown below. Clearly seen by fig that surface potential is increasing in Si-DGTFET along the length of channel with respect to Ge-DGTFET.The surface potential increases in Si-DGTFET as compare to Ge-DGTFET because of bandgap difference of Ge and Si i.e higher the bandgap higher the electrostatics potential. Besides this it is also observed that surface potential increases for higher gate voltage. Furthermore for electric field it is also observed that by figure that the peak electric field is greater in source channel region in Si-DGTFET as compare to Ge-DGTFET which indicating that the tunneling probability of carriers between the occupied energy bands at source side to unoccupied energy band at channel side will be greater in Si-DGTFET.

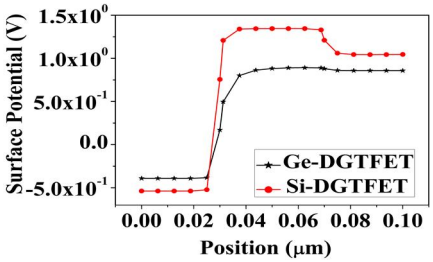

Fig.4 Surface Potential along the channel

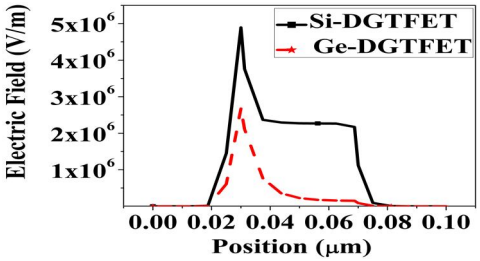

Fig.5 Electric Field along the channel

B. Effect of Work Function

Effect of changing the gate work function can be observed from the transfer characteristics of both Ge and Si DGTFET i.e. shifting of the central point of the current curve to the left upon a decrease in the gate work function. Effect of work function on DG-TFET characteristics I_{OFF} is determined by gate-drain leakage current . I_{OFF} initially decreases while increasing gate work function due to decrement in gate current but increases for higher gate work function values due to higher tunneling rate between the drain and channel. Decreasing the gate work function increases the source–channel tunneling and decreases the drain–channel tunneling, raising the right-hand curve and lowering the left-hand curve along the current axis, this will effect on shifting the central point of the curve to the left.

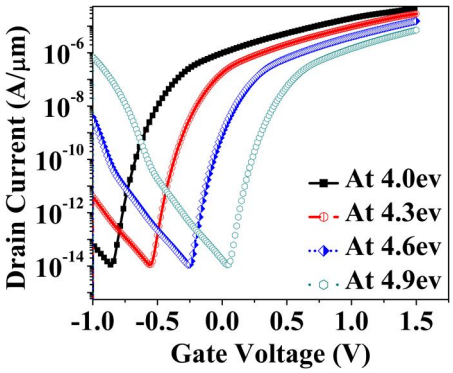

Fig.6 I_D-V_G curve at different workfunction for Si-DGTFET

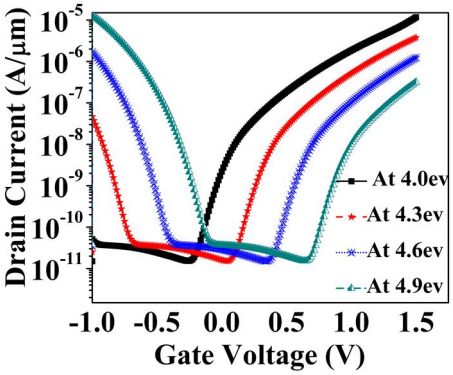

Fig.7 I_D-V_G curve at different workfunction for Ge-DGTFET

C. Effect of changing Gate Oxid

Oxide is an insulator, the gate oxide prevents current leakage from the channel to the gate oxide capacitance is given as $C_{ox} = \epsilon_{ox}/t_{ox}$, Clearly observed by this formula, the gate oxide capacitance increased by reducing the thickness. Using oxide material with high permittivity has the added benefit of further reducing the oxide capacitance and thus increasing the gate control of the channel. For both the diagram for Ge and Si DGTFET Si-DGTFET show better results to enhanced on current It has been observed by the diagram that as the dielectric constant is increased, the gate has more control over the channel due to reduction of equivalent oxide thickness. This gives rise to a higher band bending and hence the minimum tunneling length decreases with increase of dielectric constant.

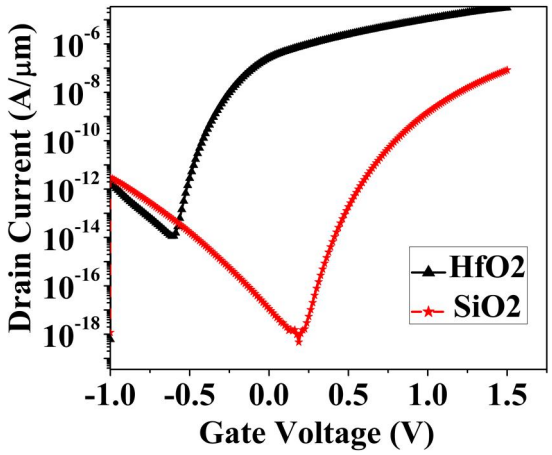

Fig.8 I_D-V_G curve at different gate oxide for Si-DGTFET

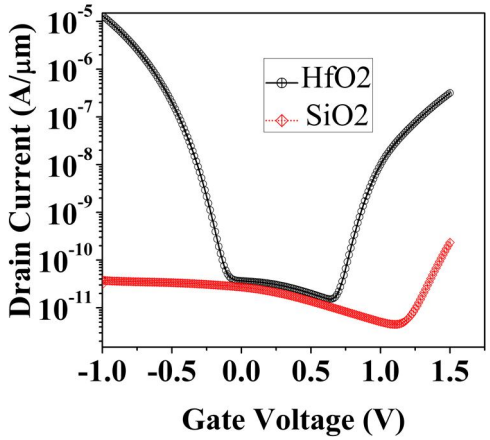

Fig.9 I_D-V_G curve at different gate oxide for Ge-DGTFET

D. Effect of Changing Source Doping Concentration

Source doping concentration is important parameter of any DGTFET to control the drain current, I_{ON} enhances while increasing source doping with respect of enhanced I_{OFF} . ON current decreases with the reduction in concentration of source doping The higher doping causes very less band bending in conduction band and valence energy bands compared to the lower doping of source. Tunneling distance is also small at source-channel interface. These parameters together cause more tunneling current as compared to the lower doped source region. In order to increase Ion, source doping needs to be kept as high as possible. In addition, the subthreshold swing also improves with increasing source doping.

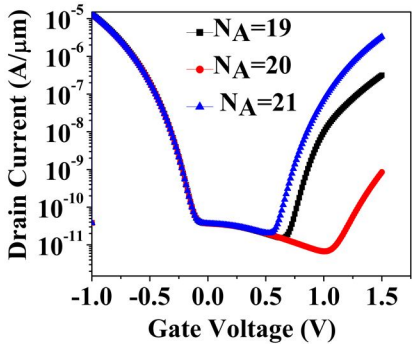

Fig.10 I_D-V_G curve at different doping conc for Ge-DGTFET

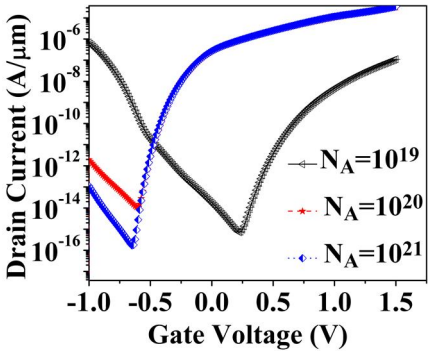

Fig.11 I_D-V_G curve at different doping conc for Si-DGTFET

IV. CONCLUSION

In conclusion, the design and physics model of Ge and Si- DGTFET are detailed through two dimensional device simulations Ge-DGTFET is shown to be able to achieve higher I_{on} as compared to Si- DGTFET. The device electrical parameters such as drain current, subthreshold slope (SS), leakage current(I_{off}), I_{ON}/I_{OFF} ratio have been obtained. It is evident from, the results that drain current is improving. Current, I_{ON} it value very low close to 10^{-6} and I_{OFF} close to 10^{-14} hence the ratio Ion/I_{OFF} is very large, whatever the nature of the gate oxide, so SS is weak. Whatever the nature of the chosen oxide, this device gives excellent I_{ON}/I_{OFF} ratio of 10^8 .Furthermore we also investigated higher source doping reduces the tunneling width and helps us to achieve a higher tunneling rate. In addition, electric field and surface potential model are also discussed.

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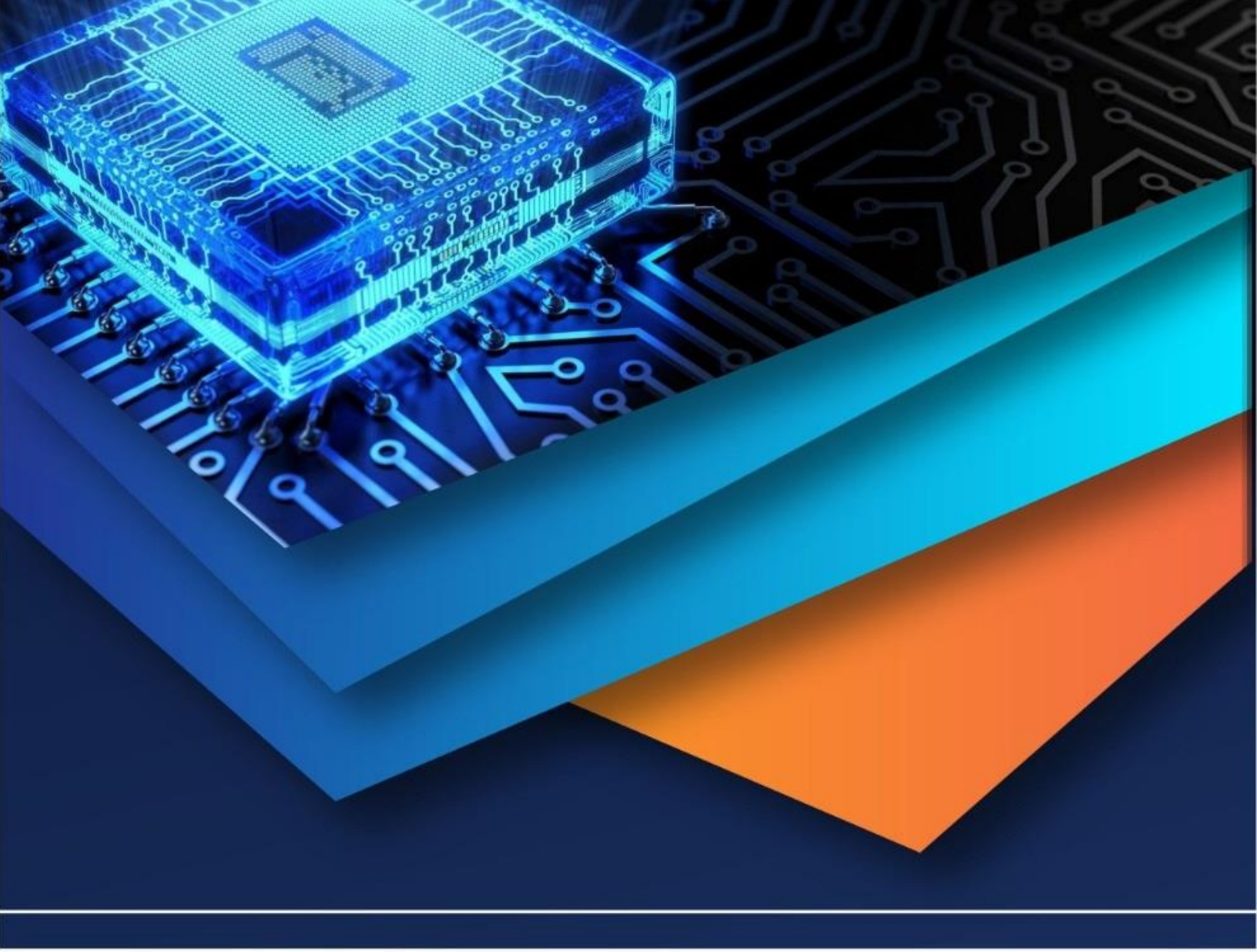

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