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Designing CMOS based Class E Power Amplifier

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Abstract: ***Here in this paper the power amplifier and CMOS has been explained. The present researches in sector of power amplifier and CMOS are also discussed here. The proposed work focus on the design and implementation of Class E power amplifier that should be CMOS technology based. The simulation of work is made in MATLAB. The design of circuit has been built of Simulink tool available in MATLAB. The proposed work would play significant role in designing application particular integrated circuits. Multi mode class e radio power amplifier has been using 30 nm CMOS technology with programming. This research has proposed Advanced CMOS RF Power Amplifier Architecture. Research has presented PAE% according to frequency. Comparison chart of Tradition researches where frequency was 5.2 to 13 ghz , 4 to 17 ghz, 6.5 to 13 ghz, 0.1 to 65 ghz,0.2 to 2.5 ghz in proposed research frequency 2.4ghz has been represented. Output power & power gain has been simulated in this section. Multi mode class e radio power amplifier has been using 30 nm CMOS technology with programming. Such system would be suitable for low power fifth generation wireless networks.***
Keywords: CMOS, MATLAB, Simulink, Power Amplifier, Class E PA

I. INTRODUCTION

Power amplifier has been considered as last block in transmitter system. It has capability to boost weak signal to needed power level. This requirement came in existence when signal is transferred. Power amplifier has been considered huge signal amplifiers. Voltage of input signal need to be high if there is needed to get a huge signal power on output Power Amplifier are classified in audio power amplifiers & rf power amplifiers refers to the Complementary Metal Oxide Semiconductor. It is popular technology in industry of computer chip design. At present time, this technology has been applied to generate the integrated circuits in several and different applications. The technology makes utilization of both P channel & N channel semiconductor devices.

Several researchers have [12] proposed a 0. 2-2. 5 GHz CMOS PA. They have used the transformer-dependent broadband Matching Network. A 0.2~2.5 GHz broadband CMOS PA has been formulated. For this the 180 nm CMOS process has been applied. It has been for a wireless transceiver. The research has considered the issues related to the integration of environment, this PA has been classified into a high-band PA and a low-band one. High-band PA obtains all elements connected on-chip. Some of the authors have [13], stated integrated Doherty Radio frequency cmos power amplifier design. It has been developed for average efficiency enhancement. Present researches are dealing with implementation of a radio frequency Doherty Power Amplifier. Its objective is to improve average efficiency. Such mechanism has been found an interesting mechanism to give efficient PA. This PA is suitable for high PAPR signal. Such signal related to present standards of communications. Many scholars have [14] introduced an RFDAC based reconfigurable multistandard transmitter in 65 nm CMOS" A transmission device which is formed on the basis of high frequency digital to analog converter was put into place for the very first time in this s work. It was put into place for the very first time in the favor of broadcasting cell phones as well as for application related to network within a 65 nano meter complementary metal oxide semiconductor methodology. The transmssion device which is formed on the basis of high frequency digital to analog converter has an organized arrangement. In order to pull off organized arrangement it uses four lower significant bit in addition to sixteen most significant bit lattice for all I as well as Q path. As a result it offers a resolution of eight bit in addition to signum.

In additional, 60GHz power amplifier [15] using 90-nm RF-CMOS methodology has been stated. 60GHz power amplifier has been described. In this system 90-nm RF-CMOS procedure has been used along with 8 metal-layers. To inductor offered by the procedure, the Q value is very low. It has been evaluated that the model is not accurate within design of MMW. Analysis as well as the design for [15] an unconditionally stable normal-drain has been developed. This design belongs to class-B Radio frequency power amplifier. It has used 90 nm CMOS technology. It has used ninety nano meter complementary metal oxide semiconductor methodlogy. In the present scenario the broadband channel required a good radio transmitter that are efficient & have less deflection. A normal channel amplifying device was so much capable that they can convert in to a one dimensional amplifying device and its performance still remains excellent when biased at or above class-B. To maintain absolute consistency as well as sufficient conversion gain at the same time is the most important and difficult task. It is required because it ensures that the power added efficiency (PAE) would not be affected by low gain. Due to this the efficiency remains good throughout. 2.45 Gega Hertz

complementary metal oxide semiconductor power amplifier [16] with high linearity was explained. 2.45 Gega Hertz high frequency complementary metal oxide semiconductor Class-AB power amplifier has been proposed.
It has high linearity & output power for WLAN. Two types of PAs were developed to demonstrate accessiblity of mechanism. The improved power amplifier with 2.4 volt supply voltage is having 22.5 dB of power gain. If there is 5 dBm increase of P1dB than fifteen percent & 5 dB updation of PAE at P1dB & IMD3 occurs.

II. RELATED WORKS

There have been several researches that are representing methods for performance improvement of multi-stacked CMOS millimetre wave power amplifiers. The research work has discussed several researches.
In 2018, Mohammad Hassan Montaseri [1] wrote to denote the improvement in Multi-Stacked CMOS mm-Wave PA. This is related and dependent on negative capacitance. The research work has provided the multi-stacked CMOS millimetre-wave PA. This proposed work is related to the negative capacitance phase detuning. It has been analyzed that it is possible to be generalized to different step detuning methods.
In 2018, Ivan Sejc[2] provide the research work on an architecture of DAC that is related to the RMS Power Detector. This detector is used for RF Applications. In the research work, they proposed a wireless receiver RF PD. This proposed tool will be used for 2.4 GHz as well as 5 GHz WLAN bands. Here the offset compensation and measurement mehod has been proposed. It has been formulated within 65 nm CMOS method.
In 2017 Xianghong Gao [3] researched on three level. In the research work, design with implementation of a three level PA within 65nm CMOS method has provided the research work. With the use of neutralization method the proposed PA can offer a peak power achieves. The PA uses 0.2mm2 chip area with the pads.
In 2016 Eli Schwartz [4], provided the introduction of 20dBm CMOS RF PA. The updated technique to PA architecture in CMOS for 802.11ac is presented here. It has been analyzed that it is able to get -35dB EVM along with output power.
In 2016, Gabor Varga[5] made design of an integrated CMOS. A significant active type of genuine root mean square power detecting device was put into place for the very first time in support of communication frequency demands. For example ti can said that Cognitive Radio. The radio frequency capacity of Power detecting device protects a range of 0.5 Gega Hertz to 3 Gega Hertz along with an effective extent of 50 decibel & a lowest recognizable capacity of fifty ohm. These structures make unlike employment of a fake and different balancing device. Its input impedance is very huge. It makes possible to put them over high impedance and also on fifty ohm lines.
In 2015, Aritra Banerjee [6] described High efficiency multi-mode outphasing RF power amplifier. A multi-channel class-E phase shift radio frequency power amplifing device whose performance was very good is introduced in combination of a idle device. With the help of multi channel power amplifing device the performance at minimum power levels can be incresed. It can be achieved by switching ON & OFF of a specific devision as well as by means of device which will increase the performance. The power amplifing device which has been put forward in this paper was prepared inside a forty five micro meter complementary metal oxide semiconductor methodology.
In 2015, Soroush Dehghani [7] described A four to seventeen Giga Hertz Darlington overlapping high speed environment. In support of high speed related examinationan middle stage inductor as well as series peaking RL circuit are used. An output long wavelength corresponding device is adopted for the purpose of gain maintaince & power consistency at highest frequency. It was represented through the determined consequencies that power amplyfing device which was introduced in this paper , shown a gain of ten decibel on the basis of four to seventeen gigahertz under 2-decibel ripple, & excess capacity in between the range of sixteen to eighteen dBm with power added efficiency better than ten percent & power consumption of three hundred and six mega watt. The chip size is only 0.67 mili meter.
In 2010, H. Wang [8] introduced A CMOS Broadband Power Amplifier with Matching Network. A design methodology is also presented in detail. It has been done to change a canonical band pass network in offered matching system.
In 2010, P. Amplifier [9] they put into place for the very first time a monitoring load for the purpose of power efficiency maximization inside a radio frequency to direct current inverter device. A monitoring load device for radio frequency inverters was explained . A monitoring load is put into place for the very first time in order to make the best use of radio frequency to direct current transformation efficiency because the radio frequency input power to rectifier changes. The device includes two rectifiers with two monitoring circuits.
In 2011, B. Ku introduced [10] A Wideband Transformer-Coupled CMOS Power. The research work has proposed the wideband transformer-coupled CMOS PA. On-chip transformers for transmission-line have been utilized as key components to match the

networks at output, input as well as at interstage. The wideband on-chip transformer has been harnessed lacking of any extra inductive application. Therefore wideband power benefits characteristic could be achieved.

In 2016, H. Wu described [11] Analysis & Design of an Ultra broad band Stacked Power Amplifier in CMOS Technology. The research work has proposed the calculation with the design of a two level stacked powers is also determined here.

In to parasitic of on-chip inductors, 2009 Munir M. El-Desouki et al [17] discussed influence of on chip Interconnections. It has been analyzed over the CMOS radio frequency connected circuits. Achieving power- and area-sufficient fully connected transceivers can be studied as issue faced at the time of designing of high-frequency electronic circuits appropriate with the biomedical apps or WSNs. Power losses connected transistors as well as the interconnections. Such are posed design issues in full integration. It is the connection is of power-efficient CMOS radio-frequency connected to circuits.

In 2009, Niklas Zimmermann [18] made system of an Radio frequency based DAC in 65nm CMOS. It is performed in case of transmitters that are multi standard and multimode. Their research work has proposed a radiofrequency digital-to-analog converter. The RF-DAC makes connection of DAC along with mixer functionality within building block which is single. It has basis for a modulator which is direct-digital vector. Such has been utilized in reconfigurable broadband. Along with this it is applicable in multi standard transmitters in the case of mobile transmission.

In 2008 Sheng-Yi Huang et al [19] was put into place for the very first time a most up to date spurious channel radio frequency batteries inside a 0.13 micro meter complementary metal oxide semiconductor methodlogy" An economical radio frequency battery whose formation takes place inside a latest 0.13 micro meter complementary metal oxide semiconductor methodlogy was bring in to limelight from this work. With the help of normal N-well as well as superficious drain insulation method the efficiency of power can be incresed because this process creates a high resistivity zone. The need of additional covers, expenditure and treatment methods are not required.

In 2008, Francesco Carrara [20] discussed Methodology of RF CMOS Power Amplifier. In this research security of CMOS power amplifiers for load mismatch has been found. Research proposed closed-loop protection circuit. It is rely on new current-mode detection. It is also considering comparison mechanism. Efficient RF efficiency and VSWR ruggedness has been considered at the same time.

In 2006, Huang Min Zh et al [21] An Input circuit for the monitoring of Class F Power amplyfing device stated an input control circuit for pushing an overlapping period of class F radio frequency power amplyfing device in penetrating micron sized complementary metal oxide semiconductor methodology has been presented. The input driver circuit would deliver an improvement to high frequency power amplifier's efficiency by reducing drain current distortion & provide better breakdown voltage protection for transistor. The proposed input driver & class F power amplifier are formed on the basis of Silterra high frequency complementary metal oxide semiconductor 0.18mum technology & simulated using Hspice.

In 2005, Kwyro Lee et al [22] offered semiconductor technology's impact. Its impact has been analyzed on CMOS RF. Digital circuits for application wirelessly is presented here. Both forward scaling of energetic application inverse scaling of interconnection layer. It is interconnection layers along with effectively thicker whole dielectric and metal layers. It is able to offer helpful scenario applicable in all passive application. Finally, impact of CMOS scaling on several digital circuits has been developed. Here the digital modem blocks are considered. Along with this the digital calibration circuits as well as the switching RF power amplifier are determined.

III. DESIGNS AND IMPLEMENTATION

A. Design of RF power detector

High frequency Power sensors are analogical appliances. There is folder of exponential intensifiers, TruPwr™ root mean square sensors apart from Peak as well as Envelope sensors in addition to consecutive Log Video identification intensifiers. It has identification intervals which is almost equal to hundred decibels. High frequency Power sensors are utilized in request like Transmit/Receive Power Measurement. They are frequently used for providing Input safety, for the determination of waste and for recognition of high frequency oscillation. These detectors can be used in universal resource locator, cyber war. High frequency power sensors are also used for the accurate determination of high frequency Power in Test , for the assessment of materials in addition to the field of medical science.

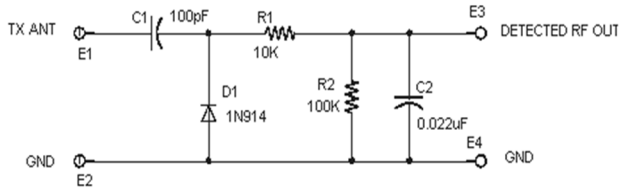

Fig 1 RF Power Detector

B. Design Of CMOS

In complementary metal oxide semiconductor methodology, negative-type transistors and positive type transistors has been used for the establishment of reasonable qualties. A particular signal which can start a transistor of one type can be utilized in order to shut down a transistor of different type. Such type of features supports the development of logical gadgets by means of switches in the absence of of a pull-up resistor. In complementary metal oxide semiconductor logic gates an assortment of negative type metal oxide semiconductor field effect transistor are organized inside a pull-down network in the middle of output & low voltage power supply rail (Vss or many times ground).

In comparison to load resistor of negative channel MOS logic gates, complementary metal oxide semiconductor logic gates have an assortment of positive type metal oxide semiconductor field effect transistor inside a pull-up network in the middle of output & higher-voltage rail which is sometimes abbreviated as Vdd.

Therefore in conditions where the gates of negative-type transistors and positive type transistors are connected to identical input, positive type metal oxide semiconductor field effect transistor would start if negative type metal oxide semiconductor field effect transistor is OFF, & vice-versa. The networks are organized in such a way that if one transistor is in ON state , then other will be in OFF state for any input array as illustrated in the diagram below.

complementary metal oxide semiconductor offers generally broadband, low power dissipation, high-frequency sound boundries in both states. It has been working within a broad spectrum of source as well as input voltages as long as source voltage is inflexible. In addition to this, for the excellent knowledge of Complementary Metal Oxide Semiconductor operation,a complete explanation related to complementary metal oxide semiconductor logic gates is illustrated below.

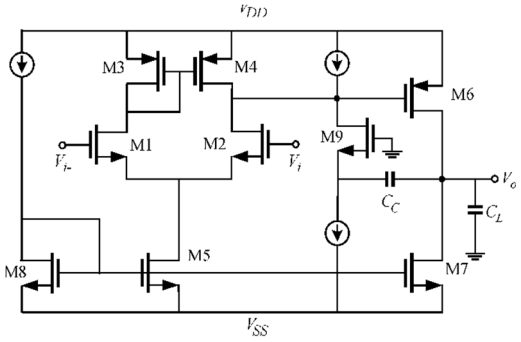

Fig 2 Circuit design of CMOS

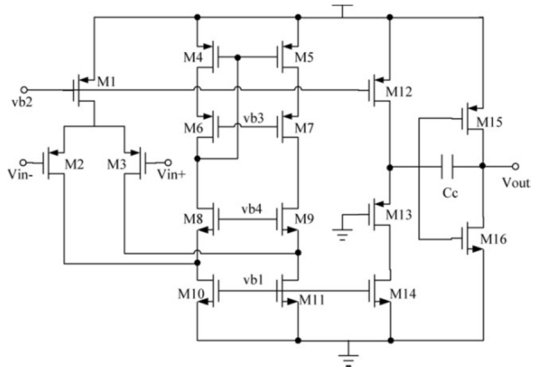

Fig 3 A Low power dissipation high speed CMOS

IV. CALCULATIONS EQUATION

Research has designed of RF power detector for 2.4ghz & 5ghz on 30nm CMOS technique. Doherty principle has been applied. It is used to a 2.5ghz integrated power amplifier over 30nm cmos mechanism.

In proposed work frequency is 2 to 5 (GHz) & PAE% has been simulated accordingly. The following chart is representing PAE% with respect to Frequency. The simulation has been made in MATLAB.

Table 1 the PAE% with respect to Frequency

FREQUENCY(GHz)	PAE (%)
0.5	23
1	15
1.5	13
2	12
2.5	8
3	7
3.5	6
4	5.5
4.5	5
5	4.5

```
frequency=[0.5 1 1.5 2 2.5 3 3.5 4 4.5 5]
pae      =[23  15 13 12 8 7 6 5.5 5 4.5 4]
plot(frequency,pae)
xlabel('Frequency')
ylabel('PAE%')
title('PAE of power frequency')
```

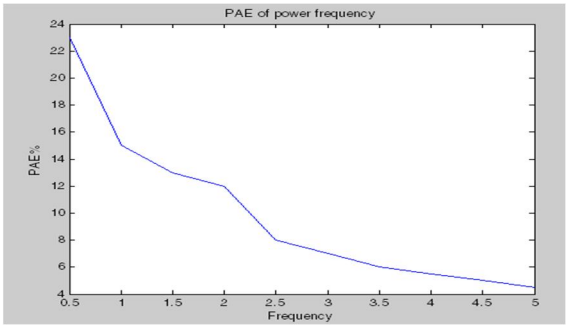

Fig 4 Graph plot (Frequency & PAE%)

Following chart is representing the optimum load of PA versus frequency here z_opt in case of PAE ROPT , PAE_IOPT, POUT ROPT, POUT_IOPT has been represented.

This chart represent Psat, Power Gain , Max PAE, S11 in dB, Chip area in mm^2, process in nm.

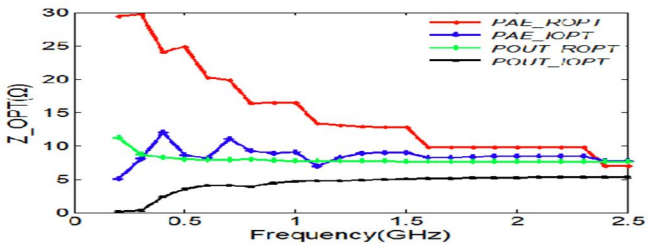

Fig 5 Optimum load of PA versus Frequency

In case of Tradition researches frequency was 5.2 to 13 ghz , 4 to 17 ghz, 6.5 to 13 ghz, 0.1 to sixty five ghz,0.2 to 2.5 ghz in proposed research frequency lies between 2.4ghz & 5ghz.

Table 2 Performance Comparison With Recent Researches

	Frequency (Ghz)	Psat	Power Gain(dB)	Max PAE	S11	Chip area (mm^2)	Process (nm)
[8]	5.2~13	25.2	17.5	21.6	<-10	0.7	90
[9]	4~17	18	9~15	12	<-9	0.67	180
[10]	6.5~13	21.5	25.3	20.3	N/A	0.63	180
[11]	0.1~6.5	22	16.9-19.9	20	<-11	0.64	180
[12]	0.2~2.5	22.42	10.44~14.81	23.3	<-10	2.41	180
This work	2.4	22.21	20	17	<-10	0.5	30

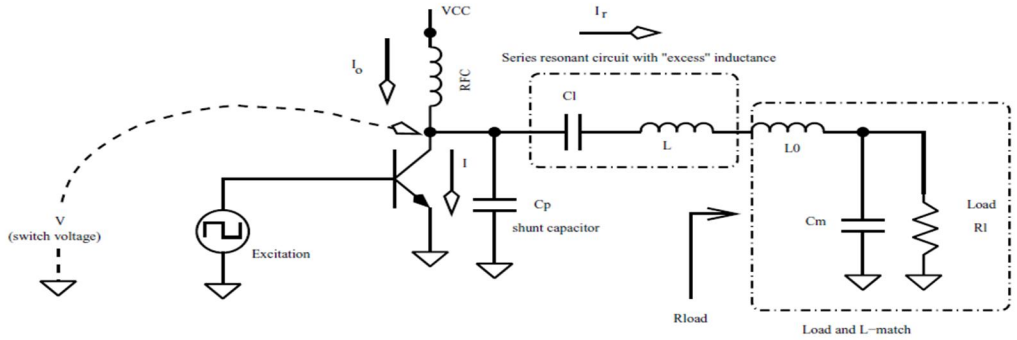

Fig 6 Design of Class E amplifier

A. Class E amplifier

Class-E conditions are completed at the time when switch closes at $\omega t = 2\pi n$:

$$V(\omega t)\big|_{\omega t=2\pi n} = 0$$
$$\frac{d}{d(\omega t)}V(\omega t)\bigg|_{\omega t=2\pi n} = 0.$$

The voltage across switch has been provided by V (wt) and present via switch has been represented by I(wt). it has been done at any instant in normalised time wt. For expediency, a table related to variables relavent for analysis has been listed here such as:

Table 1: Table of pertinent variables

Variable description	Variable	Notes
DC supply voltage	V_{cc}	
DC supply current	I_0	
Load current	$I_r(\omega t)$	single sine wave
Shunt capacitor current	$I_c(\omega t)$	only when switch is open
Switch current	$I(\omega t)$	Only when switch is closed
Shunt capacitor value	C_p	
Series capacitor value	C_l	
Series inductor value	L	$L = L_{res} + L_{ext}$
Series resonant inductor	L_{res}	
Series loading inductor	L_{ext}	extra inductance for Class-E
L-Match inductor	L_0	transform load impedance
L-match capacitor	C_m	
Load resistance	R_l	usually 50 Ω
Load resistance	R	before L-match; a low value

Using results of 2, current through capacitor immediately after switch closes must be zero, i.e.

$$I_c(\omega t) = \omega C \frac{d}{d(\omega t)}V(\omega t) = 0.$$

B. Design Process

1) Choose power supply voltage (Vdd).
2) It decides Vdd(max) of FET at nearly 3.5 times Vdd
3) Choose target power level
4) It decides optimum value of C1 & optimum load impedance
5) Decide the value of C2 and L2 from Excel Worksheet

C. Matlab Simulation

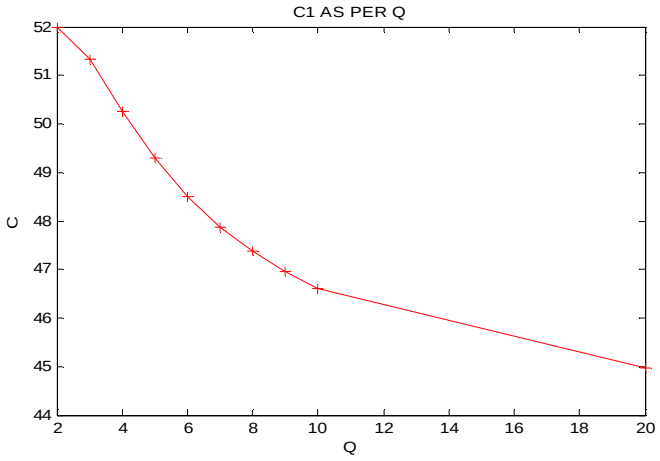

Fig 7C1 as PER Q

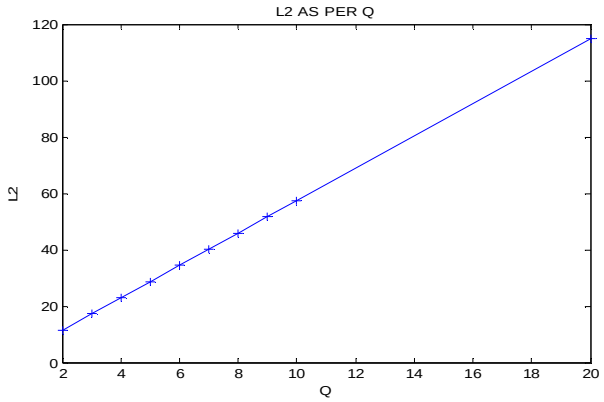

Fig 8 L2 AS PER Q

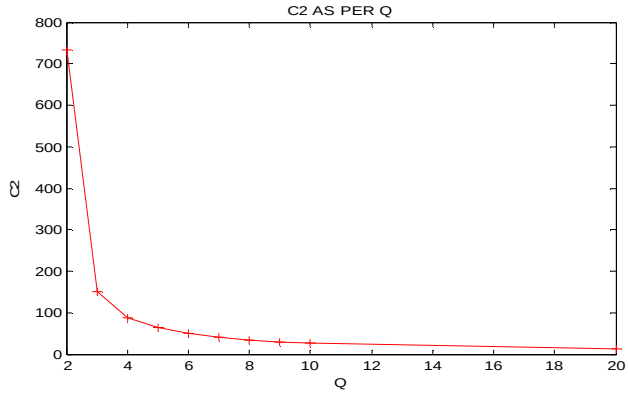

Fig 9 C2 AS PER Q

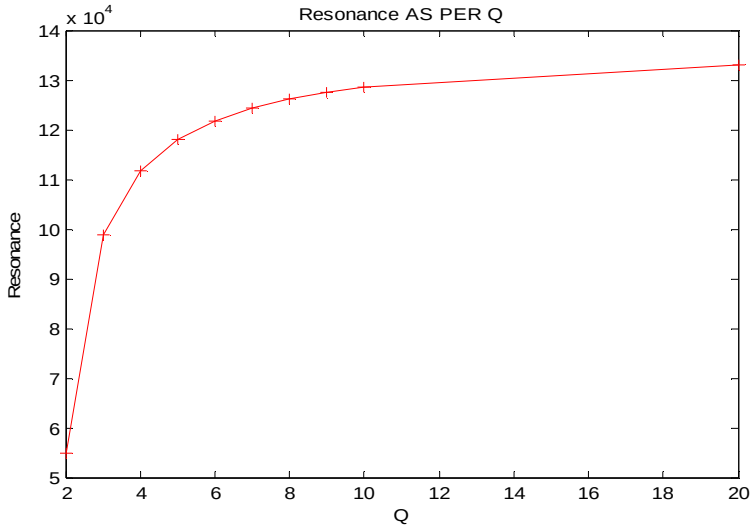

Fig 10Resonance as per Q

V. SCOPE OF RESEARCH

Several areas are there such as Precise RF Power Measurement in Test and as Measurement. Analysis related to Materials with HealthCare are there in which the RF power detectors. The Research work would be beneficial in field of Radar, Electronic Warfare. This research is beneficial where CMOS technology is digital IC designs. It would be useful in field of Computer memories, CPUs, Microprocessor designs, Flash memory chip designing.

The proposed is going to play essential role in designing application specific integrated circuits. Multi mode class E radio power amplifier having 30 nm CMOS technology with programming is proposed. This research has proposed Advanced CMOS radio frequency Power Amplifier Architecture. It has been proposed in case of Low Power 5G Wireless Networks.

VI. CONCLUSION

Research has presented effect of PAE% according to frequency. Tradition researches in which frequency was 5.2 to 13 Ghz , 4 to 17 ghz, 6.5 to 13 Ghz, 0.1 to 65 ghz,0.2 to 2.5 Ghz have been explained & proposed research where frequency 2.4Ghz has been represented. This type of research has been proved significant in wireless communication and CMOS based application. Output power & power gain has been simulated to represent effect of change in frequency & process. It has been observed that influencing factors are Psat, Power Gain, Max PAE when S& frequency is modified.

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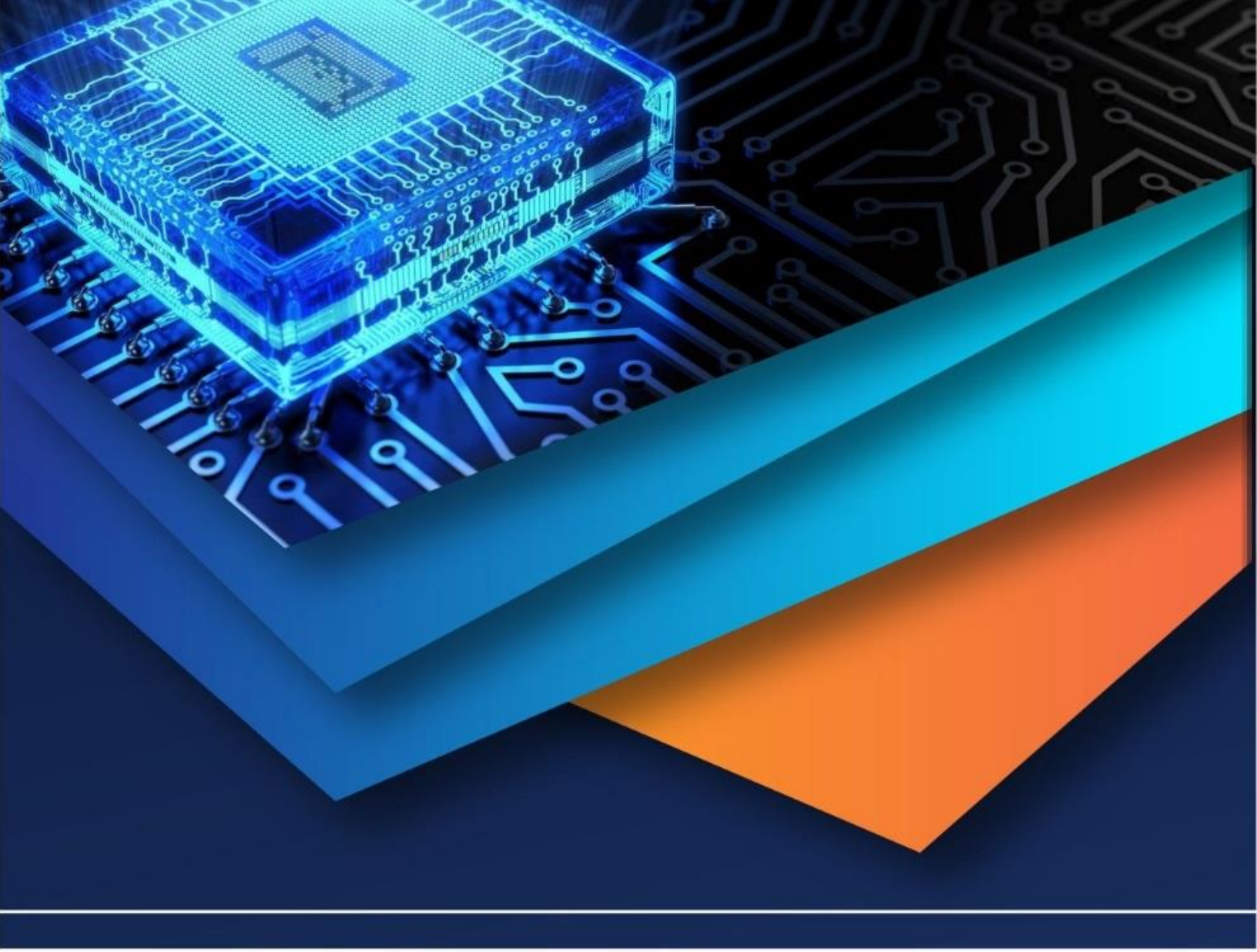

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