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Voltage THD Reduction for Cascaded H-bridge Multi-level Converter using Sliding Mode Control

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Abstract: ***This paper presents a detailed harmonic analysis in terms of Total Harmonic Distortion (THD) for different power circuit topologies of multi-level inverter fed induction motor drives. The most common multilevel inverter topologies are the neutral-point-clamped inverter (NPC), flying capacitor inverter (FC), and cascaded H-bridge inverter (CHB). This work is to analyze the performance of all the power circuit topologies of multilevel inverter with various multi carrier PWM control techniques. Simulation and results shows that the superiority of these inverters over two-level pulse width modulation based inverter fed drives.***

Keywords: ***Multi-level Converter, Pulse Width Modulation, Total Harmonic Distortion***

I. INTRODUCTION

The expanding requirement for electrical vitality sources urges individuals to utilize inexhaustible power. The most prevalent sustainable power source is photovoltaic. Photovoltaic is a segment that uses daylight to deliver voltage. The subsequent voltage of a photovoltaic is a DC voltage. DC voltage can't be straightforwardly utilized on the grounds that the current electrical framework is commanded by the electric burden with AC voltage source. Subsequently, it requires an instrument to change over DC voltage into AC voltage. Numerous innovative improvements concerning the transformation of voltage from DC to AC voltage have been finished by the scientists [1].

Inverter is a gadget used to change over DC voltage into AC voltage that uses the exchanging states of a change part to create AC voltage. The yield voltage of the inverter still has a low voltage quality that is demonstrated by an enormous Total Harmonic Distortion (THD). This voltage requires a channel to deliver the yield voltage with least THD voltage in order to create a reasonable sinusoidal wave for the voltage source [2]. THD is an estimation of the nature of voltage or current. In typical conditions the yield voltage structure is a sinusoidal wave where THD is near or equivalent to 0 (zero). THD is the rate an incentive between the all out segments of music with its principal parts.

The more prominent the level of THD, the more prominent the danger of gear harm. As per the guidelines by IEEE STD 519-1992, the standard Harmonic Voltage Limits on the general framework is 5% [3], and 8% is for Pacific Corp standard [4]. On the off chance that the THD esteem is more noteworthy than the THD standard, it can prompt the demolition of electrical hardware, the consuming of link/channel, overheat on the electric engine, and mistake on the electromechanical estimation of KWH meter. To beat this, the staggered inverter was worked to improve the yield voltage nature of the transformation. Staggered inverter yield has preferable voltage quality over inverter [5]. The voltage quality is shown by littler THD. This is on the grounds that staggered inverters produce voltage wave on stages as per a level that takes after a sinusoidal structure. One kind of staggered inverter is a staggered inverter clip diode [6].

This sort would be utilized for the transformation instrument from DC voltage to Air conditioning voltage. The yield voltage type of the staggered inverter relies upon the exchanging technique utilized. Much look into has been done on the point of the exchanging strategy [7]. Common strategies were tried including Pulse Width Modulation (PWM), Sinusoidal Pulse Width Modulation (SPWM) and Third Harmonic Pulse Width Modulation (THIPWM) to create voltage with least THD voltage. With the outcomes exhibited in different papers and diaries, the specialists attempted to look into the exchanging technique utilized in staggered inverters to get a base or exceptionally little THD voltage.

In this investigation, the analysts have made altered PWM for staggered inverter exchanging with the goal that the THD yield voltage is least. Changed PWM is finished by including a 50 Hz sinusoidal reference signal with a sinusoidal sign having a specific plentifulness and recurrence. The recurrence of the snake signal is the recurrence at which the estimation of the individual consonant voltage shows up (n symphonious).

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II. MULTI LEVEL CONVERTER

Figure 1 shows the staggered converter adjustment strategies. The tweak control plans for the staggered inverter can be isolated into two classes, major exchanging recurrence and high exchanging recurrence PWM, for example, staggered bearer based PWM, particular consonant end and staggered space vector PWM Multilevel SPWM needs different transporters. Every DC source needs its very own transporter. A few multi-transporter procedures have been created to diminish the mutilation in staggered converters, in view of the traditional SPWM with triangular bearers. A few techniques use bearer aura and others use stage moving of various transporter signals. By summing up, for a 'n' level staggered inverter, (n-1) bearers are required. The usage of the different bearer PWM procedures that is workable for staggered inverters are [3]-[6]:

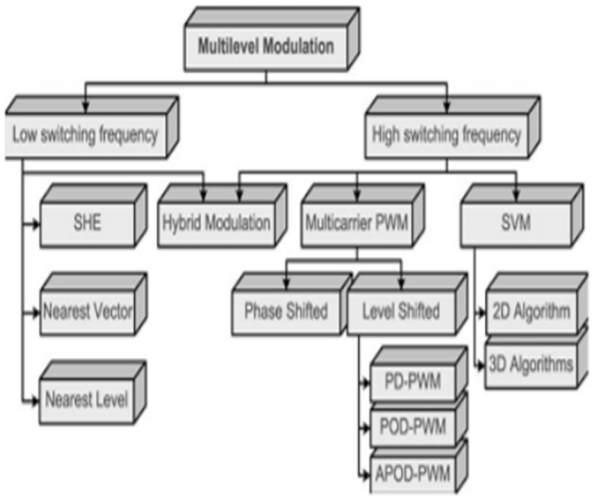


Figure 1: Multilevel converter modulation methods

A. Level Shifted PWM (LSPWM)

This modulation method is especially useful for NPC converters, since every bearer can be effectively related to two power switches of the converter. LSPWM prompts less contorted line voltages since every one of the transporters are in stage contrasted with PSPWM [8]. Moreover, since it depends on the yield voltage levels of an inverter, this standard can be adjusted to any staggered converter topology. In any case, this strategy isn't favored for CHB and FC, since it causes an uneven power appropriation among the various cells. This creates input current mutilation in the CHB and capacitor unbalance in the FC contrasted with PSPWM [3]-[6]. Figure 6 shows the LS-PWM transporter plans.

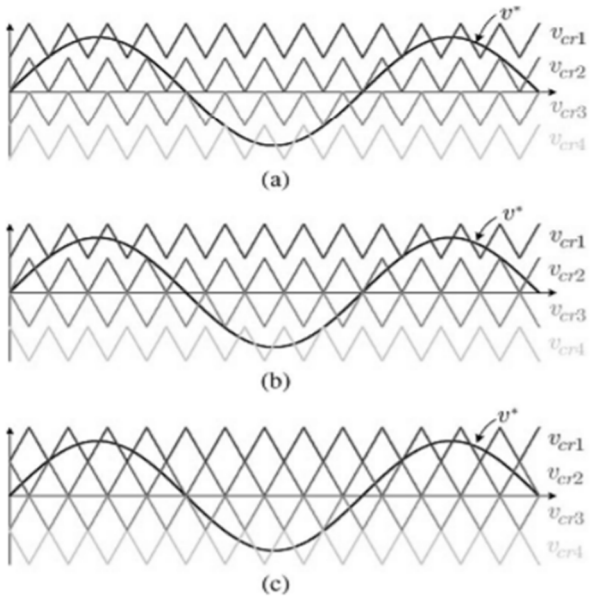


Figure 2: LS-PWM carrier arrangements: (a) PD, (b) POD, and (c) APOD.

B. Phase Shift Pulse Width Modulation

PWM signals are beat trains which are applied to the entryway of changes to play out the activity of converter. The beat trains are fixed recurrence and size and variable heartbeat width [5]. There is one beat of settled degree in each PWM period. Regardless, the width of the beats changes from period to period as showed by a directing sign. Right when a PWM banner is associated with the door of a power transistor, it causes the turn on and executes intervals of the transistor to change beginning with one PWM period then onto the following PWM period as showed by a similar controlling sign and in this way working of converter starts. The repeat of a PWM banner must be considerably higher than that of the managing signal, the significant repeat, with the ultimate objective that the essentialness passed on to the load depends for the most part on the tweaking signal. The control of yield voltage is finished using beat width balance.

This procedure utilizes a lot of bearers that are all stage moved. The four triangular transporters are stage moved by 90o. Utilizing a similar inspecting period, it has multiple times bigger exchanging recurrence than that of different strategies. This procedure is uncommonly considered for FC and CHB converters. Since each FC cell is a two-level converter, and each CHB cell is a three-level inverter, the conventional bipolar and unipolar PWM procedures can be utilized, individually. Because of the seclusion of these topologies, every phone can be tweaked autonomously utilizing a similar reference signal.

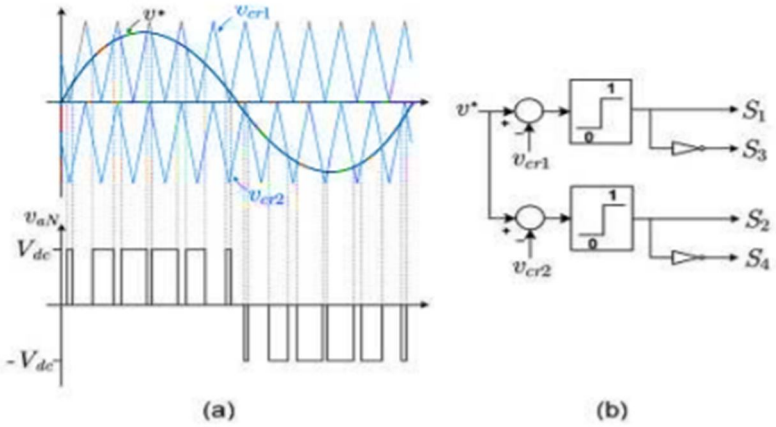


Figure 3: Phase Shift PWM

III. ANALYSIS OF OUTPUT LINE TO LINE VOLTAGE HARMONICS

In this area, recreation results utilizing the proposed control systems are introduced. Reproduction has been performed in Matlab/Simulink. To assess the inverter topologies for an assortment of utilizations, transporter frequencies of fc= 450Hz ..1050Hz are accepted for all researched inverter topologies. This range is run of the mill for accessible mechanical medium voltage drives [11]. Additionally all the inverter topologies are associated with the Induction engine load. To approve the proposed technique, the reproduction of ordinary two level PWM voltage source inverter (VSI) bolstered acceptance engine is performed and the yields are acquired. Figure 4 shows the music delivered by two level VSI and it is recorded to be 38.68%. Likewise the seventh symphonious is predominant in this consonant range.

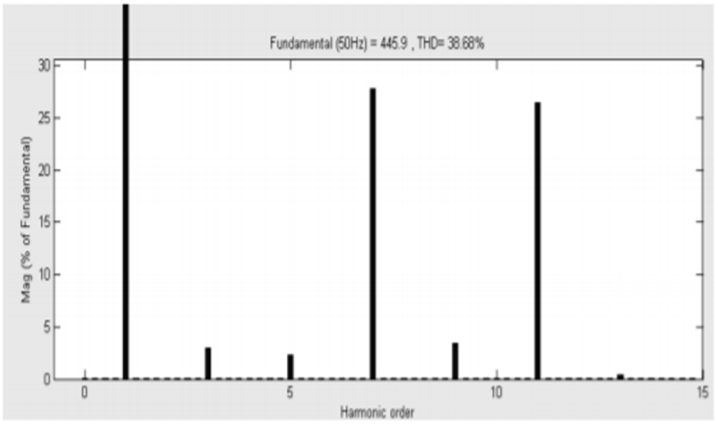


Figure 4: Harmonic spectrum of line voltage for Two level VSI

IV. PROPOSED METHODOLOGY

SMC configuration includes two stages: (I) Selection of stable hyperplane(s) in the state/blunder space on which movement ought to be limited, called the exchanging capacity, and (ii) Synthesis of a control law which makes the chose sliding surface appealing.
A direction beginning from a non-zero starting condition, develops in two stages: a) Reaching mode, in which it arrives at the sliding surface, and b) Sliding mode, in which the direction on arriving at the sliding surface, stays there for all times and along these lines advances as per the elements indicated by the sliding surface.

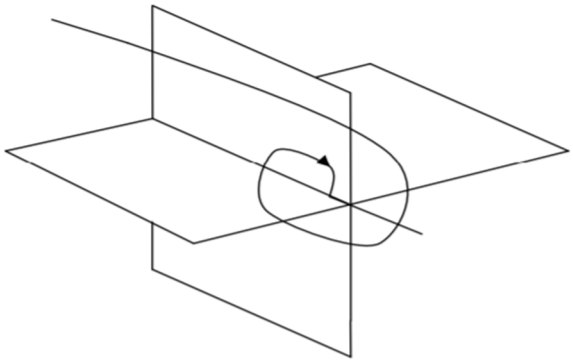
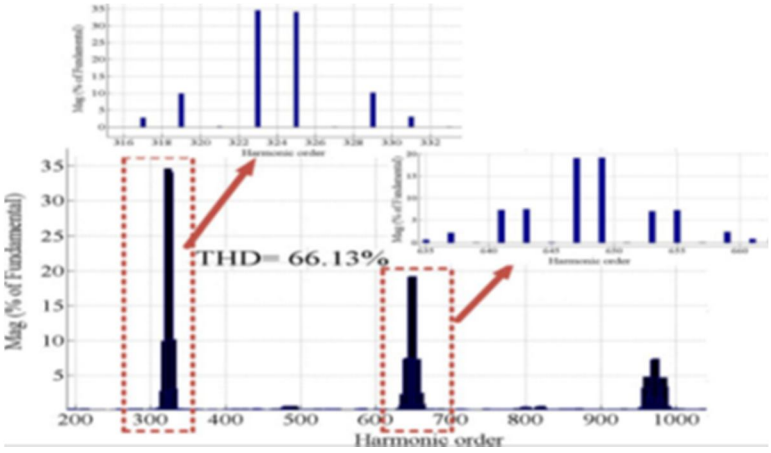


Figure 5: Sliding Mode Control

Sliding mode control is a particular type of the variable structure control system (VSCS), which is characterized by a discontinuous feedback control structure that switches as the system crosses certain manifold in the state space to force the system state to reach, and subsequently to remain on a specified surface within the state space called sliding surface. The switching function (sliding variable) is a function of the states and the sliding surface represents a relationship between the state variables. The system dynamics when confined to the sliding surface is referred as an ideal sliding motion and represents the controlled system behaviour, which results in reduced order dynamics with respect to the original plant.

V. SIMULATION RESULT

Inside the structure of the proposed strategy, the dynamic time of heartbeats at the subsequent inverter is generally balanced inside exchanging interim (contrasted with the first VSI). The stage voltage sounds are detailed for double inverter balanced by NSPWM; at that point, ideal modification is distinguished by means of a three-dimensional bend of stage voltage THD versus balance file (MI) and stage edge removal (PAD). Because of the constraint of MI in NSPWM, the ideal yield voltage is integrated with changing MI as well as PAD between references of two VSIs. Moreover, NSPWM intrinsically exploits better proficiency contrasted with customary space vector tweak because of exchanging just two stages inside an interim (by bracing one stage to positive/negative dc-rail). The double VSI provided by two separated dc sources is collected in the research facility to tentatively assess the THD decrease highlight of the proposed technique; likewise, the reenactment results got by methods for a MATLAB/Simulink condition show close concurrence with exploratory information.



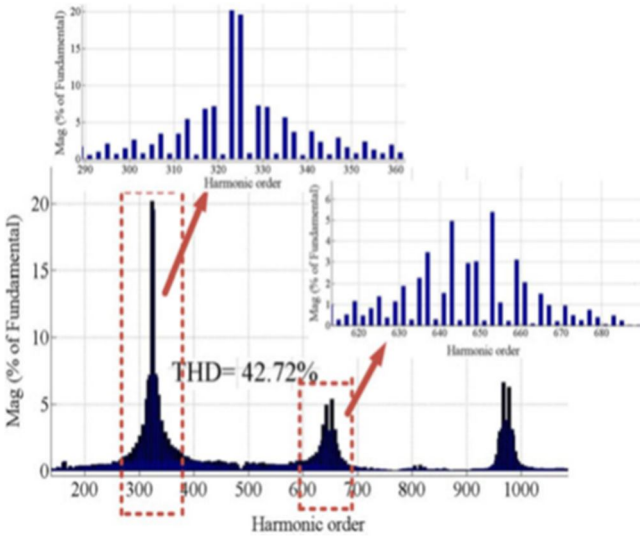


Figure 6: Total Harmonic Distortion

VI. CONCLUSION

This paper proposes the three staggered topologies and they spread various requirements for various sort of uses. The multi bearer PWM tweak control strategies are acquainted in these topologies with get diminished sounds at the yield voltage THD and to improve the productivity of the inverter. Subsequently the proposed inverter topologies with the proposed regulation strategy control procedures are approved through the nitty gritty reproduction investigation alongside the regular two level voltage source inverter, and it was demonstrated that the yield voltage levels are expanded in the staggered inverters to approach close to sine wave and to get the higher voltage and diminished Total Harmonic Distortion.

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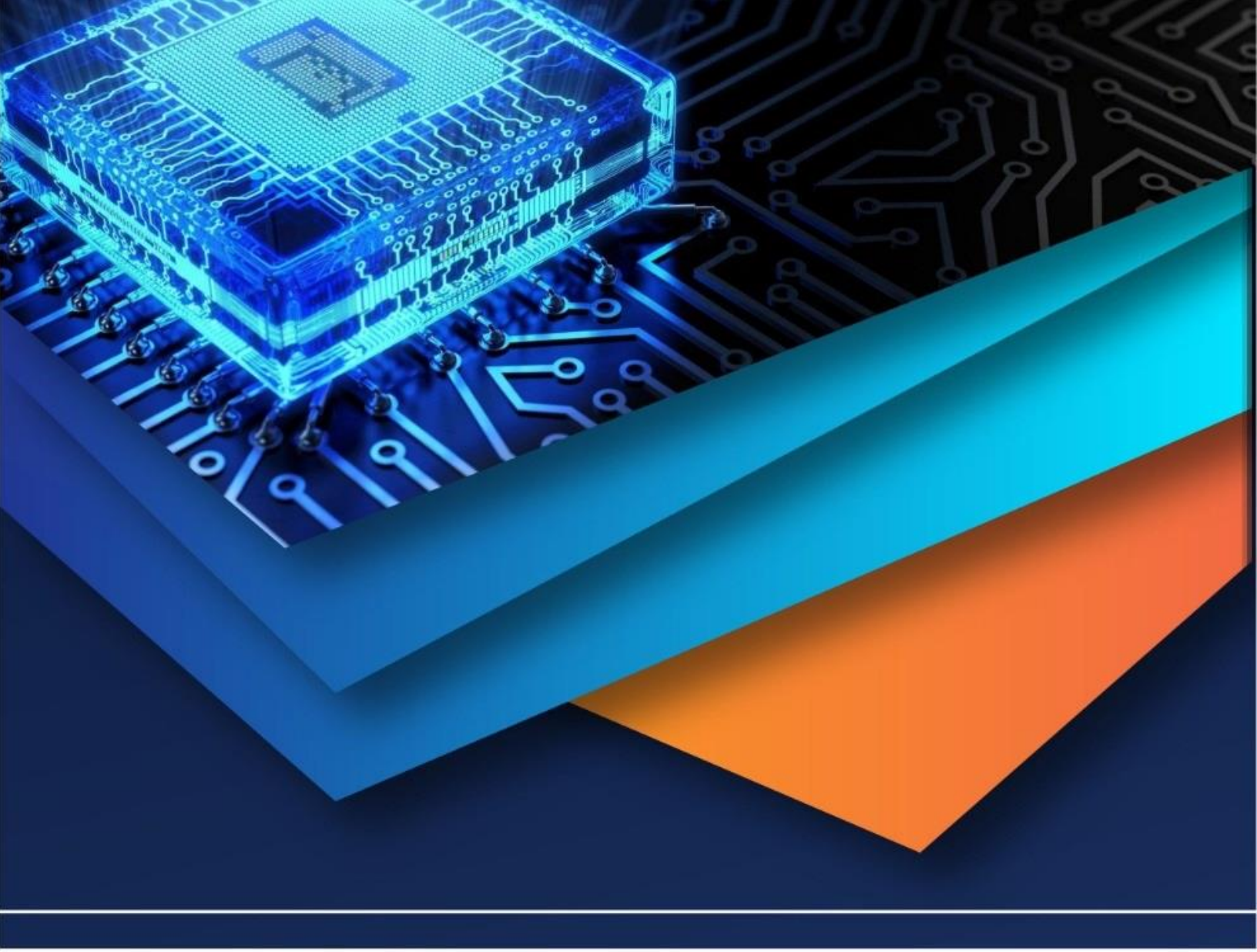

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