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ASIC Implementation of Serial Commutator Fast Fourier Transform for Real Valued Signal

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***Abstract:** This paper presents serial pipelined Fast Fourier Transform hardware architecture for real valued signal. The SC-RFFT uses bit exchange circuitry for serial data at intermediate stages. The observation made from proposed architecture is that, in radix 2 FFT algorithm one fourth of the samples are rotated at first stage and remaining stages requires half rotators. For real valued input signals numbers of butterflies are reduced, hence clock pulses. As a result the proposed architecture has less hardware requirement compared with serial commutator for conventional FFT.*

***Keywords:** RFFT, Serial Commutator, Bit-Exchange, ASIC implementation, Pipelining*

I. INTRODUCTION

As VLSI technology is growing day-by-day, DSP and communication system devices also demands high speed computation and minimum hardware requirement.

DFT and FFT are widely used and important area of DSP. Frequency domain analysis of signal provides information which is difficult to analyse signal in time domain. So, different transform techniques can be used to analyse signal in frequency domain. So, DFT is one of the popular technique. FFT is an efficient algorithm to implement DFT. FFT removes redundant calculations and reduces the arithmetic units, so it is much faster.

There are many techniques have been proposed to increase the speed of FFT algorithm in last few years. The arithmetic complexity and its recursive structure decide the performance of FFT structure.

The various architectures are already available for computation of FFT. But pipelined architectures are more popular and suitable to process high speed data.

The conventional architectures of FFT use dedicated RAM to perform butterfly operations. In contrast, the pipelined architectures directly begin FFT computation instead of storing input in dedicated RAM.

Mainly, there are two types of Pipelined FFT's. First one is serial pipelined FFT process, which computes one sample per clock cycle. And second type is parallel pipelined FFT process which computes several samples in parallel per clock cycle.

Over the period the development happened widely in Parallel pipelined FFT architecture. The multipath delay commutator reduces the number of required amount of butterflies, memory and rotators. In contrast, the efficient development in serial pipelined architecture is not reached up to mark of parallel ones yet. In serial pipeline, the single-delay commutator (SDC) FFTs improves the use of butterflies and rotators but it takes larger memory.

Therefore, in every case, there is trade-off among butterflies, rotators and memory.Above mentioned both type of pipelined FFT architectures can compute both real and complex signals. But, most of signals which receive from outside world are real-valued. So, complex FFT processors are not efficient to compute real-valued signals.

So, customized real-valued FFT (RFFT) signal is required, which increases hardware efficiency over complex FFT processors. In N-Point DFT, X[k] is representation of x[n], and if x[n] is real valued then by Hermitian symmetry property, X[N-k] = X[k] implies, out of N outputs of FFT algorithm N/2 -1 are conjugate symmetry. So, these conjugate symmetry points become redundant and are not necessary to compute it. For 16-point radix-2 FFT, then half of the butterfly and multiplication terms become redundant if this property applied to Data flow graph (DFG). Moreover, many real-time applications such as video, audio, image, mobile applications and biomedical applications require RFFT.

So, operation on real valued signal is done by either parallel pipelined or by serial pipelined architectures. The architecture for the parallel pipelined FFT processors for real valued signal is proposed [2]. This paper presents the Serial commutator for real valued FFT (SC-RFFT).

This SC-RFFT uses bit-exchange circuit for data management of serial data at intermediate stages. This architecture requires less number of registers, rotators and butterflies. The sections organised as follows. Section II gives explanation of proposed architecture for SC-RFFT. Section III compares the computation complexity using proposed architecture.

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II. PROPOSED ARCHITECTURE

In N point DFT, with Radix-2 base $N=\log_2 N$ stages are required. In this paper, the proposed model if for N=16 points. So, n=4 stages are required. Here, all 16 point inputs are received first atage of serial commutator are real.

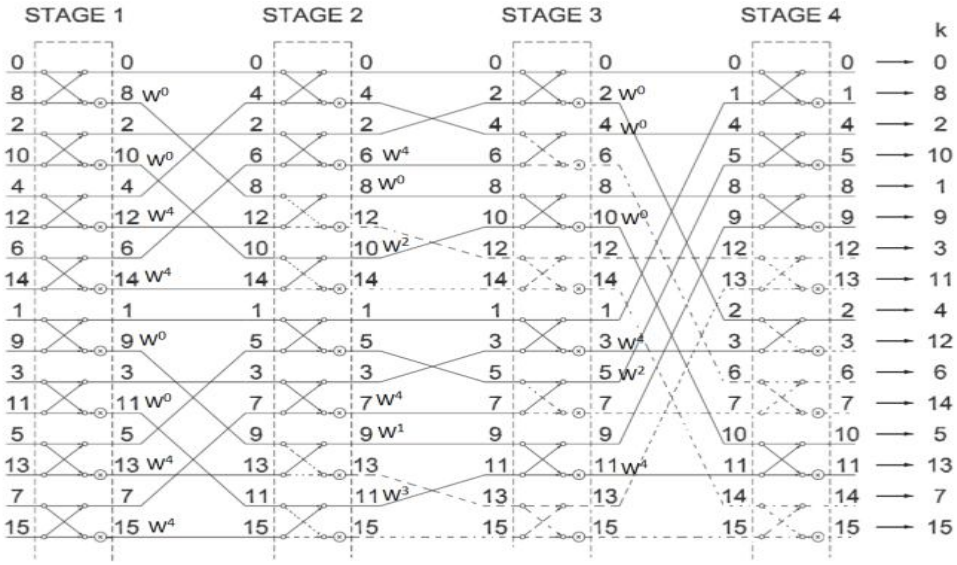

Fig1. Data Flow Graph of radix-2 SC-RFFT

So, any radix-2 FFT architecture which computes one sample per clock cycle only needs one adder and half a rotator per stage. This leads to $\log_2 N$ butterflies and $(\log_4 N–1)$ rotators to implement complete FFT. The butterfly structure used here has only real adder and real subtracter instead of complex ones, the rotators is made up of two multipliers and one adder instead of four real multipliers and two adders. Fig 2. shows the proposed architecture for serial computation of 16 point radix-2 SC-RFFT. The Processing Element (PE) used to calculate butterflies and rotations.

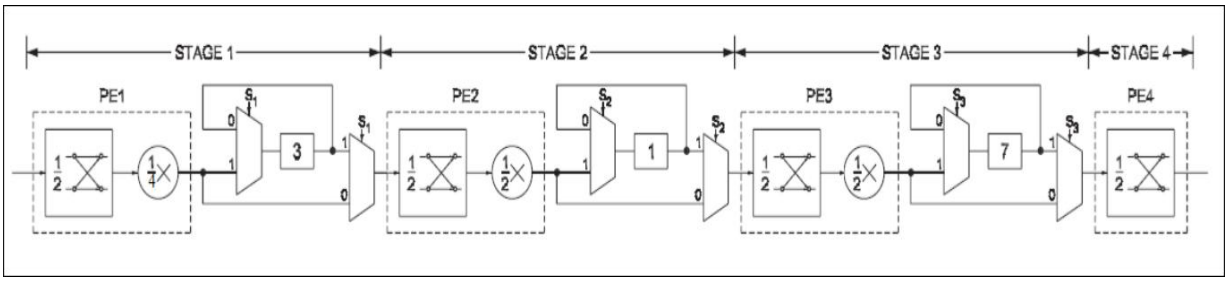

Fig2. Proposed Architecture of 16 point radix 2 SC-RFFT

1) PE1: Processing element for 1st stage is shown in Fig.3

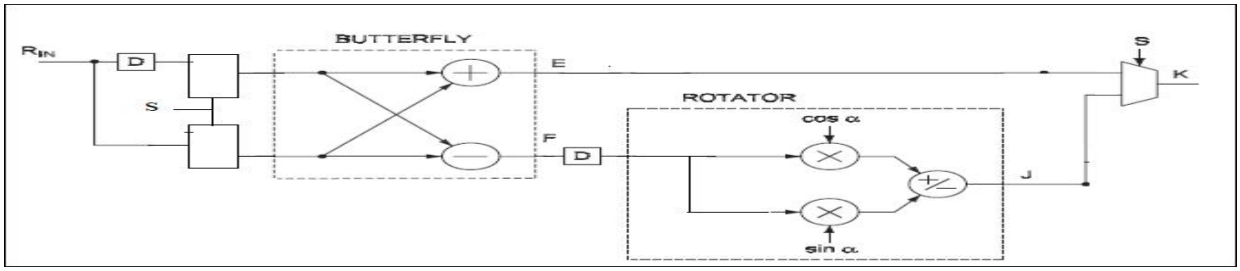

Fig3. Processing Element used at Stage 1

For real valued signal Outputs are First stage don't have real plus imaginary terms, hence one real adder and real subtractor required. Control element is used to select input using select line. Rotator requires only 1 rotation per 4 clock cycles hence quarter rotator used. $Y_0 = I_0 + I_8$, $Y_8 = (I_0 - I_8)e^{-j\alpha}$. Inputs are in consecutive clock cycles, Y_0 and Y_8 are obtained in consecutive clock cycles.

2) PE2, PE3: Processing element for 2nd and 3rd stage is shown in Fig. 4

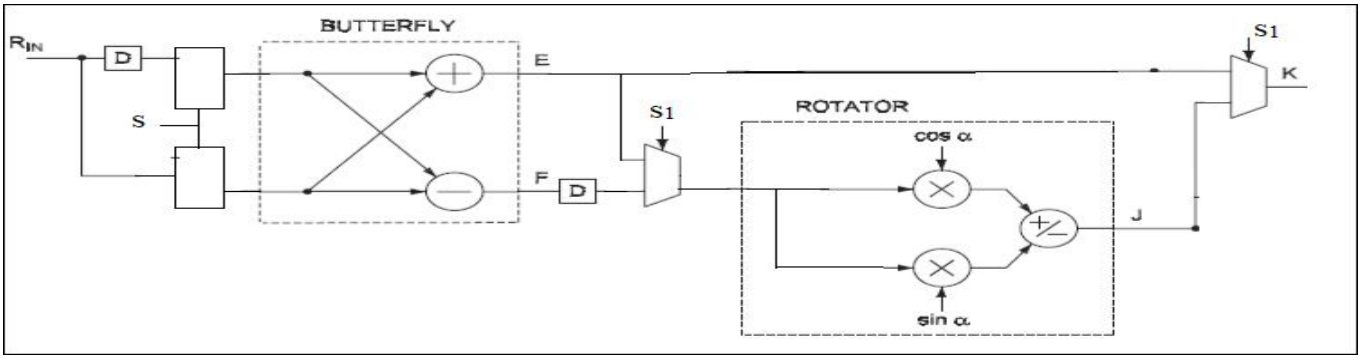

Fig4. Processing Element used at stage 2 and stage 3

In 2nd and 3rd stage mux is used to control input to rotator. In the last stage processing element does not require any rotator.

Table 1: Timing diagram of PE stage 1

T	In	S	E	F	K
0	I_0	0			
1	I_8	1	$Y_0=I_0+I_8$		Y_0
2		0		$Y_0=I_0-I_8$	Y_8

Table 2: Timing diagram of PE stage 2

T	In	S	E	F	K
4	Y_0	0			
5	Y_8	1	$Z_0=Y_0+Y_4$		Z_0
6		0		$Z_4=Y_0-Y_\$$	Z_4

3) PE4: Processing element for 4th stage is shown in Fig.5

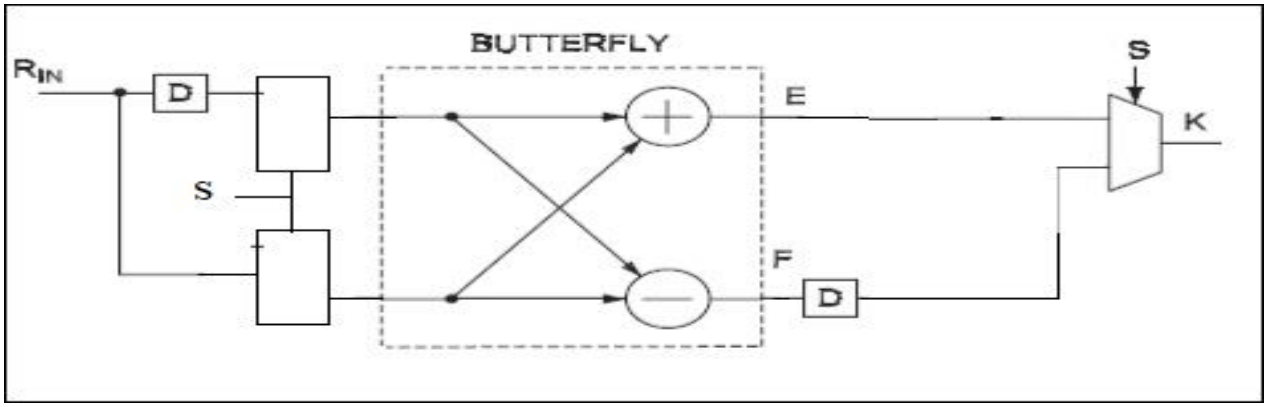

Fig5. Processing Element used at stage 4

A. Bit Exchange Element

Outputs of processing should be re-arranged before given as inputs to next processing element. Samples to be operated together must come in consecutive clock cycles: hence Bit-exchange circuit is required. Inputs required to be delayed by different amount for different stages, This circuit can be used for DIF as well as DIT.

III. COMPARISON AND ANALYSIS

Table 3 and Table 4 give comparison for pipelined FFT architectures for serial data. Table 3 does not focuses on any specific order for I/O, whereas next table gives comparison for natural inputs and outputs. In Table 3, first table denotes the type of architecture, and numbers of rotators, adders used in architecture are showed in second, third column, and latency and throughput is compared in last two columns. Since all architecture process serial data, throughput can be calculated by one sample/clock cycle.

Table 3 compares different parameters for natural inputs and outputs. Proposed architecture reduces the number of delay registers by 50%.

Table 3: Comparison for pipelined architecture for N-point FFT for serial data

Pipelined Architecture	Complex Rotators	Complex Adders	Latency (cycles)	Throughput
SDF Radix-2, [2]	$2(\log_4 N-1)$	$4(\log_4 N)$	N	1
SDF Radix-2, [9]	$\log_4 N-1$	$2(\log_4 N)$	4N/3	1
SDF Radix-4, [3]	$\log_4 N-1$	$8(\log_4 N)$	N	1
SDF Radix-4, [2]	$\log_4 N-1$	$4(\log_4 N)$	N	1
SDF Split-radix, [13]	$\log_4 N-1$	$4(\log_4 N)$	N	1
SDF Radix-4, [14]	$\log_4 N-1$	$3(\log_4 N)$	2N	1
SDC-SDF Radix-2, [8]	$\log_4 N-1$	$2(\log_4 N)$	3N/2	1
Proposed SC-RFFT	$\log_4 N-1$	$2(\log_4 N)$	N	1

Table 4: Comparison for pipelined architecture for N-point FFT for natural inputs and outputs

Pipelined Architecture	Complex Rotators	Complex Adders	Latency (cycles)	Throughput
SDC Radix-2, [6]	$2(\log_4 N-1)$	$2(\log_4 N)$	2N	1
SDC Radix-2, [5]	$2(\log_4 N-1)$	$2(\log_4 N)$	2N	1
Proposed SC-RFFT Radix-2, even N	$\log_4 N-1$	$2(\log_4 N)$	N	1
Proposed SC-RFFT Radix-2, odd N	$\log_4 N-1$	$2(\log_4 N)$	N	1

IV. RESULTS

SC-RFFT for n=1024 points and word length as 16 bits is implemented on ASIC technology using UMH 90-nm technology. Various parameters for former architectures are compared in Table 5. In proposed architecture clock frequency and area are improved with compared to other architectures.

For s^{th} stage, number of delay registers required given as $(2^{n-s-1} – 2^0)$. For 1^{st} stage required delay registers are $(2^{4-1-1} – 2^0) = 3$. For 2^{nd} stage, required delay registers are $(2^{4-2-1} – 2^0) = 1$. For last stage, required delay registers are $(2^{4-1} – 2^0) = 7$. Thus for 16-bit RFFT 11 delay registers are required. And also, number of delay registers for N-bit is given as: (Number of bits- Number of stages-1).

Table 5: Comparison of serial FFT after implementing on ASIC

Parameter	Proposed Architecture	[15]	[16]	[17]
FFT Size	1024	64	2048	256
Radix	2	2^3	2^4	2^4
Architecture	SC-RFFT	SDC	SDF	SDF
Word length	16	16	10	-
Technology (nm)	90	-	180	180
Voltage (V)	0.9	-	2.7	1.8
Clk (MHz)	200	166	76	51.5
Area (mm^2)	0.15	0.47	7.58	-
Gate Count	134066	-	-	173875
SQNR (dB)	55	-	45.3	-
Power (mW)	8.0	29.7	526	-
Norm. Power (mW)	8.0	-	9.18	-

V. CONCLUSIONS

This paper presents novel architecture for the 16-point radix-2 serial commutator for real valued fast fourier transform (SC-RFFT) architecture. This bit exchange circuit for data management at intermediate stages. Compared to previous designs [1], SC-RFFT reduces execution time for computation of real valued input signal FFT. Finally proposed architecture is implemented on ASIC technology for 90nm technology and experimental results are obtained which clearly shows that proposed architecture has small area and consumes low power with compared to previous architectures.

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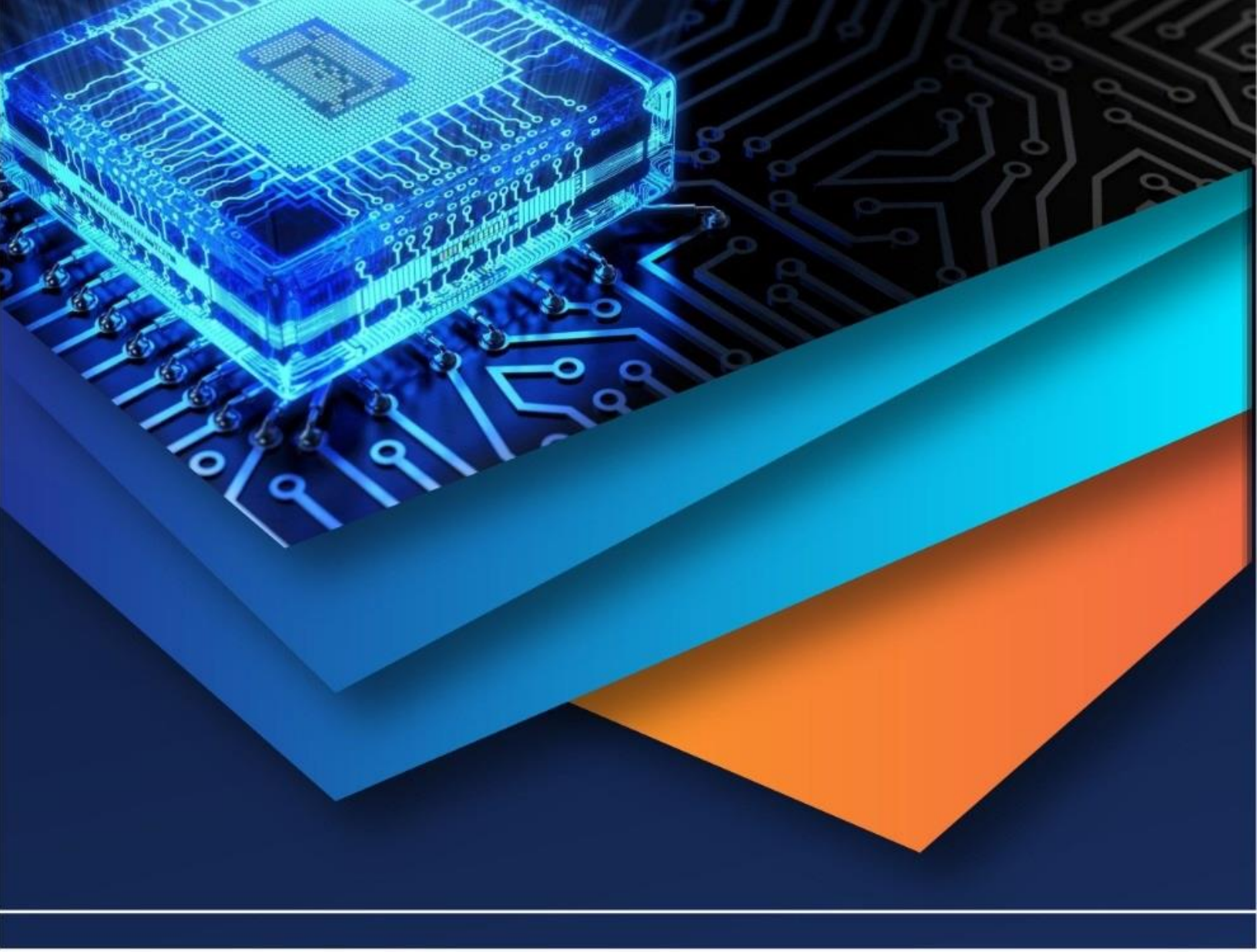

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