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A Multi-Level Full Bridge DC-DC Converter with ZVZCS PWM Control Scheme

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Abstract: ***In all the PWM DC to DC and DC to AC converter topologies, the controllable switches are operated in switch mode where they are required to turn ON and OFF the entire load current during each switching. Here the switches are subjected to high stress and high switching losses that increases linearly with the switching frequency of the PWM. Another major significant drawback of switch mode operation is the EMI produced due to large di/dt and dv/dt caused by a switch mode operation. Therefore, to realize high switching frequencies in converters, the aforementioned shortcomings are minimized if each switch in a converter changes its status (from ON to OFF or vice versa) when the voltage across it and/or the current through it is zero at the switching instant. This paper propose a simplified switching scheme for three level full bridge DC to DC converters that enables zero voltage and zero current switching of all the main power devices. This describes the main operational modes of the converter as well as simulated results through MATLAB/simulink.***
Keywords: DC-DC Converter, Zero voltage Switching(ZVS), Zero Current Switching(ZCS), Switching losses, Full bridge, Inverter, duty cycle, switching period, Pulse width Modulation (PWM)

I. INTRODUCTION

The DC-DC converters are widely used for battery power supply in different electronic devices like mobile phones, MP3 players and laptops. There is a scope for developing DC-DC converters to generate multiple dc output voltage from single dc power supply. These multiple output voltages are feed to the different dc load applications. This scheme of developing multiple dc voltage levels from a single dc supply source can reduce the overall device area. The dc voltage provided by rectifier or battery contains more ripples and it is not a constant value and it ia not suitable for many electronic devices. To overcome this problem, the dc-dc voltage regulators are used to control the ripples even when change in the input voltage or load current. The switching mode type dc-dc converters power supply is widely used because it uses a switch in the form of transistor type and less loss components such as transformers, inductors and capacitors for controlling the output voltage. The switched mode power supply contains two different parts: control part and power part. The majority of the work is carried out by the control part for getting better control of output voltage. Generally the MOSFET is used as a control switch in Switched mode power supply for stabilizing the required output voltage. The MOSFET switches are not to be conducted continuously and they operate only under specific frequency interval only, hence these switches are useful for a long future and also provide less power loss the converter circuit. The basic structure of Switched mode power supply is used for stepping up or stepping down of input DC voltage. The SMPS circuit is basically consists of a filter at the output side for removing the ripples due to switching.

The trends of the power electronics system are toward smaller size, lighter weight and higher efficiency. So, the switching frequency is increased for these reasons. Because increasing of the switching frequency can reduce the size of the magnetic components that are major constituents at the point of view with weight and size .On the other hand, when the switching frequency is increased, switching losses are also increases. When the switching devices like MOSFET or IGBT perform hard switching, the higher switching frequency increases, the more switching losses are generated. Also according to that, the whole system efficiency go down. To overcome these problems, the zero-current switching (ZCS) or zero voltage switching (ZVS) resonant converters have been proposed. The present paper presents a dc–dc converter that achieves soft switching for all the main switches, reduces the voltage stresses across each main switch, and controls the voltage on the secondary side of Full Bridge step- down converter. The simulation is done with the help of MATLAB/Simulink..

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II. ZVZCS DC-DC CONVERTER

Figures 2.1 & 2.2 shows the circuit topology and the operational waveforms of the proposed converter. The simple control strategy is based on phase-shifted pulse-width modulation with diagonal switches receiving the same control signals. Thus, S_1 and S_8, S_2 and S_7, S_3 and S_6, and S_4 and S_5 are each controlled in pairs.

The resistance R-load is the load equivalent resistance and might represent, for example, the inverter interfacing a distribution system. The intermediate voltage stages typically available in a 3L converter (i.e., ±*V*dc/2) allow a better approximation of a sinusoid thus resulting in a reduction in harmonic levels for the inverter case, but this feature is not applicable to the dc–dc converter here since the output voltage *V*out fixed at a constant dc level, is greater than the intermediate levels typical of dc–ac 3L converters. If the intermediate voltages were used, the voltage at the input of the diode-bridge rectifier would be less than *V*out and the rectifier would not conduct, so no power would be delivered to the load.

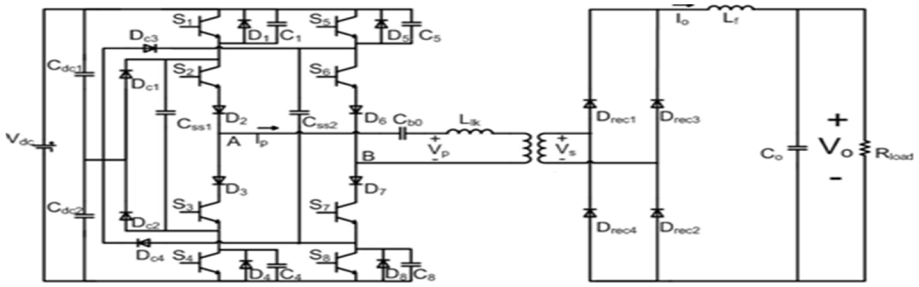

Fig.2.1 ZVZCS control DC-DC converter

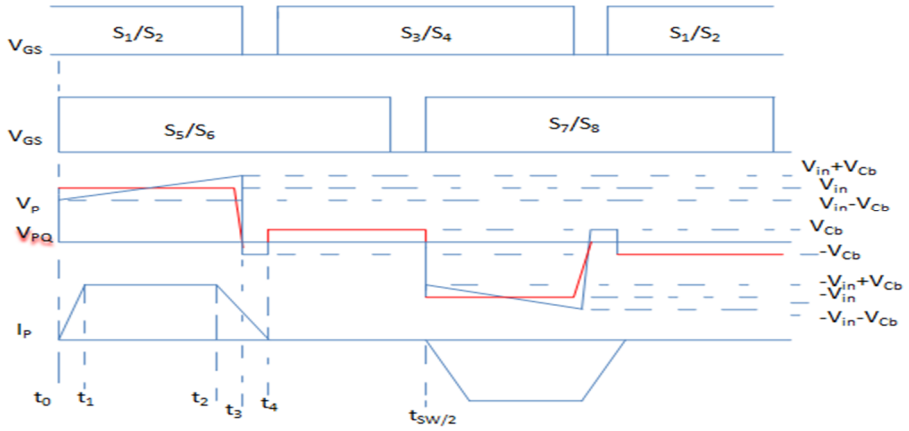

Fig 2.2 operational wave forms of the proposed converter

State	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V
1	+	+	-	-	-	-	+	+	V_{DC}/n
2	-	+	-	-	-	-	+	-	0
3	-	+	-	+	+	-	+	-	0
4	-	-	-	+	+	-	-	-	0
5	-	-	+	+	+	+	-	-	$-V_{DC}/n$
6	-	-	+	-	-	+	-	-	0
7	+	-	+	-	-	+	-	+	0
8	+	-	-	-	-	-	-	+	0

Table.2.1.Switching table

Table 2.1 gives the proposed switching states and identifies the voltage levels *Vs* at the output of the transformer for each switching

state. A "+" symbol indicates that the switch is ON during the switching state, while a "−" symbol indicates that the switch is OFF. The switching frequency is fixed and each switch is ON for exactly half a switching cycle, but the timing of the turn-OFF and turn-ON of each controlled switch is controlled so that the dc-bus voltage is applied to the transformer for the desired time as with phase-shifted PWM. Using Table I and recognizing that the rectifier causes the voltage at the output filter to be positive regardless of the polarity of the transformer voltage, it can be realized that the system has the same general operating modes as a buck converter. The switching scheme, though it does not allow the intermediate voltage levels, does achieve soft switching for all the main devices. Furthermore, the loss of intermediate switching states is consistent with other 3L soft-switched designs. The rectifier diodes *D*rec1–*D*rec4 change the transformer voltage so that a positive voltage is applied to the output filter regardless of the polarity of the transformer voltage; thus, the converter's operation can be defined in terms of half cycles with the voltage and current seen by the output filter *Lf –Co* being the same for each half cycle. If the converter is in state 1 for duration $D \times T$sw /2, where *D* represents the duty cycle and is a fraction between 0 and 1, then the average voltage at the rectifier will be

$$V_{out} = \frac{D*V_{dc}}{n} \qquad (2.1)$$

Where *n* is the turn's ratio of the transformer. This provides the desired dc voltage conversion and shows that the system operates as a transformerized buck converter. This Chapter will show how the switching scheme achieves soft switching. Examining Table I and Fig.3.1 reveals that diagonal switches receive the same control signals. The switching scheme can be simplified by controlling the devices in pairs, so that each pair— *S*1 and *S*8, *S*2 and *S*7, *S*3 and *S*6, and *S*4 and *S*5—receives the same control signal. It can be further noted that the switching order and duration is identical to phase-shifted PWM for a two level FB, so existing phase-shifted PWM controllers can be used to control the converter. This is an advantage compared to other 3L FB soft-switching topologies which require complex switching control schemes, such as double-phase-shifted control.

III. ZVZCS DC-DC CONVERTER OPERATION MODES

The figures of 3.3 to 3.7 show the first five operational modes of the ZVZCS DC-DC Converter. The subsequent five modes operate similarly to the first five modes, along with the sixth operational mode to show its similarly to the first. The following analysis is assumes that the switching period, and the blocking capacitor is large enough to act as a constant voltage source while the current is being reset.

A. Operational Mode1

$t_0 \le t \le t_1$

Switches S_1 and S_8 have been ON for a (relatively) long time and Cb_0 is charged to $-v_{cb0.}$ At t = 0, switches S_2 and S_7 being conducting and $(V_{dc} - v_{cb0})$ is applied to the primary of the transformer. As a result the primary current rapidly rises from 0 to the reflected output current.

$$I_{po} = \frac{I_o}{n} \qquad (3.1)$$

Where I_{P0} is the peak value of the primary side current going into the transformer, I_0 is the Current through L_f, and n is the turns ratio of the transformer. The voltage applied to the transformer leakage inductor L_{lk} during this period is $V_{dc} - (- V_{cb0}) = V_{dc} + V_{cb0,}$ and the duration of this period is

$$t_1 - 0 = t_1 = \frac{L_{lk}*I_{p0}}{V_{dc}+V_{cbo}} \qquad (3.2)$$

Since this period is so short, V_{cb0} is assumed to be constant throughout the period. The load current is not completely supplied by V_{dc} during this period, so the excess current freewheels through the secondary rectifier diodes $D_{rec1} - D_{rec4}$

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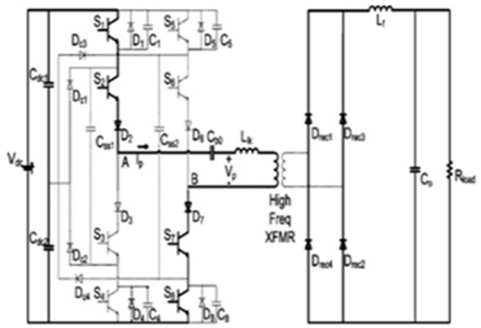

Fig 3.3 Operation mode1($t_0 \leq t \leq t_1$)of the proposed converter

B. Operational Mode 2

$t_1 \leq t < t_2$

The freewheeling mode ends when the primary current reaches I_{p0} at t_1 and diodes D_{rec3} and D_{rec4} stop conducting. The output filter is connected in series with the leakage inductance of the transformer through D_{rec1} and D_{rec2}, and acts to keep the primary current constant at I_{p0}. The duration of this mode is related to the voltage conversion ratio by the duty cycle parameter D, which is given by

$$\frac{V_0}{V_{dc}} = \frac{D}{n} = \frac{\left((t_{ON})\middle|(T_{sw}/2)\right)}{n} = \frac{(t_2 - t_1)/(T_{sw}/2)}{n} \qquad (3.3)$$

Since interval t_1 is so short, t_{ON} is set equal to t_2 and

$$D = \frac{t_2}{T_{sw}/2} \qquad (3.4)$$

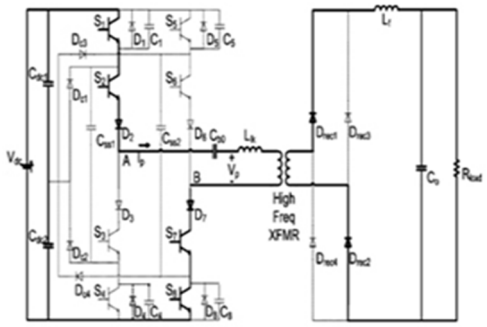

Fig 3.4 Operation mode2 ($t_1 \leq t < t_2$ **)** of the proposed converter

The blocking capacitor is charged from $-V_{cb0p}$ to $+ V_{cb0p}$ by I_{p0} during this mode.

C. Operation Mode 3

$t_2 \leq t < t_3$

Switches S_1 and S_2 are turned OFF at t_2. Capacitors C_1 and C_8 are charged and C_4 and C_5 are discharged by i_p, which is still held constant at I_{po} by the large output filter inductance. When C_4 and C_5 are completely discharged at t_3, the primary current begins to circulate through devices S_2 and S_7 and diodes D_{c1} and D_{c4}. Switches $S_4$and S_5 can be gated ON under complete at any time after t_3.

Since this mode is so short, V_{cb0} is assumed to remain constant at V_{cb0p} for the duration of this mode. Each of the parallel capacitors conducts $I_{p0}/2$ during this mode and has change of voltage of $V_{dc}/2$. Using the same value C_r for capacitors C_1,C_4,C_5 and C_8 the duration of this mode is

$$t_3 - t_2 = c_r * \frac{V_{dc}}{I_{p0}} \qquad (3.5)$$

D. Operation Mode 4

$t_3 \leq t < t_4$

As the primary current circulates through S2, S7, Dc1 and Dc4, the blocking capacitor voltage Vcb0p is applied to the transformer and the primary current begins to decrease. As soon as the primary current falls below I_{p0}, the output current begins to freewheel through the output rectifier diodes, disconnecting the primary side of the circuit from the load and short circuiting the transformer magnetizing inductance.

$$T_{reset} = t_4 - t_3 = L_{lk} * \frac{I_{p0}}{V_{cb0p}} \qquad (3.6)$$

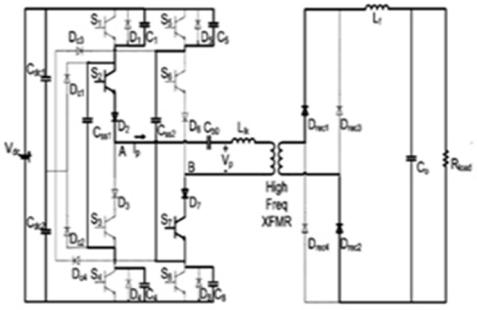

Fig 3.5 Operation mode3($t_2 \leq t < t_3$)of the proposed converter

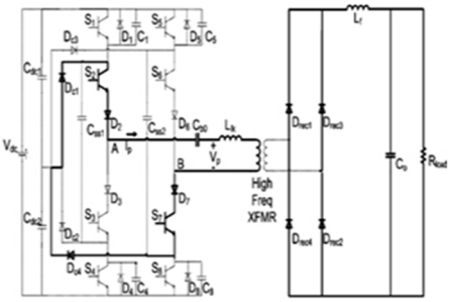

Fig 3.6 Operation mode4($t_3 \leq t < t_4$) of the proposed converter

E. Operational Mode 5

$t_4 \leq t < T_{sw}/2$:

Upon reaching zero, the current is prevented from flowing in the negative direction by the diodes D_2 and D_7. The output current continues to freewheel through the output rectifier diodes. The voltage The voltage *Vcb*0*p* appears across the output terminals *AB*, so *S*1 and *S*8 have to block (*V*dc + *Vcb*0*p*)/2. At *T*sw /2, *S*2 and *S*7 turn OFF under ZCS, and shortly afterward, *S*3 and *S*6 turn ON under ZCS. Since *S*4 and *S*5 are already ON, *S*3 and *S*6 conduct, and (−*V*dc + *Vcb*0*p*) is applied to the primary of the transformer, beginning operational mode 6. Modes 6–10 are similar to modes1–5 except for the reversal of current and voltage signs.

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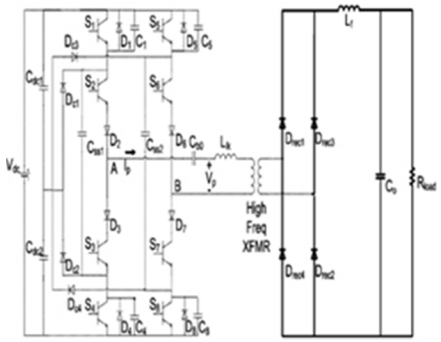

Fig 3.7 Operation mode5($t_4 \leq t < T_{sw}/2$)of the proposed converter

IV. DESIGN EQUATIONS

The design of the converter involves determining values for *C*dc1, *C*dc2, *C*ss1, *C*ss2, *C*1, *C*4, *C*5, *C*8, *Cb*0, *Llk* , and the output filter. The output filter should be large enough to maintain the load current for the entire switching period *T*sw, while the transformer leakage inductance *Llk* should be minimized in order to minimize the reset time. Beyond these restrictions, transformer and filter design principles also apply. Capacitors *C*dc1 and *C*dc2 are essential for the proper voltage division across the switching devices. Consequently, they should be selected with identical values using tight tolerance parts. In practice, the dc-bus capacitors will be required to maintain the voltage through changes in the input voltage *V*dc and through voltage spikes caused by parasitic inductances, so a large value may be required. Smaller capacitors with good high-frequency response may be placed in parallel with the bulk dc-bus capacitors in order to handle high-frequency ripple due to parasitic components. Capacitors *C*ss1 and *C*ss2 are also identical. Fig. 2 shows that they conduct during mode 3 and its mirror, mode 8. These capacitors must maintain a near-constant voltage during the entire cycle; thus, they should be selected so that they do not experience more than a 5%voltage change during mode 3. Each capacitor conducts *Ip*0/2 during mode 3, and its nominal voltage is *V*dc/2. Therefore, the capacitor value required for a 5%ripple is

$$C_{SS} = \frac{I_{P0} * (t_3 - t_2)}{0.05 * V_{dc}} \qquad (3.7)$$

This can be simplified using (4.6), so that

$$C_{SS} = \frac{C_r}{0.05} = 20 * C_r \qquad (3.8)$$

The size of the parallel capacitors, *Cr* , is determined by the minimum requirement to achieve ZVS during turn-OFF, which requires that the parallel capacitors must be large enough to hold the voltage close to zero during the current fall-time of the device t_{fi}, which can be determined from the data sheet. Once this parameter has been determined, *Cr* can be calculated as follows

$$C_r = \frac{t_{fi} * I_{p0}}{V_{dc}} \qquad (3.9)$$

A large value of Vcb0p is desirable in order to quickly reset the primary current during mode 4, but the "OFF" devices; see (Vdc + Vcb0p)/2 at the end of mode 2. Thus, the value of Vcb0p should be limited to one-fifth the dc-bus voltage in order to limit the voltage stress on the devices. Capacitor Cb0 is charged from −Vcb0p to +Vcb0p during mode 2 by I_p at a value of I_{p0}. The blocking capacitor will reach its largest value when the converter is transferring maximum rated power and I_p is at I_{p0max}. In order to meet the voltage restriction outlined earlier for these conditions, Cb0 should be chosen as

$$C_{b0} = \frac{5 * I_{P0.max} * D_{max}}{4 * f_{sw} * V_{dc}} \qquad (3.10)$$

Where $I_{P0.max}$ is the maximum value of the steady-state primary current expected during normal operation, D_{max} is the value of the duty cycle at maximum power transfer, and f_{sw} is the switching frequency. Since V_{cb0p} is directly proportional to I_{p0} any value of I_p less than $I_{P0.max}$ will result in a value of V_{cb0p} less than $V_{dc}/5$. The voltage Vcb0p for any value of I_{p0} less than $I_{P0.max}$ or any D less than D_{max} is

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$$V_{cb0p} = \frac{I_{P0} * D}{4 * f_{sw} * C_{b0}} \quad (3.11)$$

V. SOFT-SWITCHING RANGE

ZVS is accomplished when I_{p0} discharges the parallel capacitors across the leading switches during mode 3. The length of mode 3, referred to as the dead time, limits the maximum duty cycle that can be commanded by the controller, which, in turn, limits the maximum voltage that can be achieved on the secondary and the maximum power that can be delivered to the load. Since ZVS, and hence the dead time, occurs twice per half cycle, the maximum duty cycle is

$$D_{max} = 1 - 2 * \frac{t_{dead}}{T_{sw}/2} \quad (3.12)$$

Once the dead time is fixed, there is a minimum value of the load current under which ZVS no longer occurs since the leading switches will be switched before the parallel capacitors are completely discharged. This minimum load current is given by

$$I_{p0,min} = C_r * \frac{V_{dc}}{t_{dead}} \quad (3.13)$$

The dead time must not only be selected to maximize the load current range for which ZVS occurs but must also minimize the reduction of the duty cycle. The precise value of the dead time will vary depending on the needs of the application, i.e., whether the application will require high duty cycles or whether it will require a large soft-switching range. ZCS is accomplished when the blocking capacitor voltage drives the primary current to zero before the state change that occurs at T_{sw} /2. The current begins to be reset at $t_2 = D \times T_{sw}$ /2, so the total time available to reset the current is

$$T_{reset,max} = (1 - D) * \frac{T_{sw}}{2} \quad (3.14)$$

ZCS will be achieved if the reset period from (6) is less than *T*reset,max, and using the value for V_{cb0p} from (12)

$$\frac{4 * f_{sw} * C_{b0} * L_{lk}}{D} \leq (1 - D) * \frac{T_{sw}}{2} \quad (3.15)$$

It can be seen from this equation that achieving ZCS is independent of the load current, though the voltage across *Cb*0 may become very large if the primary current exceeds the maximum load current used in (10) to calculate the value of the blocking capacitor. There is a limit on the range of duty cycles for which ZCS occurs, given by

$$\frac{1 - \sqrt{1 - 32 * f_{sw}^2 * C_{b0} * L_{lk}}}{2} \leq D \leq \frac{1 + \sqrt{1 - 32 * f_{sw}^2 * C_{b0} * L_{lk}}}{2} \quad (3.16)$$

VI. DESIGN PROCEDURE

Let I_0 = 4.2 A

$$I_{PO} = \frac{I_o}{n} = \frac{4.2}{2} = 2.1 \text{ A}$$

D=0.25=25%

Blocking capacitor $C_{bo} = \frac{5 \times I_{POmax} \times D_{max}}{4 \times f_{sw} \times V_{dc}}$

$$= \frac{5 \times 2.1 \times 0.25}{4 \times 10^4 \times 100} = 6.5625 \times 10^{-7}$$

The condition for ZCS is

$$\frac{4 * f_{sw} * C_{b0} * L_{lk}}{D} \leq (1 - D) * \frac{T_{sw}}{2}$$

$$L_{lk} \leq \frac{D(1 - D)}{8 \times f_{sw}^{\ 2} \times C_{bo}}$$

$$\leq \frac{0.25 \times 0.75}{8 \times 10^{8} \times 6.56 \times 10^{-7}}$$

$$L_{lk} \leq 3.57 \times 10^{-4} H$$

The dead time is $t_3 - t_2 = 5 \times 10^{-7} sec$

$$t_3 - t_2 = c_r * \frac{V_{dc}}{I_{p0}}$$

$$C_r = \frac{2.1 \times 10^{-6}}{100}$$

$$C_r = 2.1 \times 10^{-8} F$$

(iv). The Capacitor C_{ss} value is

$$C_{SS} = \frac{C_r}{0.05} = 20 * C_r$$

$$= 20 \times 2.1 \times 10^{-8} = 0.42 uF$$

VII. SIMULATION MODEL FOR ZVZCS DC-DC CONVERTER

In the above Matlab Simulink model, a 100V/20V DC-DC converter has been proposed. In the proposed converter there are totally eight switches. In the positive half cycle diagonal four switches (S1,S2,S7 and S8) will operate and input voltage is applied to primary of the transformer. Similarly in the negative half cycle other diagonal four switches (S3,S4,S5 and S6) will operate and negative voltage is applied to the primary of the transformer. During the switching transitions all the switches operate under soft switching technique. In the proposed model the four outer switches (S1,S4,S5 and S8) operate under ZVS condition and the remaining inner four switches (S2,S3,S6 and S7) operate under ZCS condition. The control signals for the switches have been developed as shown in the below figure.4.2. in the below figure dead band is created between the signals S1 and S4, S2 and S3 to achieve the ZVS condition.

A. Simulation Results Of The ZVZCS DC-DC Converter

The figure.4.2 shows the control signals and output waveforms of primary voltage and current of the transformer. From the figure it is evident that, when all the diagonal switches are turned on then only power will be transferred to the load. ZVS is accomplished when primary current discharges the parallel capacitors across the leading switches during dead band time.

$$I_{p0,min} = C_r * \frac{V_{dc}}{t_{dead}} \qquad (3.17)$$

Fig 4.3(a) shows the voltage across switches S4/S5. When the pulse is given the voltage across the switch is zero and when pulse is

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removed the voltage across the switch is $V_{dc}/2$. Fig 4.3(b) shows ZVS turn-OFF condition of switches S4/S5 and Fig 4.3(c) shows ZVS turn-ON condition of switches S4/S5

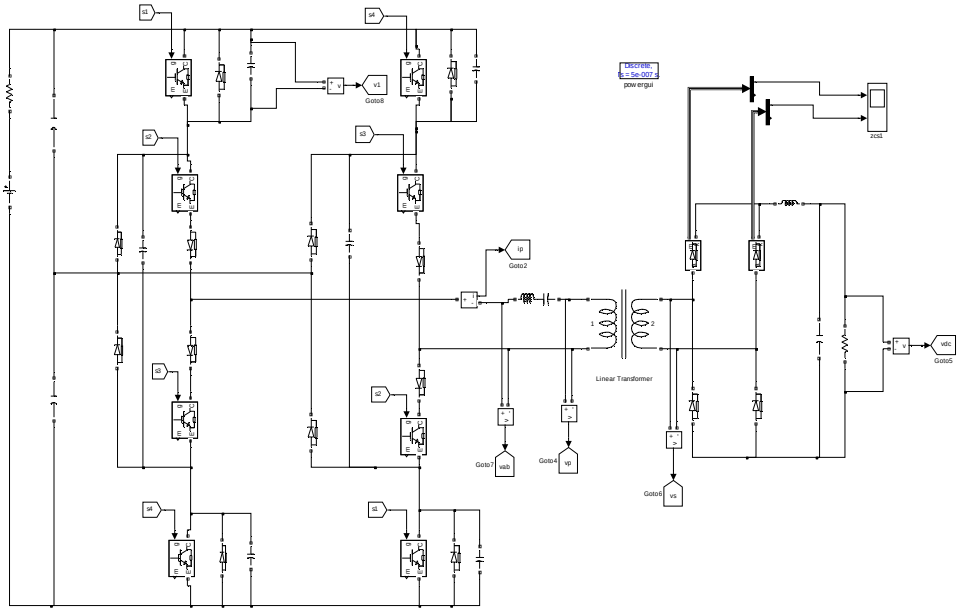

Figure.4.1.Simulink diagram of ZVZCS DC-DC converter

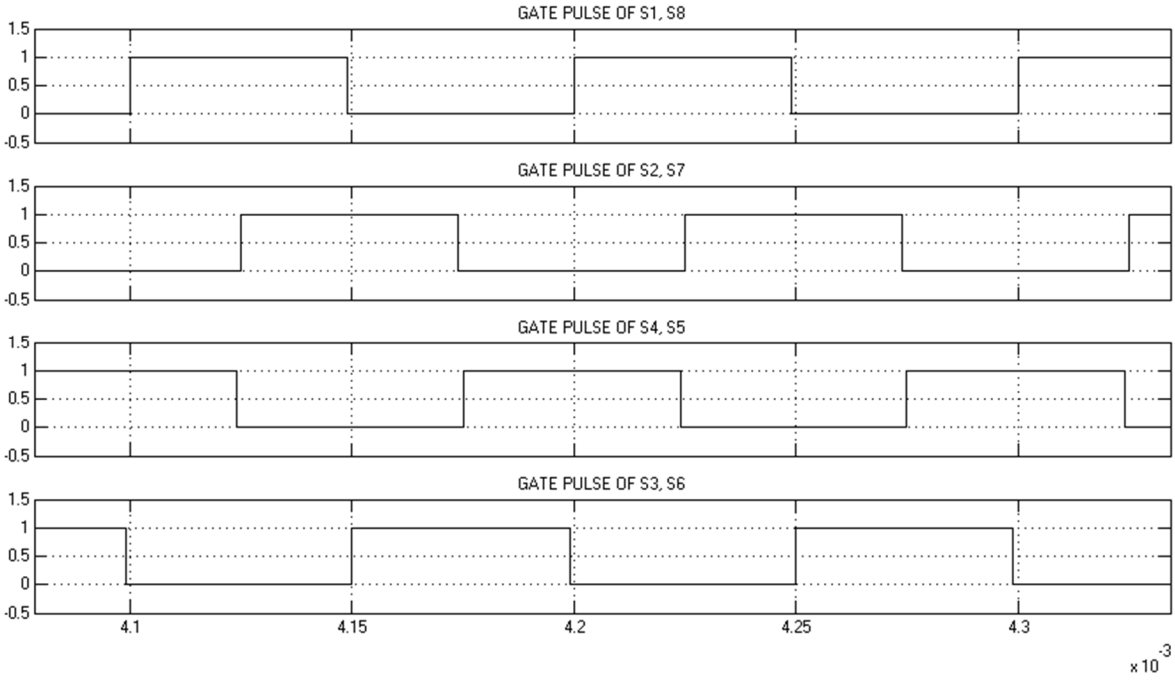

Figure.4.2.Operational waveforms of proposed converte

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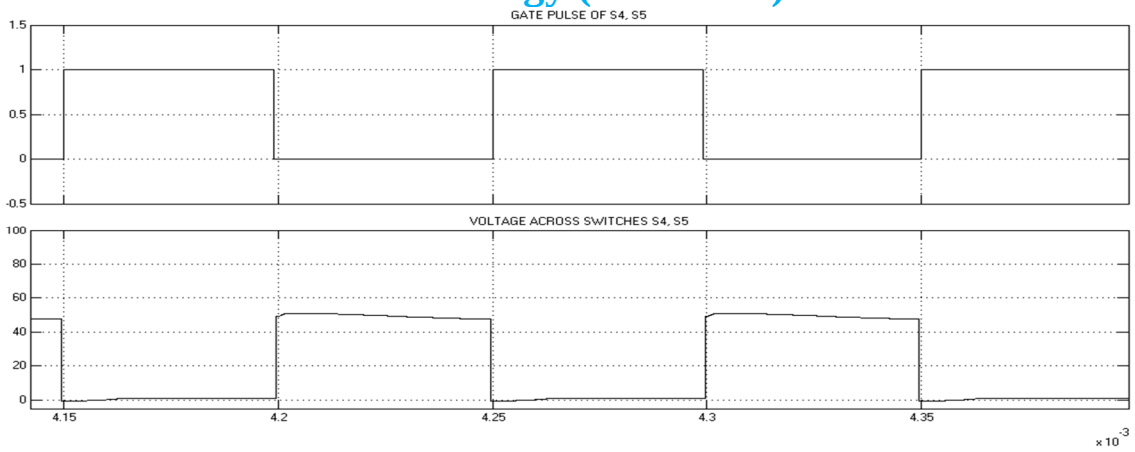
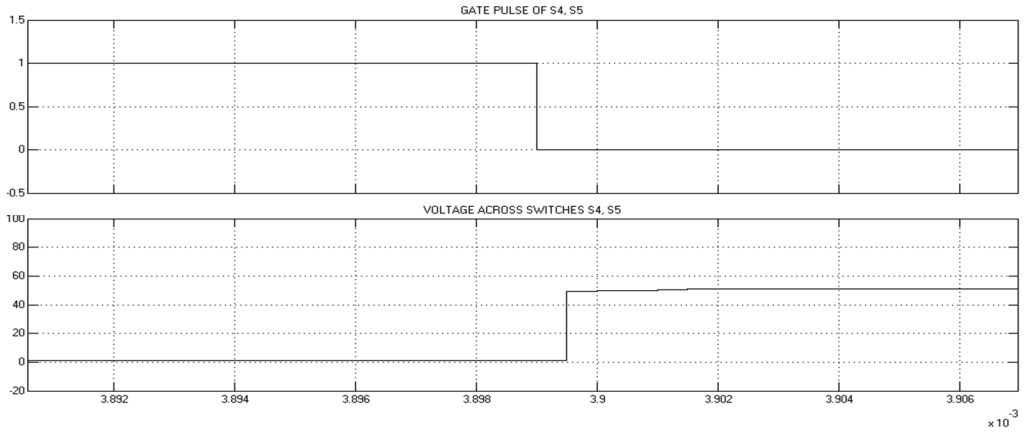
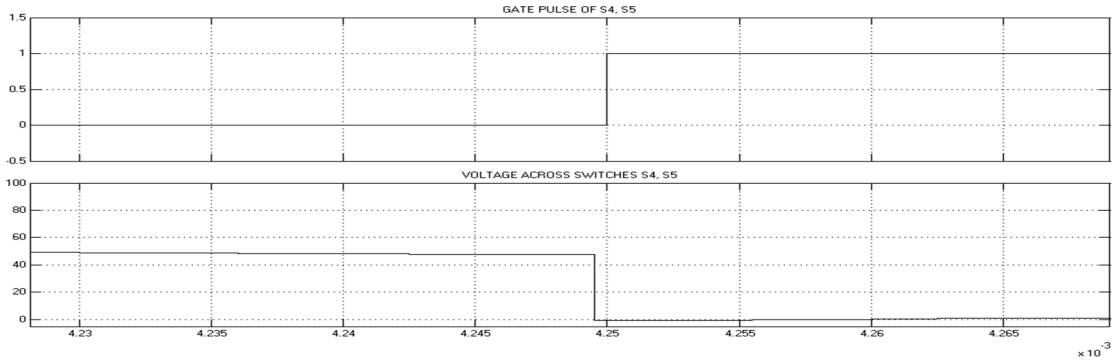


(a)



(b)



(c)

Figure.4.3. simulation (a)switch across voltage

(b) ZVS S4/S5 turn-OFF (c) ZVS S4/S5 turn-ON

Fig 4.4(a) shows the voltage across switches S1/S8. When the pulse is given the voltage across the switch is zero and when pulse is removed the voltage across the switch is $V_{dc}/2$. Fig 4.4(b) shows ZVS turn-OFF condition of switches S4/S5 and Fig 4.4(c) shows

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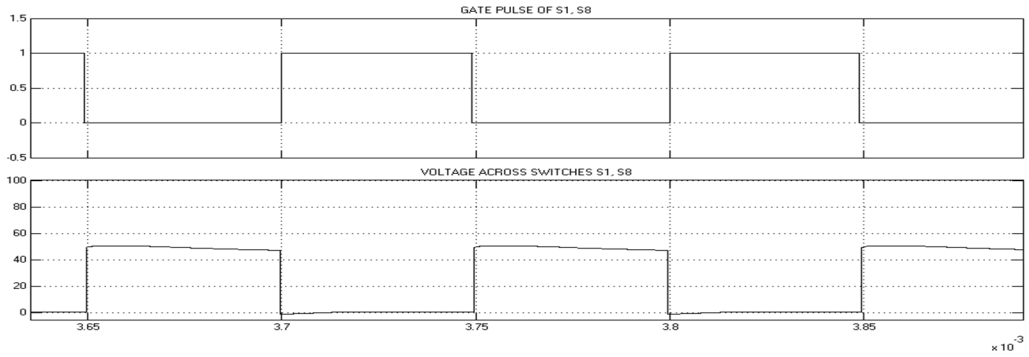
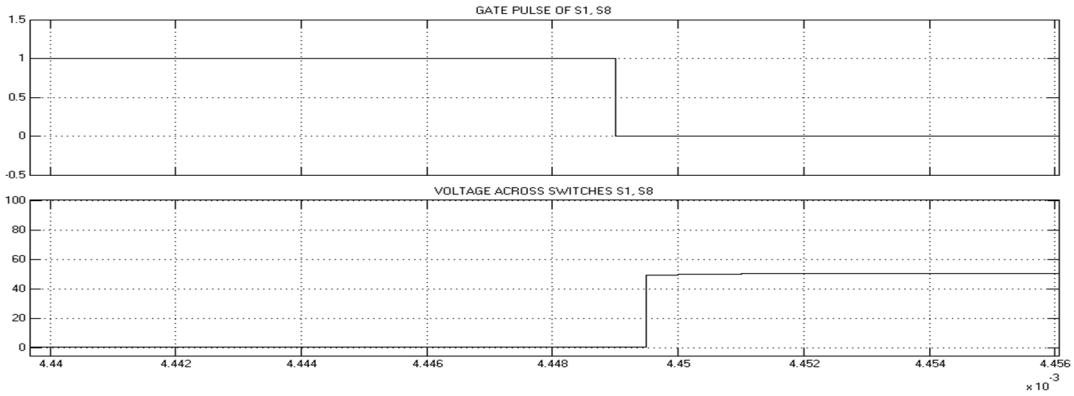
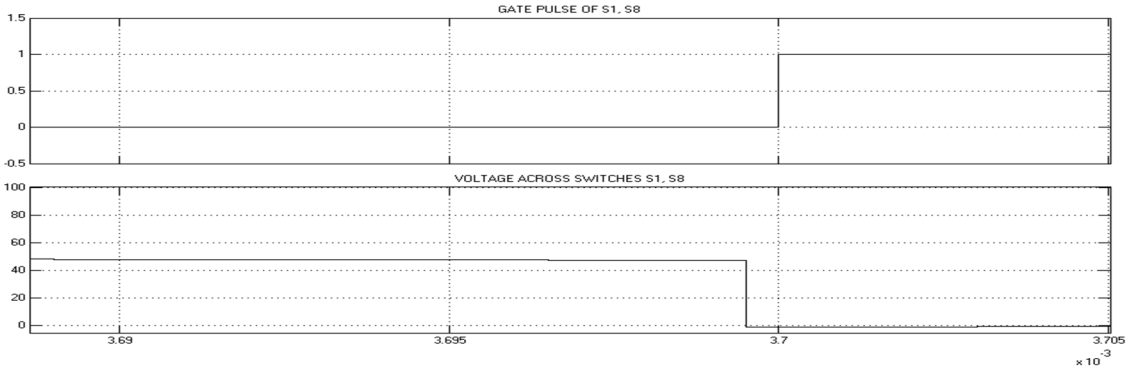
ZVS turn-ON condition of switches S1/S8.



(a)



(b)



(c)

Figure.4.4. simulation (a)switch across voltage

(b) ZVS S1/S8 turn-OFF (c) ZVS S1/S8 turn-ON

Fig 4.5(a) shows the current through switch. When the pulse is given to switch current starts flowing through it. Before removing pulse to switch current coming zero.

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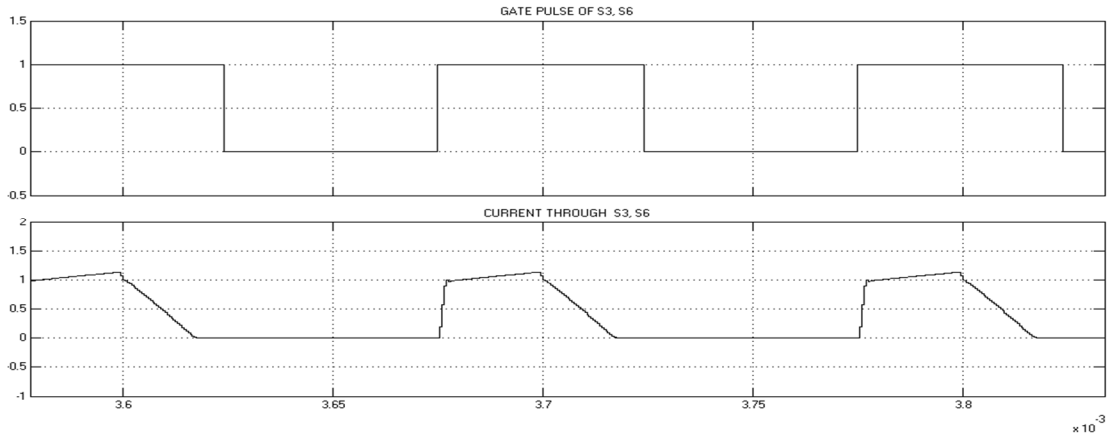
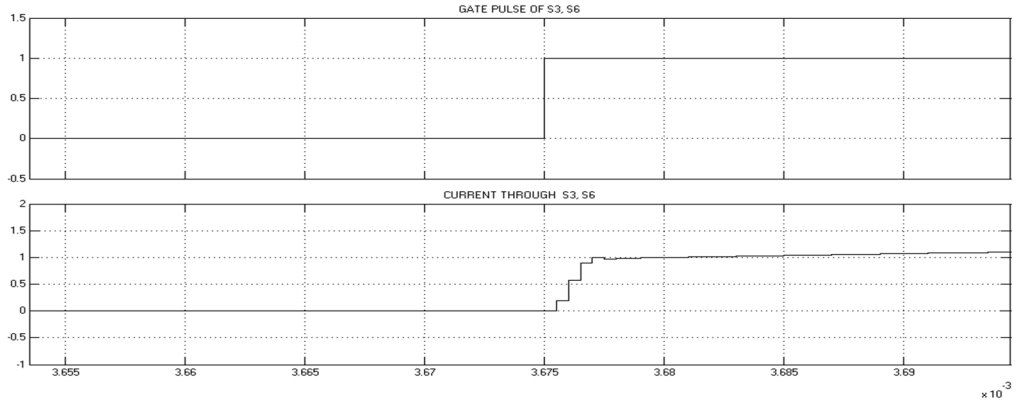
Fig 4.5(b) shows ZCS turn-ON condition of switches S3/S6 and Fig 4.5(c) shows ZCS turn-OFF condition of switches S3/S6.



(a)



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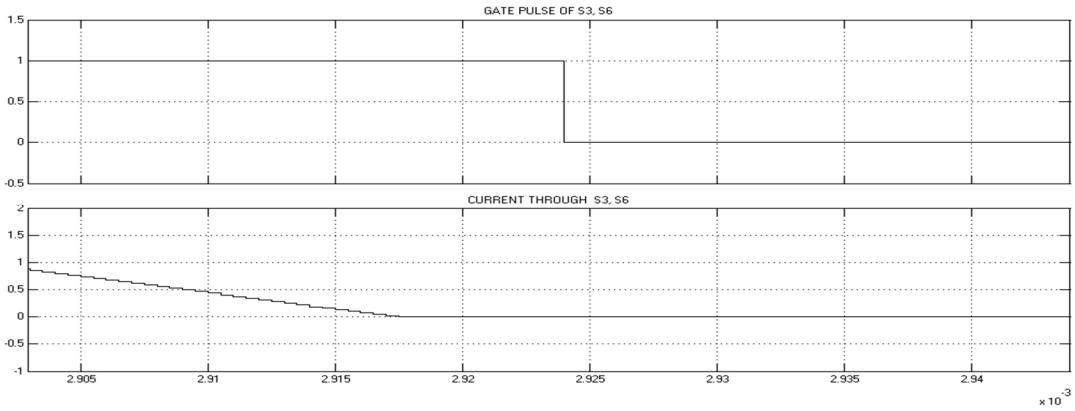

(c)

Figure.4.5.simulation (a)current through switch

(b) ZCS S3/S6 turn-ON (c) ZCS S3/S6 turn-OFF

Fig 4.6(a) shows the current through switch. When the pulse is given to switch current starts flowing through it. Before removing

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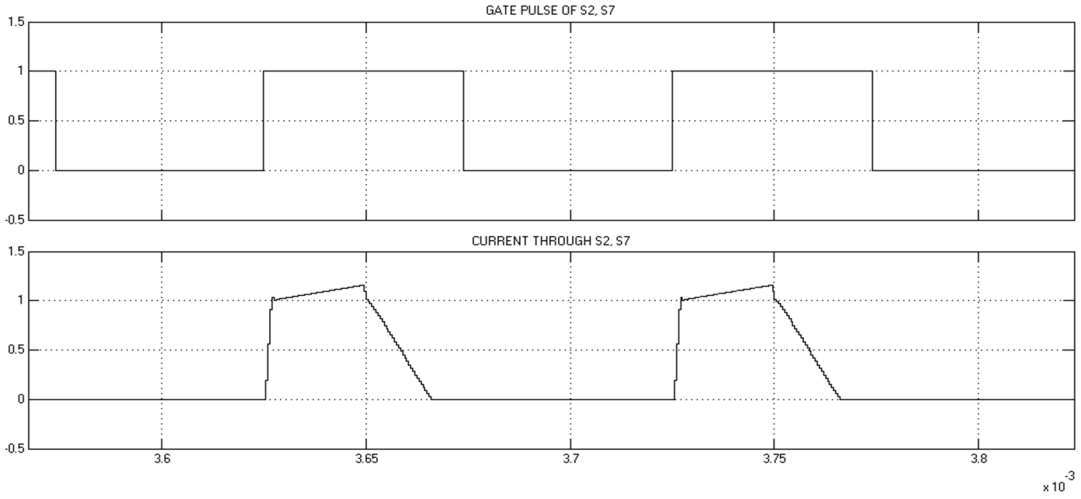
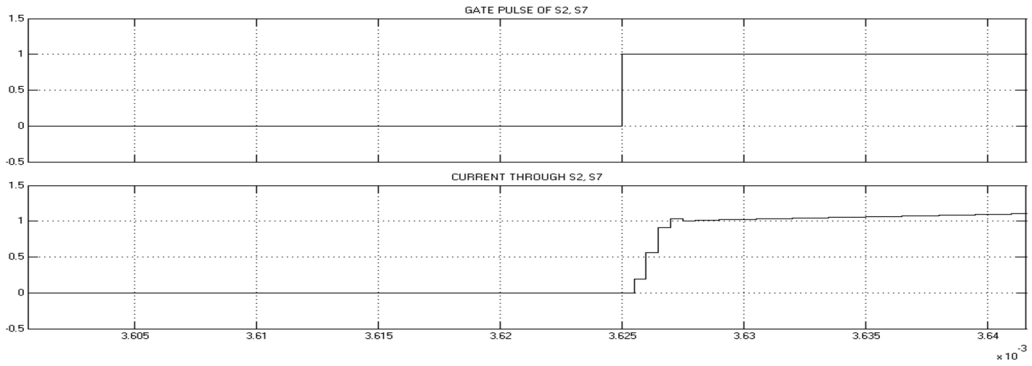
pulse to switch current coming zero.

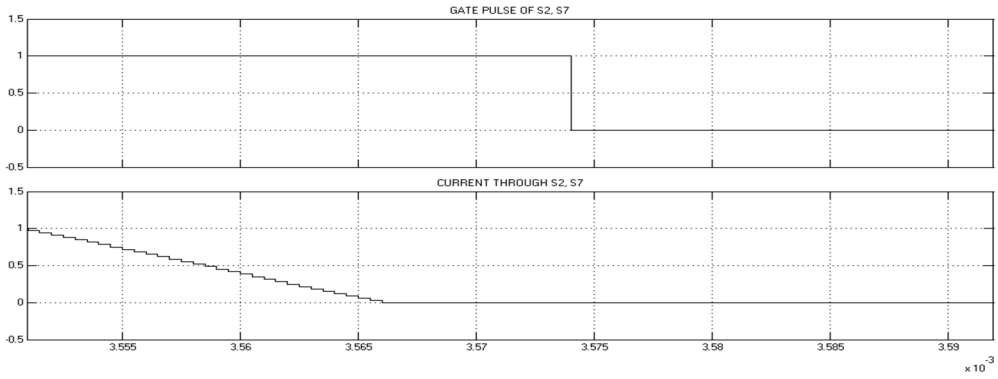
Fig 4.6(b) shows ZCS turn-ON condition of switches S2/S7 and Fig 4.6(c) shows ZCS turn-OFF condition of switches S2/S7.



(a)



(b)



(c)

Figure.4.6.simulation (a) current through switch
(b) ZCS S2/S7 turn-ON (c) ZCS S2/S7 turn-OFF

Fig 4.7 shows the simulation results of transformer primary voltage, transformer secondary voltage and dc output voltage.

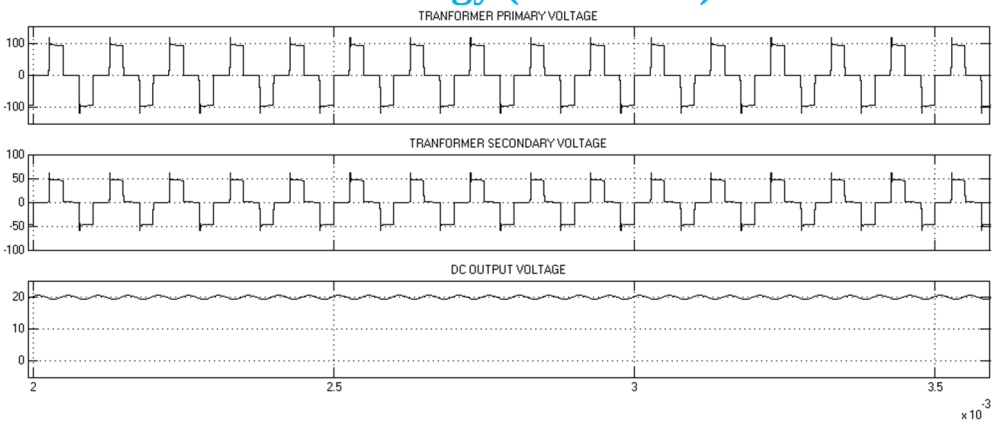


Fig 4.Results of transformer primary voltage, transformer secondary voltage and dc output voltage.

VIII. CONCLUSION

The topologies of Resonant converters are used to reduce the cost of magnetic circuit and increase the switching speeds of the circuit. The switching losses are also minimized. The Full wave topologies are used to generate less EMI as compared to half bridge topologies. When turning on, the MOSFETs are generally suitable for Zero voltage switching than zero current switching but its poor turn-off characteristics. So the IGBT is more suitable for Zero-Current switching topologies. The dc-dc converter presented here offers significant advantages over traditional designs. The power stage inverter provides efficient dc-dc conversion at very high frequencies, with few small-valued passive components and low device stresses. The multi-stage resonant gate driver developed here provides high-speed, low-loss driving of the inverter. Due to the small values and energy storage of the passive components in both the power stage and gate driver, the transient response can be very fast compared to conventional designs, and the converter is especially well suited to on-off control. This project proposes a FPGA controlled ZVZCS DC-DC converter for use in solid-state solutions. The soft switching converter was shown to have the advantages of reduced voltage stresses across the power devices, and thus allowing to operate under higher voltages. The FPGA controlled ZVZCS DC-DC converter was analyzed.

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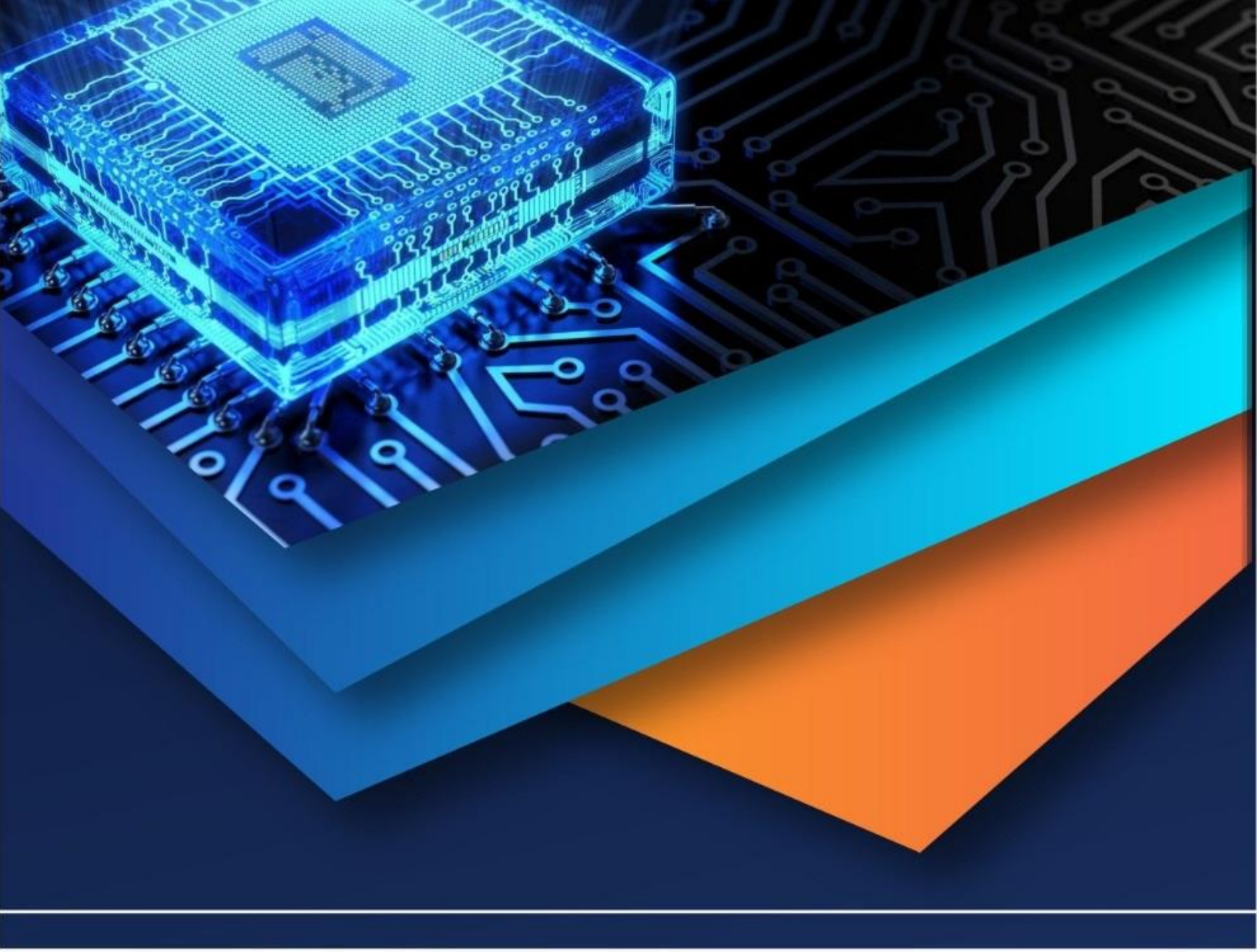

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