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Design of Low Power Consumption Inverter

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***Abstract:** As the technology scaled down, supply voltages are lowered and in-turn gate oxide thickness is reduced to decrease the threshold voltage. This increased the leakage power and continues to be one of the major issues in the design of CMOS circuits in the nanometer technology. Inverters are the fundamental circuits used in the design of VLSI circuits. In this paper, forced NMOS inverter is modified with parallel diode connected PMOS for low power consumption. Design is simulated in Cadence Virtuoso software at 45nm GPDK technology file. It is observed that the proposed design reduces power consumption by about 22%.*

***Keywords:** Inverter, Low power, Nanometer, Technology, VLSI Design*

I. INTRODUCTION

Prediction of Moore's law holds good even after 50 years of his prediction. Over the years, the number of components integrated into an Integrated Circuits (ICs) increased to several billions. Speed, area and power are main constraints for the designer in designing the Very Large Scale Integrated Circuits (VLSI) ICs. With the advances in technology, the complexity of algorithms and implementation has increased. This leads to more power consuming devices. Since most of the devices are run on batteries, power reduction techniques has taken the front seat in research in the recent times. As the technology scaled to lower technology, the percentage of leakage power dominates in the overall power dissipation. The system costs increased because of this and the reliability of the system reduced. In any processors, static power, dynamic and leakage power are the main sources of power dissipation. The static power dissipation is because of the leakage current when the circuit in standby mode. The Dynamic power is due to switching and short-circuit power. Switching power is due to the charging or discharging of the capacitance associated with the devices or nodes in the circuit. Short-circuit power arises because of the instantaneous connection between the ground and the supply voltage during the gate switches from logical 1 to 0 or vice versa [1]. To reduce power consumption, various techniques like clock gating, reduced swing clock, tristate keeper circuit, blocking gate, network restructuring and reorganization and many more methods have been bought forward. According to the literature available in [2], leakage power dominates over the total power dissipation in the nanometer device regime. The paper proposes an approach called sleepy keeper method the leakage current reduced by saving logic state. Leakage current estimation because of die and inter-die process variability is discussed in [3]. Mathematical expressions to find the leakage current probability density function (PDF) in the CMOS gates stacked devices derived in this paper. The Leakage reduction (LECTOR) technique using a control transistor is discussed in [4]. An energy efficient design in terms of multiple-threshold CMOS is proposed in [5]. In [6], the charge pumping technique is used to lower the power consumption by boosting the internal gate voltage. This shifts the operating region from the sub-threshold to a higher region and improves performance and tolerance to PVT changes. Leakage power is reduced in [7] by introducing a new inverter technique by reducing the swing using 2n mos approach. This reduces the power consumption at the cost of delay and area. In this paper, we made an attempt to reduce the leakage power by connecting a parallel diode CMOS with the forced NMOS inverter.

The paper is organized in the following manner. Section 2 describes the proposed method for the design of CMOS inverter for the low power consumption. Different inverter design details are given in Section 3. Simulation results and comparison of different designs are discussed in Section 4. The Conclusion is given in Section 5.

II. PROPOSED APPROACH

In the lower technology transistors, major leakage current is because of sub-threshold leakage current. This leakage current arises due to the transistor operating in the weak inversion mode. This current consists of direct gate current and gate induced current. This effect comes into picture due to the reduced channel length. The leakage current is given in equation 1 [8].

$$I = I_0 \exp\left(\frac{(V_{gs} - V_{th})}{nV_T}\right)\left(1 - \exp\left(\frac{-V_{ds}}{V_T}\right)\right)$$

---- (1)

where $I_0=\mu_0 C_{ox}(W/L)V_t^2 e^{1.8}$, μ_0 is the carrier mobility, C_{ox} denotes gate oxide capacitance, W is the Width and L indicates the length of the MOS device.

From Equation (1), it is observed that sub-threshold leakage current depends on Voltage across the Drain (V_{ds}) and Gate (V_{gs}) of the transistor and the threshold voltage (V_{th}).

The Threshold voltage(V_t) depends on voltage across source and body of the transistor (V_{sb}) as given in equation 2.

$$V_t = V_{t0} + \gamma\left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}\right) \quad \text{--- (2)}$$

where Vt_0 is the threshold voltage when the source is connected to the ground, Φ_s is the surface potential at threshold and Y is the body effect coefficient. In our work, voltage across Drain and Source of the transistor is attempted to reduce and Voltage across Source and Body is attempted to increase and hence the threshold voltage.

III. DIFFERENT DESIGNS OF INVERTER:

A. Design of Conventional CMOS Inverter

CMOS Inverter contains two MOSFETs(one NMOS and one PMOS) as shown in Figure 3.1.The MOSFET works like a switch. During ON state, it passes the signal with low resistance and in OFF state it does not pass the signal and offers high resistance. For logic 1 input, the NMOS is in ON state and PMOS is in OFF state. The output will be in logic 0 state. Similarly, for logic 0 input, it is vice-versa.

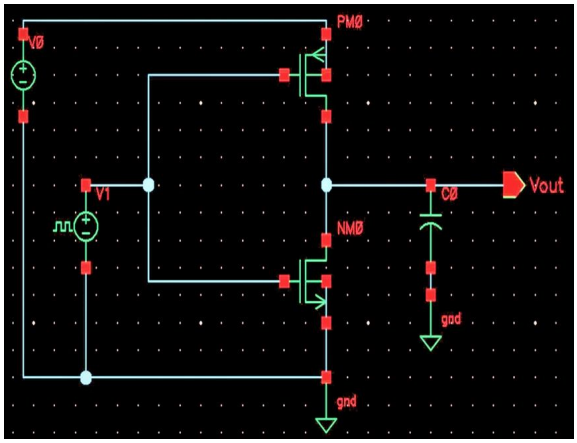

Fig 3.1 : Conventional CMOS inverter

B. Forced NMOS Inverter Design

Reducing the voltage across the Drain and Source of the transistor decreases the sub-threshold current. Therefore another NMOS in the circuit of conventional CMOS circuit s introduced as shown in Figure 3.2. Also the NMOS which is above the lowest NMOS has voltage difference between its Source and Body. This increases its threshold voltage.

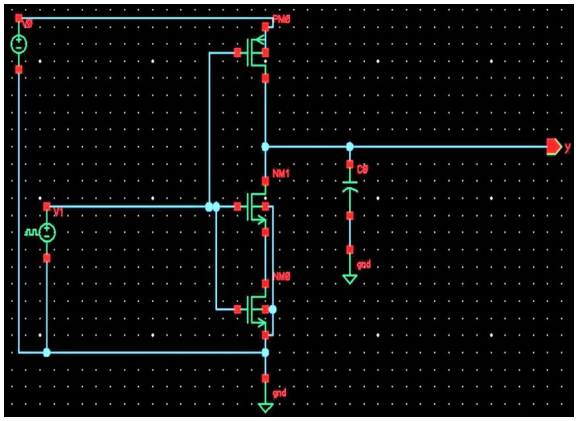

Fig 3.2 : Forced NMOS Inverter Design

C. Modified Forced NMOS Inverter with Parallel diode connected PMOS Design:

This design is similar to the Forced NMOS Inverter design but with an addition of a transistor. A diode connected PMOS is connected in parallel to the NMOS as shown in Figure 3.3. Diode connected means that the drain and the gate of the transistor are tied together. In this circuit, the voltage across the drain and source of the NMOS is altered accordingly and the threshold voltage as well. One additional thing provided by this design is that it also provides a alternate low resistance path for the discharge of the voltage.

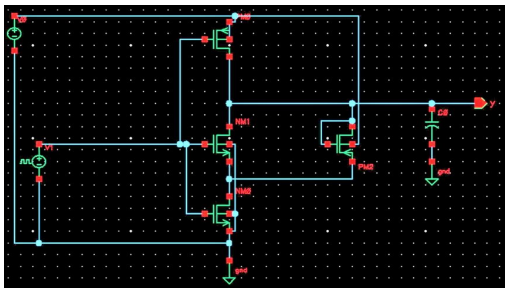

Fig 3.3 : Modified Forced NMOS Inverter with Parallel diode connected PMOS

IV. SIMULATION RESULTS

Circuits are simulated using 45nm technology GPDK library file in Cadence Virtuoso. All the transistors dimensions (W/L ratio) are kept at 120n/45n. The supply voltage used is 1.8V. Input signal of 40ns clock signal is applied as the input to test the circuit the circuit.

A. Simulation Results of Conventional CMOS Inverter

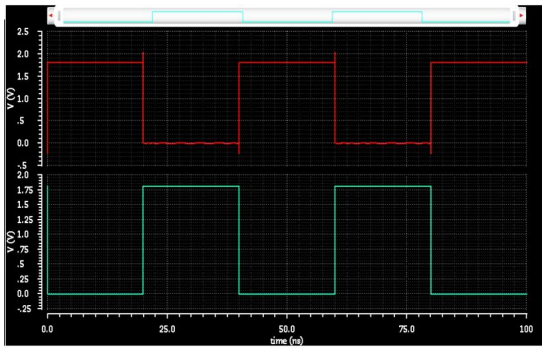

Fig 4.1.1 : Transient response of the CMOS Inverter

Circuit shown in Figure 3.1 is simulated and and resulting output waveform is shown in Fig 4.1.1. Delay performance metric is calculated using the calculator option available in Cadence Virtuoso tool and it is 2.165 psec.

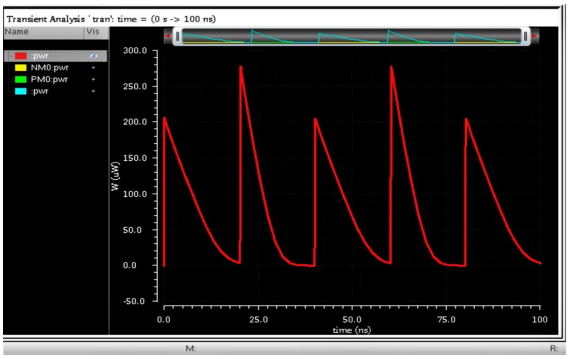

Fig 4.1.2: Instantaneous power consumption in the inverter

Fig 4.1.2 shows the instantaneous power consumption in the CMOS inverter. Using the average tool in the Cadence Virtuoso calculator, power consumption is calculated and it is 89.88 μW.

B. Simulation Results of Forced NMOS Inverter Design

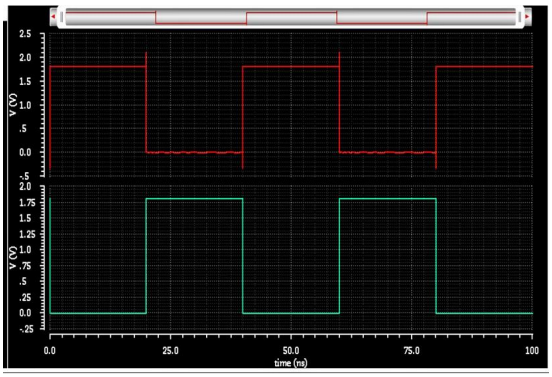

Fig 4.2.1 : Forced NMOS Inverter Transient response

Circuit in Figure 3.2 is simulated and resulting transient output waveform is shown in Figure 4.2.1 and the delay is 3.699 psec.

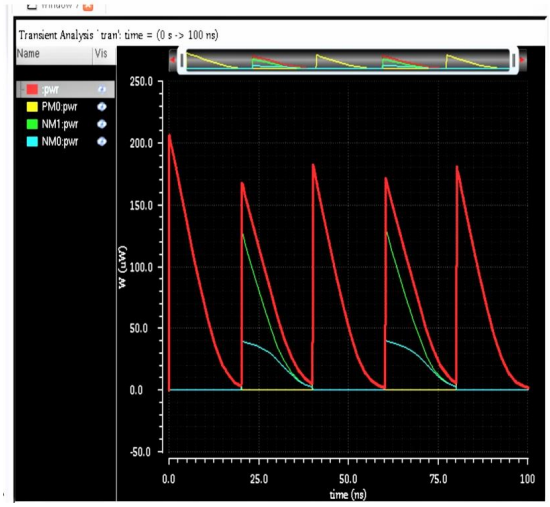

Fig 4.2.2 : Instantaneous power consumption in the Forced NMOS Inverter

Figure 4.2.2 shows the instantaneous power consumption in the Forced NMOS Inverter and it is 76.14 µW.

C. Modified Forced NMOS Inverter with a Parallel diode connected PMOS Design

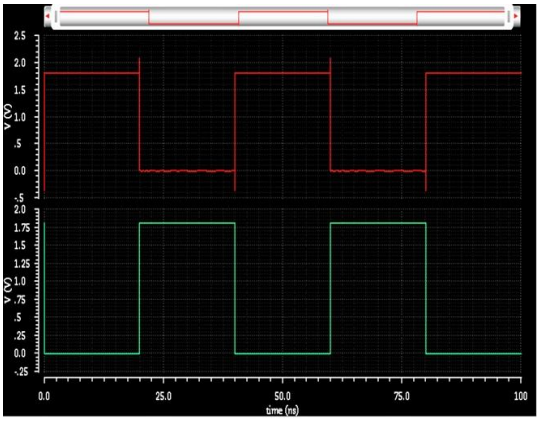

Fig 4.3.1 : Transient response of the modified Forced NMOS Inverter with a Parallel diode connected PMOS

Circuit shown in Figure 3.3 is simulated and and resulting transient output waveform is shown in Figure 4.3.1 and the delay is 4.386 psec.

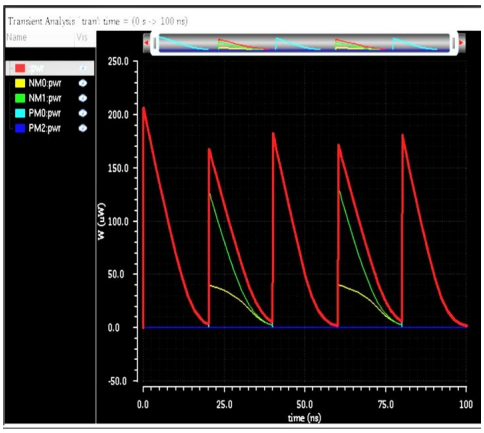

Fig 4.3.2 : Instantaneous power consumption in the modified Forced NMOS Inverter with a Parallel diode connected PMOS

Fig 4.3.2 shows the instantaneous power consumption in the modified Forced NMOS Inverter with a Parallel diode connected PMOS and it is 70.32 µW.

Table 4.1 : Comparison of delay and power consumption in different types of inverters

	Conventional	Forced NMOS	Modified Forced NMOS
Delay (in ps)	2.165	3.699	4.386
Power Consumption (in µW)	89.88	76.14	70.32

Table 4.1 shows the comparison of the delay and power consumption in different types of inverters. It has been observed that power consumption decreases in the modified Forced NMOS Inverter with a Parallel diode connected PMOS.

V. CONCLUSION

This paper proposes Modified Forced NMOS inverter design for low power consumption. Power consumption reduction of around 22% is observed in this method even though a increase in the delay metric. As the channel length further decreases, power consumption further decreases. Also inverters are the basic circuits and used in large numbers in the design of VLSI circuits. In that case, overall reduction in power consumption will be significant. Effect of optimal W/L of the different transistors on power consumption and delay is required to analyze.

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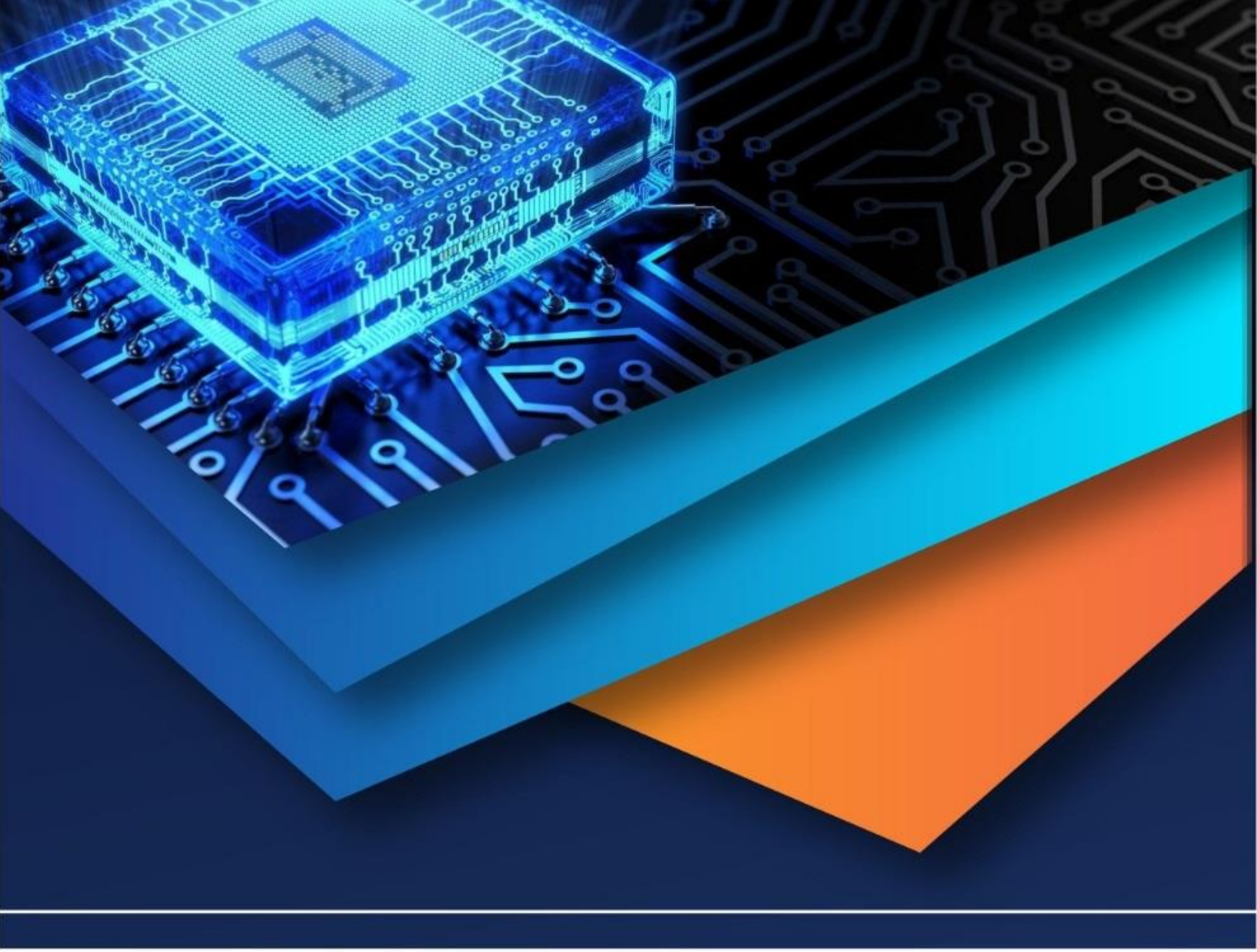

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