Volume 3 Issue IX, September 2015
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

Design of Multioutput High Speed Adder Using Domino Circuit

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Abstract— Dynamic gates have been excellent choice in the design of high-performance modules such as full adders, subtractors, multipliers, registers, multiplexers and comparators in modern microprocessors. However, the main drawback of dynamic gates is their relatively low noise margin compared to that of standard static logic gates. Traditionally, this problem has been resolved by employing a PMOS keeper transistor in the pull up network that compensates for the sub threshold leakage current of the pull-down NMOS network. In this paper, a new Multioutput ripple carry adder is designed using a technique called current comparison based domino circuit. In this method, a single current mirror circuit is used to track threshold voltage variation in dynamic node. This technique also reduces parasitic capacitance on the dynamic node.
Keywords— Domino logic,CCD domino circuit, leakage power, power consumption.

I. INTRODUCTION

Dynamic logic gates and circuits have been excellent choice in the design of high-performance modules such as multiple bit adders, subtractors, multipliers, comparators, multiplexers, registers, etc in modern VLSI microprocessors [1]. The advancement in fabrication technology along with the shrinking device size has allowed for placement of nearly two billion transistors on Intel's latest processor [2]. The digital logic gates and circuits designed using dynamic domino technique is considerably faster than the logic gates and circuits designed with standard static logic style. The aggressive technology scaling to improve the performance as well as the integration level makes the noise play a major role in design parameters like area, power and speed [3]. Therefore the digital integrated circuit noise has become one of the most important issues in the design of deep submicron VLSI chips [4]- [9]. The robustness and performance of wide fan-in dynamic circuits significantly degrade with increasing levels of process variations and sub threshold leakage.

A number of design techniques such as PMOS feedback keeper transistor method to prevent the dynamic node floating problem, precharging the internal nodes to eliminate the charge sharing problem and weak complementary p-network is constructed to improve the noise tolerance to the level of skewed static CMOS logic gates, have been developed in the past three decades to minimize the effect of noise in dynamic circuits [6]. It is also shown that voltage scaling aggravates the crosstalk noise in the dynamic circuits and reduces circuit noise immunity, motivating the need for noise-tolerant circuit design [10]-[12]. To design a high performance domino logic circuit, there are two most important factors to be considered when designing a keeper circuit. The first factor is the additional loading caused by the keeper and its control circuits and the second factor is the keeper circuit should be capable of switching off very fast [13]. If the keeper circuit remains ON during evaluation it will compete for longer time with the NMOS network during the pull down process. Designing feedback keeper circuit for wide fan-in gates is a challenging task since the leakage current largely depends on increase in variability [14].

In this paper, a 256-bit ripple carry adder circuit is designed using a technique called current comparison based domino (CCD) that enables faster switching and tracks the variation of threshold voltage in the dynamic node[15] and its performance is compared with other domino circuit. In this paper the effect of temperature on the circuit performance is analysed in detail by sweeping the temperature from 25^0C to 70^0C.

The performance of the dynamic circuits can be significantly improved by precise design and properly sizing the transistors. Usually in all the digital circuits the transistor gate length remains uniform. So the size of the transistor in digital circuits depends on the width of the transistor. In this paper the multiple bit domino adders are implemented with L=0.016nm technology along with a supply voltage of 0.7V. The noise sensitivity of the domino circuits depends on the threshold voltage of the transistors used in the circuit and since the transistor size is decreasing year by year due to aggressive scaling trends in modern electrons, due to the low threshold voltage, the circuits should be more sensitive to noise that necessitates the use of noise tolerant circuits design techniques.

The paper is organized as follows. Section II details the circuit implementation and operation of the 4-bit adder using three different

Volume 3 Issue IX, September 2015
ISSN: 2321-9653
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domino techniques. Section III compares the performance of these full adder circuits using the simulated results. Section IV concludes the paper.

II. EXISTING SYSTEM

The circuit diagram of a full adder circuit implemented using current mirror domino (LCR) technique is shown in fig.1 and its layout is shown in fig.2. The full adder circuit implemented using leakage current replica (LCR) keeper domino technique uses an analog current mirror to replicate the leakage current of the pull-down network and it tracks process, voltage, and temperature.The block diagram of the adder circuit implemented using the LCR technique is shown in fig.3.The timing diagram of the adder using LCR technique is shown in Fig.4.

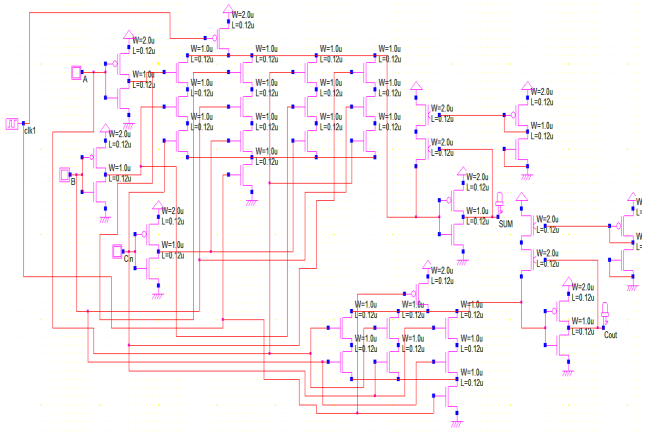

Fig.1. Full Adder circuit using current mirror domino logic

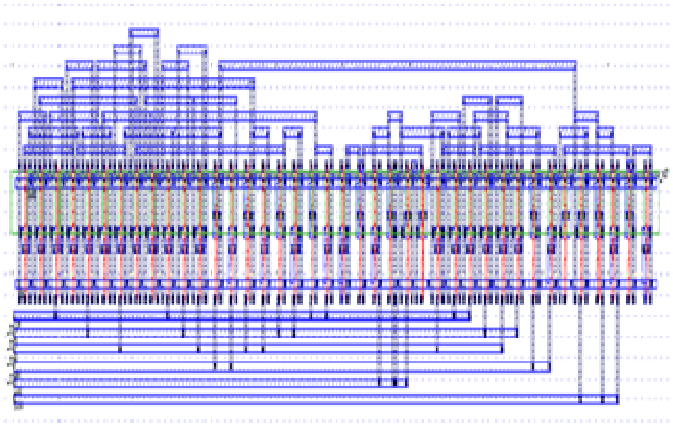

Fig.2. Layout of the Full Adder circuit using current mirror domino logic

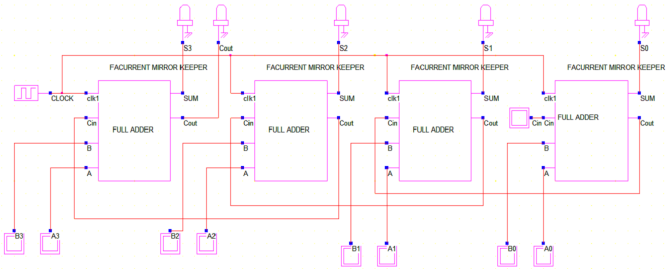

Fig.3 Block diagram of 4-Bit adder using current mirror domino logic

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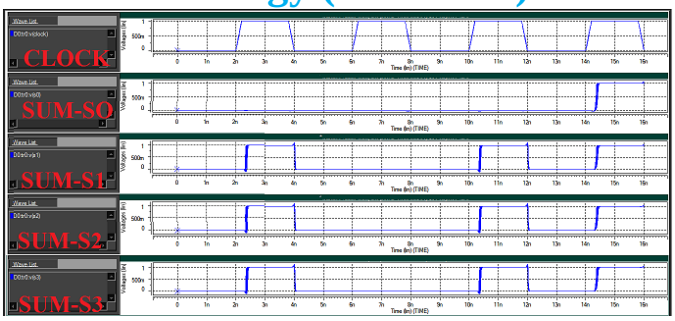

Fig.4 Timing diagram of the adder using high current mirror logic

In this full adder circuit a current mirror is connected to the keeper which compensates for the sub threshold leakage current of the pull-down network. This current mirror circuit can be shared for all the logic gates in the circuit. In this configuration the keeper and current mirror circuit minimizes the delay of the circuit (delay in the order of pico seconds) by minimizing the effect of charge sharing. This circuit need proper selection of clock signal. If the clock frequency exceeds 500MHz, the performance of the adder circuit degrades.

The LCR technique is useful for constructing wide fan in circuits such as multiple bit adders, registers, multiplexers etc. This adder circuit has the area overhead of an extra NMOS transistor which is connected to the keeper from the current mirror circuit. This adder circuit has much better noise margin, low leakage current and low power consumption. But the performance of LCR is degraded. To improve the performance of adder, we implement technique called current comparison based domino. By using this technique we design ripple carry adder to reduce delay and leakage current.

III. PROPOSED WORK

Adders are of fundamental importance in a wide variety of digital systems. Many fast adders exist, but adding fast using low area and power is still challenging. The importance of a fast, low-cost binary adder in a digital system is difficult to overestimate. Not only are adders used in every arithmetic operation, they are also needed for computing the physical address in virtually every memory fetch operation in most modern CPUs. Adders are also used in many other digital systems including telecommunications systems in places where a full-fledged CPU would be superfluous. More recently, carry-skip adders, Carry-look-ahead and carry-select adders are very fast but far larger and consume much more power than ripple carry adder.

In this paper, we design a ripple carry adder using CCD technique shown in Fig.5 and layout diagram of this adder is shown in Fig.6. This adder consumes only low power. By changing the circuit design we can reduces delay of the adder. So, here a new technique is proposed for ripple carry adder.

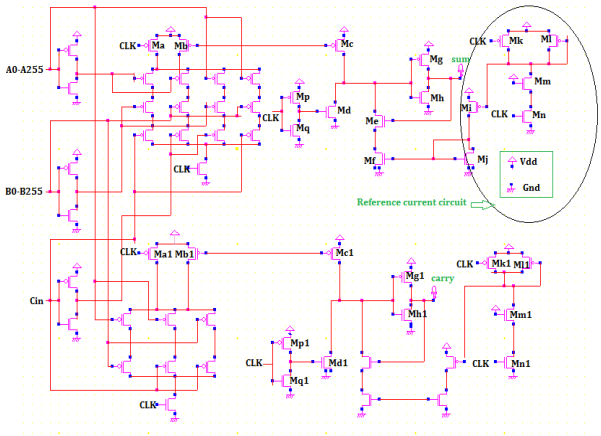

Fig.5 CCD based Ripple Carry Adder

When threshold voltage in the dynamic node decrease compared to desire level, the leakage current in the circuit increases. So the delay and power consumption of the circuit increases. To reduce leakage current, reference current circuit used in this technique to

compensates threshold voltage variation in the dynamic node. This circuit operates in two phases.

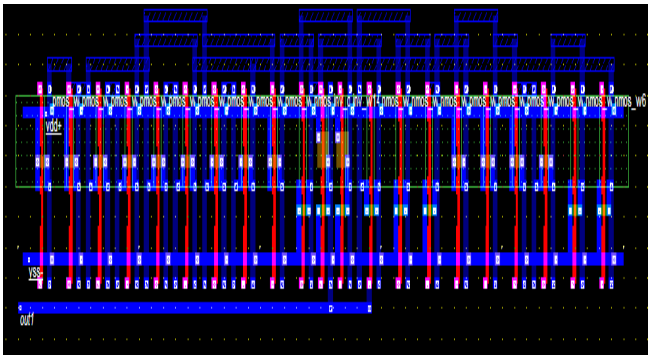

Fig.6 Layout of the CCD based Ripple Carry Adder

A. Predischarge Phase

Input signals and clock voltage are in high and low levels, respectively, [CLK = "0", CLKB = "1" and of the RS signal is high in Fig 5] in this phase. Therefore, the voltages of the dynamic node (Dyn) and node A have fallen to the low level by transistor Md and raise to the high level by transistor Ma, respectively. Hence, transistors Ma, Md, Me, and Mf are on and transistors M_1, M_2, and Mo are off. Also, the output voltage is raised to the high level by the output inverter.

B. Evaluation Phase

In this phase, clock voltage is in the high level [CLK = "1", CLKB = "0" and RS= either "0" or "1" in Fig. 5] and input signals can be in the low level. Hence, transistors Ma and Md are off, transistor Mb, Mc, Mf, and Mo are on, and transistor Me can become on or off depending on input voltages. Thus, two states may occur. First, all of the input signals remain high. Second, at least one input falls to the low level. In the first state, a small amount of voltage is established across transistor Mb due to the leakage current. Although this leakage current is mirrored by transistor Mc, the keeper transistors of the second stage (Me and Mf) compensate this mirrored leakage current. It is clear that upsizing the transistor Mb and increasing the mirror ratio (M) increase the speed due to higher mirrored current at the expense of noise-immunity degradation. In the second state, when at least one conduction path exists, the pull-up current flow is raised and the voltage of node A is decreased to nonzero voltage, which is equal to gate-source voltage of the saturated transistor Mb. This voltage is also equal to drain-source voltage of Mb and depends on size of Mb and its current. Increasing the pull-up current increases the mirrored current in transistor Mc, thus voltage of the dynamic node Dyn is charged to VDD, yielding discharging the voltage of the output node and turning off the main keeper transistor Me. By this technique the contention current between the keeper transistor and the mirror transistor is mitigated. Timing diagram of 256-bit CCD based ripple carry adder is shown in below.

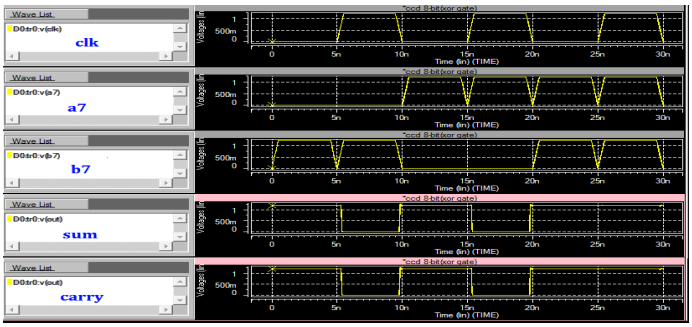

Fig.7 Timing Diagram

IV. SIMULATION RESULTS

The simulations were performed using L=16nm technology along with the supply voltage V_{DD}=0.7V. In this paper a 256-bit wide fan-in gate for adder is constructed using CCD based domino technique. Since a single reference current structure can be shared among more than one domino logic circuits, the CCD technique is useful for constructing wide fan in circuits such as multiple bit registers, multiplexers etc. This adder circuit has much better noise margin, low leakage current and low power consumption

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ISSN: 2321-9653

compared to other circuits designed using domino logic styles with traditional feedback keepers.

In this work the temperature is varied from 25^0C to 70^0C. From the fig.8 it is clear that as the temperature increases the transition delay also increases due to the increase in leakage current.

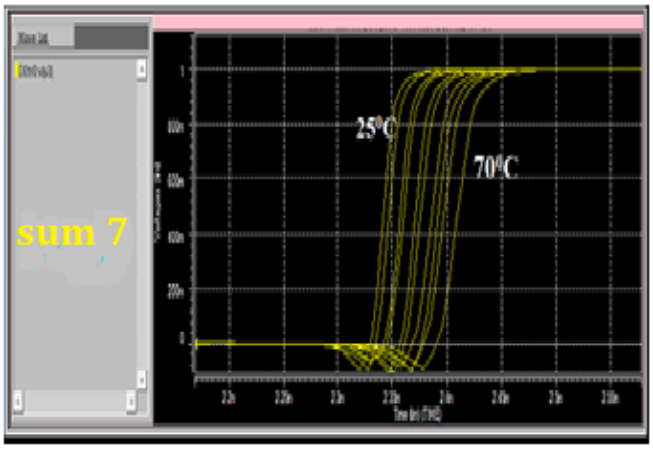

Fig.8 Effect of temperature on the performance of 256-bit adder using CCD

The simulation result of adder is shown in Fig.9. This result shows CCD technique has less noise in the output. It also gives voltage at the different node.

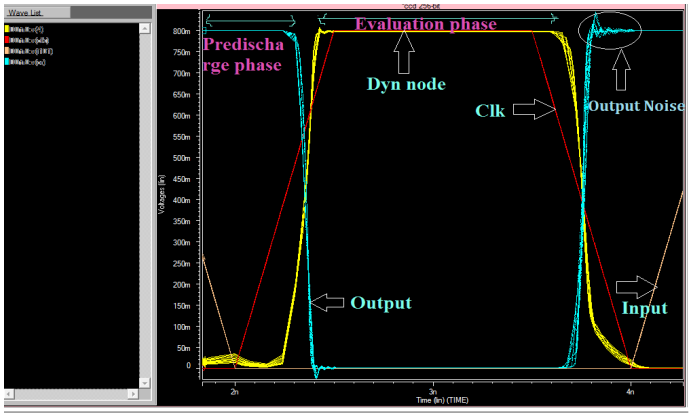

Fig.9 Simulation Result

The CCD based ripple carry adder is analyzed with different domino ripple carry adder and performances of all types of adders are compared with delay and power consumption. The table-1 & 2 shows sum and carry delay of all types of adder. By this, we can conclude the CCD based ripple carry adder has less delay compared to other domino adder.

Technique	Sum Delay (ps)
SFLD	458.63
SFD	486.27
HSD	360.73
LCR	332.12
RSK	254.93
DFD	198.37
CCD	153.74

Table-1 Sum Delay Comparison

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Technique	Carry Delay(ps)
SFLD	189.72
SFD	203.39
HSD	167.57
LCR	135.53
RSK	89.63
DFD	57.42
CCD	8.859

Table-2 Carry Delay Comparison

The power consumption of all types of adder is shown in Table-3. By this table, we conclude that CCD based ripple carry adder require less power for operation.

Technique	Power Consumption(mW)
SFLD	22.087
SFD	22.38
HSD	19.29
LCR	17.61
RSK	13.74
DFD	7.635
CCD	3.467

Table-3 Power Consumption Comparison

V. CONCLUSIONS

A new domino circuit called CCD technique is proposed for full adder circuit design. This technique is necessary to reduce the leakage current in the evaluation phase. The leakage current is also reduced when we scale down the technology. By using this technique, the power dissipation, parasitic capacitance and keeper transistor size is also reduced. Using the high-performance PTM V2.1 of 16 nm at power supplies of 0.7V, wide fan-in 256-bit adder gate circuits were used as a benchmark. The proposed design plus existing circuit designs were simulated and compared. Simulation results demonstrated significant progress in leakage reduction and acceptable speed for high-speed applications.

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