iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 3 **Issue:** X **Month of publication:** October 2015

DOI:

www.ijraset.com

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International Journal for Research in Applied Science & Engineering Technology (IJRASET)

0.18µm CMOS Based Divider for Wireless Applications Using Wideband Prescalar

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Abstract---Wireless LAN (WLAN) in the multigigahertz bands, such as HiperLAN II and IEEE 802.11a/b/g, are recognized as leading standards for high-rate data transmissions and standards like IEEE 802.15.4 are recognized for low-rate data transmissions. The demand for lower cost, lower power and multiband RF circuits increased in conjunction with need of higher level of integration. The frequency synthesizer, usually implemented by a phase-locked loop (PLL), is one of the power-hungry blocks in the RF front-end and the first-stage frequency divider consumes a large portion of power in a frequency synthesizer. In this paper, a wideband 2/3 prescaler is verified in the design of proposed wide band and multimodulus 32/33/47/48 prescaler. A dynamic logic multiband flexible integer-N divider is designed which uses the wideband 2/3 prescaler, multimodulus 32/33/47/48 prescaler. However, the P and S counters are programmed accordingly. From the synthesis report the minimum period and the maximum frequency required to maintain the functionality are 3.606ns and 277.316MHz.The proposed design consumes the power dynamically according to the corresponding selected FPGA.
Keywords: DFF, Dynamic Logic, Dual Modulus Prescalar, E-TSPC.

I. INTRODUCTION

In this paper, a dynamic logic multiband flexible integer-N divider based on pulse-swallow topology is proposed which uses a low-power wideband 2/3 prescaler and a wideband multimodulus 32/33/47/48 prescaler. The divider also uses an improved low-power loadable bit-cell for the Swallow S counter. The integrated synthesizers for WLAN applications at 5GHz reported in [1] and [2] consume up to 25mW in CMOS realizations, where the first-stage divider is implemented using an injection-locked divider which consumes large chip area and has a narrow locking range. The best published frequency synthesizer at 5GHz consumes 9.7mW at 1-V supply, where its complete divider consumes power around 6mW[3].

The frequency synthesizer is one of the basic building blocks in modern communication systems. The operating frequency of the frequency synthesizer is limited by the frequency divider and the voltage-controlled oscillator. The function of channel selection in the frequency synthesizer demands programmable division ratios for the frequency divider.Dynamic latches are faster and consumes less power compared to static dividers. The TSPC[5] and ETSPC[8] designs are able to drive the dynamic latch with a single clock phase and avoid skew problem[5].However, the adoption of single-phase clock latches in frequency dividers has been limited to PLLs with applications below 5GHz[7],[8].

The integer-N frequency synthesizer is more practical, less costly and of low spurious sideband performance as compared with the fractional-N frequency synthesizer . It is usually formed by a prescaler, a program counter (P counter) and a swallow counter(S counter). Such a topology can provide a programmable division ratio of N *P + S, where N, P and S are the division ratios of three blocks respectively. The prescaler provides a dual-modulus of N=N +1. The P counter provides a fixed division ratio according to the requirement of the overall division ratio, while the continuous division ratios from 3 to 2n is achieved through the S counter by periodically reloading the divide-by-2 stages, where n is the number of stages of the S counter. The continuous division ratio is used to select the desired channels. Much research has been focused on the prescaler design for its highest operating frequency . However, in the modern communication system, there is an increasing demand for multi-standards applications. The requirement for wide band and high resolution operations continue to be the problems. To satisfy these requirements, different reference frequencies, and different arrangement for N, P and S counters are selected for different applications.For example only UN II bands are covered. In this paper, a new wide-band high resolution programmable frequency divider is proposed. The wide band and high resolution are obtained by using the all-stage programmable topology in both counters , the high-speed frequency divider is a key block in frequency synthesis. The prescaler is the most challenging part in the high-speed frequency-divider design

because it operates at the highest input frequency. A dual-modulus prescaler usually consists of a divide-by-2/3 (or 4/5) unit followed by several asynchronous divide-by-2 units. The operation of the divide-by-2/3 unit at the highest input frequency makes it the bottleneck of the prescaler design. To achieve the two different division ratios, D flip-flops (DFFs) and additional logic gates, which reduce the operating frequency by introducing an additional propagation delay, are used in the unit. The power consumption of this divide-by-2/3 unit, which is the greatest portion of the total power consumption in the prescaler, significantly increases due to the power consumption of the additional components.

II. PROPOSED SYSTEM

The proposed wideband multimodulus prescaler which can divide the input frequency by 32, 33, 47, and 48 It is similar to the 32/33 prescaler, but with an additional inverter and a multiplexer. The proposed prescaler performs additional divisions (divide- by-47 and divide-by-48) without any extra flip-flop, thus saving a considerable amount of power and also reducing the complexity of multiband divider which will be discussed in Section V. The multimodulus prescaler consists of the wideband 2/3 N1/(N1+1)) prescale, four aysnchronous TSPC divide-by-2 circuits (AD=16) and combinational logic circuits to achieve multiple division ratios. Beside the usual MOD signal for controlling (N/N+1)divisions, the additional control signal sel is used to switch the prescaler between 32/33 and 47/48 modes.

A. Methodology

Wireless LAN (WLAN) in the multigigahertz bands, such as HiperLAN II and IEEE 802.11a/b/g, are recognized as leading standards for high-rate data transmissions and standards like IEEE 802.15.4 are recognized for low-rate data transmissions. The demand for lower cost, lower power, and multiband RF circuits increased in conjunction with need of higher level of integration. The frequency synthesizer, usually implemented by a phase-locked loop (PLL), is one of the power-hungry blocks in the RF front-end and the first-stage frequency divider consumes a large portion of power in a frequency synthesizer. The battery life for mobile applications is inversely proportional to the energy consumption of mobile devices. Thus it is important to mninimize the energy consumption by mninimizing both the active duty-cycle and the active power consumption of a wireless termninal concurrently. The active duty-cycle of a ZigBee wireless node strongly depends on the frequency settling time of a PLL, since the settling time is a domninant portion of the total active period. Generally speaking, the frequency settling time of a PLL decreases as the loop-bandwidth increases. Since a fractional-N PLL with higher reference frequency can achieve a wider loop bandwidth, it has been favored for small active duty-cycle. However, it requires a high frequency fractional controller such as a YIA-modulator, and thus increases the hardware complexity and active power consumption. In this paper, a new frequency synthesizer with very short frequency settling time and low active power consumption is introduced. For short frequency settling time, a two-point channel control scheme composed of a direct-VCO control (compensation-path) and a divider control (main-path) is used. The key parameters of high-speed digital circuits are the propagation delay and power consumption. The maximum operating frequency of a digital circuit is calculated.

$$F_{max} = \frac{1}{T_{PLH}+T_{PHL}} \quad (1)$$

Here T_{PLH} and $T_{PHL}$are the propagation delays of the low-to-high and high-to-low transitions of the gates, respectively.
The total power consumption of the CMOS digital circuits is determined by switching and short circuit power. The switching power is linearly proportional to the operating frequency and is given by the sum of switching power at each output node as in

$$P_{switching} = \sum_{i=1}^{n} f_{clk} C_{li} V_{dd}^2 \quad (2)$$

Where n is the number of switching nodes, Fclk is the clock frequency, C_{Li} is the load capacitance at the output node of the ith stage, and V_{dd} is the supply voltage. Normally, the short-circuit power occurs in dynamic circuits when there exists direct paths from the supply to ground which is given by

$$P_{sc} = I_{sc} V_{dd} \quad (3)$$

Where Isc is the short-circuit current. The analysis shows that the short-circuit power is much higher in E-TSPC logic circuits than n

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ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

TSPC logic circuits. However, TSPC logic circuits exhibit higher switching power compared to that of E-TSPC logic circuits due to high load capacitance. For the E-TSPC logic circuit, the short-circuit power is the major problem. The E-TSPC cicuit has the merit of higher operating frequency than that of the TSPC circuit due to the reduction in load capacitance, but it consumes significantly more power than the TSPC circuit does for a given transistor size. The following analysis s based on the latest design using the popular and low-cost 0.18-microm CMOS process.

B. Wideband 2/3 Prescaler

The E-TSPC 2/3 prescaler reported in consumes large shortcircuit power and has a higher frequency of operation than that of 2/3 prescaler. The wideband single-phase clock 2/3 prescaler used in this design was reported which consists of two D-flip-flops and two NOR gates embedded in the flip-flops as in Fig. 2. The first NOR gate is embedded in the last stage of DFF1, and the second NOR gate is embedded in the first stage of DFF2 . Here, the transistors M2,M25, M4, and M8 in DFF1 helps to eliminate the short-circuit power during the divide-by-2 operation. The switching of division ratios between 2 and 3 is controlled by logic signal MC.

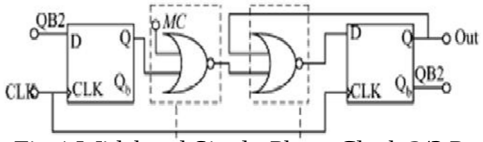

Fig.1 Wideband Single-Phase Clock 2/3 Prescaler

When MC switches from “0” to “1,” transistors M2, M4 and M8 in DFF1 turns off and nodes S1, S2 and S3 switch to logic “0.” Since node S3 is “0” and the other input to the NOR gate embedded in DFF2 is Qb, the wideband prescaler operates at the divide-by-2 mode. During this mode, nodes S1, S2 and S3 switch to logic “0” and remain at “0” for the entire divide-by-2 operation, thus removing the switching power contribution of DFF1. Since one of the transistors is always OFF in each stage of DFF1, the short-circuit power in DFF1 and the first stage of DFF2 is negligible. The total power consumption of the prescaler in the divide-by-2 mode is equal to the switching power in

DFF2 and the short-circuit power in second and thirrd stages of DFF2. Where C_{Li} is the load capacitance at the output node of the i th stage of DFF2, and Psc1 and Psc2 are the short-circuit power in the second and third stages of DFF2.

When logic signal MC switches from “1” to “0,” the logic value at the input of DFF1 is transfered to the input of DFF2 as one of the input of the NOR gate embedded in DFF1 is “0” and the wideband prescaler operates at the divide-by-3 mode. During the divide-by-2 operation, only DFF2 actively participates in the operation and contributes to the total power consumption since all the switching activities are blocked in DFF1. Thus, the wideband 2/3 prescaler has benifit of saving more than 50% of power during the divide-by-2 operation.

C. Multimodulus 32/33/47/48 Prescaler

The proposed wideband multimodulus prescaler which can divide the input frequency by 32, 33, 47, and 48 is shown in Fig. 4. It is similar to the 32/33 prescaler used in, but with an additional inverter and a multiplexer. The proposed prescaler performs additional divisions (divide- by-47 and divide-by-48) without any extra flip-flop, thus saving a considerable amount of power and also reducing the complexity of multiband divider which will be discussed in Section V. The multimodulus prescaler consists of the wideband 2/3 (N1/(N+1))prescaler [10], four asynchronous TSPC divide-by-2 circuits ((AD)=16) and combinational logic circuits to achieve multiple division ratios. Beside the usual MOD signal for controlling N(N+1) divisions, the additional control signal Scl is used to switch the prescaler between 32/33 and 47/48 modes.

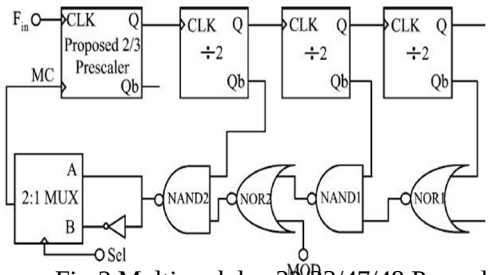

Fig.2 Multimodulus 32/33/47/48 Prescaler

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Case 1: Sel='0'

When Sel=0 , the output from the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulus prescaler operates as the normal 32/33 prescaler, where the division ratio is controlled by the logic signal MOD. If MC=1, the 2/3 prescaler operates in the divide-by-2 mode and when MC , the 2/3 prescaler operates in the divide-by-3 mode. If MOD =1, the NAND2 gate output switches to logic "1"(MC=1)and the wideband prescaler operates in the divide- by-2 mode for entire operation. The division ratio N performed by the multimodulus prescaler is

$$N = (AD*N1)+(0*(N1+1)) = 32 \quad (4)$$

Where N=2 and AD=16 is fixed for the entire design. If MOD=0 , for 30 input clock cycles MC remains at logic "1", where wideband prescaler operates in divide-by-2 mode and, for three input clock cycles, MC remains at logic "0" where the wideband prescaler operates in the divide-by-3 mode. The division ratio N+1 performed by the multimodulus prescaler is

$$N+1 = ((AD1)*N1)+(1*(N1+1))=33 \quad (5)$$

Case 2: Sel = 1

When Sel = 1, the inverted output of the NAND2 gate is directly transfered to the input of 2/3 prescaler and the multimodulus prescaler operates as a 47/48 prescaler, where the division ratio is controlled by the logic signal MOD. If MC = 1, the 2/3 prescaler operates in divide-by-3 mode and when MC=0, the 2/3 prescaler operates in divide-by-2 mode which is quite opposite to the operation performed when Sel=0. If MOD = 1, the division ratio N+1 performed by the multi modulus prescaler is same as except that the wideband prescaler operates in the divide-by-3 mode for the entire operation

given by

$$N+1 = ((AD *(N1+1))+(0*N1)) = 48 \quad (6)$$

If MOD = 1, the division ratio N performed by the multi modulus prescaler is

$$N = ((AD - 1) * (N1+1)) + (1*N1) = 47 \quad (7)$$

D. Program Counter

The program counter is responsible for counting *P* pulses of SlowCLK before outputting a pulse to the phase/frequency detector and resetting itself and the swallow counter. The implementation used in this project, using a 7-bit ripple counter, a 7-bit comparator, and a zero-detector is shown in Figure 12. The ripple counter is clocked by SlowCLK, and increments its count by one each clock cycle. At each stage, the 7-bit comparator compares each count bit to the corresponding bit in the control signal, and outputs a 0 for each equal bit. When the zero-detector detects equivalence in all of the 7 bits, indicating that the desired count has been reached, Fout is driven high. On the next clock cycle, the program counter is reset to zero and the count is restarted. In addition, the output pulse on Fout is used to reset the count of the swallow counter, indicating the end of one complete cycle of the frequency divider. The ripple counter is implemented using 7 cascaded D-type flip-flops, each arranged in a toggle configuration. The output of each flip-flop is used to clock the next flip-flop. Since the output of each flip-flop inverts on every clock cycle, each flip-flop essentially divides its clock by two, causing the next stage of the ripple counter to be clocked at half the rate of the previous flip flop. Each flip-flop was designed to respond to the falling edge of its clock, when the output of the previous stage changes from a 1 to a 0.

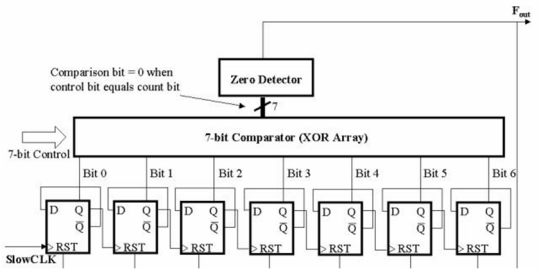

Fig.3 Block Diagram Of a 7-bit Program Counter

In this way, an incrementing binary count is achieved with the outputs of each flip-flop forming the bits of the count. Since the program counter contains 7-bits, any count between 0 and 127 can be set by the control signal. It is important to realize however that

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in order to achieve a division ratio as specified in the equation *DIV=NP+S*, the control signal must be set to *P-1*, since the zero-state is included in the count.

E. Swallow Counter

The swallow counter, as indicated in Figure 4, is used to count *S* pulses of SlowCLK before asserting the modulus control signal and changing the modulus of the DMP to *N*. A block diagram of the swallow counter is provided in Figure 4. By looking at Figure 4, the similarities between the swallow counter and the program counter are apparent. Once again, the count (6-bits in this case) is maintained using a ripple counter comprised of cascaded flip-flops clocked with SlowCLK. In addition, a comparator compares each count bit with its corresponding bit in the control signal, and a zero-detector asserts modulus control when all bits are equal. However, the swallow counter does not reset when the count is reached, but masks the input clock using an AND gate connected to the inverse of modulus control. As a result, the ripple counter stops counting when the count is reached, and the state of the circuit is maintained until a reset signal (SwallowRST) is received from the program counter. Since the swallow counter contains 6 bits, it is capable of any count from 0 to 64. Once again, the control signal must be set to *S-1*, since the zero-state is included in the count.

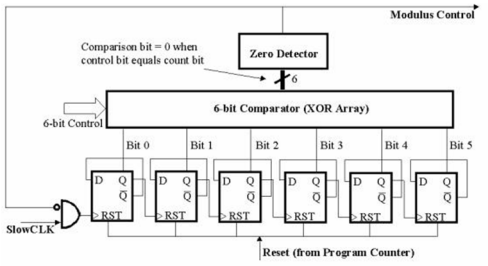

Fig.4 Block Diagram of A 6-bit Swallow Counter

F. Prescalar 2/3

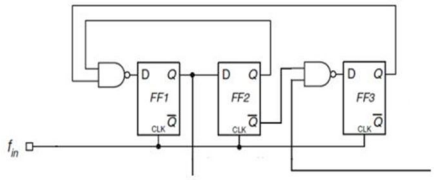

Fig.5 Prescaler_2 by 3

The multimodulus prescalar consists of the wideband 2/3 (N_1/N_1+1) prescalr[10], four asynchronous TSPC divide-by-2 circuits ((AD)=16) and combinational logic circuits to achieve multiple division ratios.The 203 presaclar can divide the frequency by the 2 modulus divisers, i.e 32/33 and 47/48 division ratios as desired division by the input.

G. Multiprescaler

The 4/5 prescaler reported in consumes large short circuit power and has a higher frequency of operation than that of 4/5 prescaler. The wideband single-phase clock 4/5 prescaler used in this design, which consists of Three D-flip-flops and two Nand gates embedded. The Multi prescaler 4by5 consist of Four D-flip flop, two nand gates, and two or gates one not gate with main 4/5 prescaler circuit. The multi modulus prescaler operates as the normal 64/65/78/79.

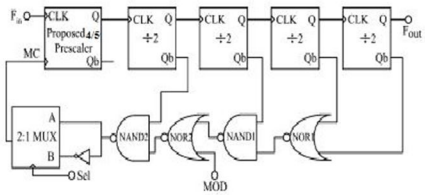

Fig.6 Multi Prescaler

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III. PROPOSED MULTIBAND FLEXIBLE DIVIDER

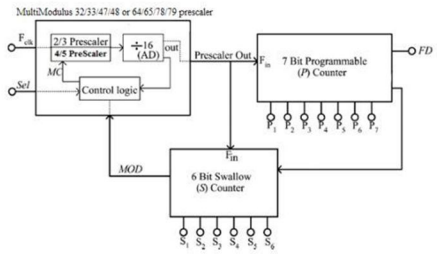

Fig7.Multiband Flexible Divider

Our proposed multiband flexible divider is Combined by 2/3 Prescaler and 4/5 Prescaler in multi modulus Prescaler. By using mux we can operate either 2/3 Prescaler and 4/5 Prescaler. The mux input gets from the NAND logic by the 2 inputs os A and B.The signal generated from mux is control signal 'MC'. It controls the prescalar selection in multimodulus prescalar.And it decides in which division it has to operate.That is it will operate 32/33/47/48 or 64/65/78/79 bandwidth.

IV. RESULTS ANALYSIS

A. In section, we present our experimental simulation and synthesis results. We also present comparison of our method with other existing method.

Table I: Device Performance

Reference	[9]	[6]	Proposed
Process(µm)	0.18	0.25	0.18
Supply Voltage(V)	1.0	1.8	1.8
Frequency Range (GHz)	2.4-2.7/5.14-5.7	5.14-5.7	2.4-2.484/5-5.825
Resolution(MHz)	9.375/20	20	1,2,5,10,20
Power(mW)	2.7	6.25	0.9602.2

Table II presents the device including No. of slice resigters,,No of slice LUTs, No. of IOBs , No. of BUFG/BUFG CTRLs

Table II: Device Utilization Summary

Logic utilization	Used	Available	Utilization
No.of slice registers	48	10000	0%
No.of slice LUTs	35	5000	0%
No.of fully used LUT-FF pairs	31	52	59%
No.of IOBs	18	200	9%
No.of BUFG/BUFG CTRLs	1	32	3%

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B. Simulation Reports

1) Vscounter

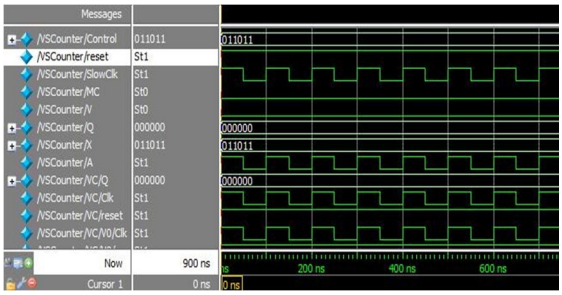

Fig 8: VS Counter

The 6-bit swallow counter programmable from 0 to 31 for low-frequency band and from 0 to 47 for the high-frequency band.It designed with a bit cell. If is logically high, nodes S1 and S2 switch to logic "0" and the bit-cell does not per-form any function. The signal goes logically high only when the S-counter finishes counting down to zero.

As per synthesis report the time dalay os VSConter is 1.045ns.

2) Prescalar: Prescalar can divides the given frequency based on mode selected i.e. 2/3 modes.When 'MC' control generates by Swallow counter the prescalar starts the division of input clock frequency.

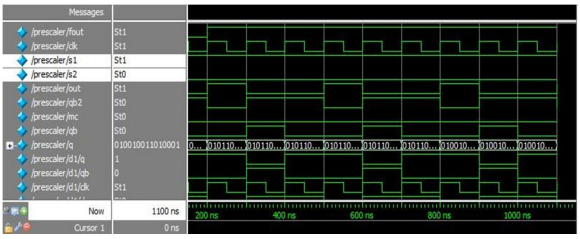

Fig.9 Presclar

Table III

Performance of different 2/3 prescalars at 2.5GHz

Design Parameters	[6]	[12]	Proposed
Process(µm)	0.18	0.18	0.18
Supply Voltage(V)	1.8	1.8	1.8
Max.Frequency (GHz)(Sim/Measured)	6.7/5.3	7.5/6	8/6.5
Power(mW)(Sim/Measured) Divide-by-2 mode	1.88/1.92	1.63/2.2	0.82/0.97
Power(mW)(Sim/Measured) Divide-by-3 mode	2.18/2.26	1.85/2.62	1.61/1.78

3) Top Module

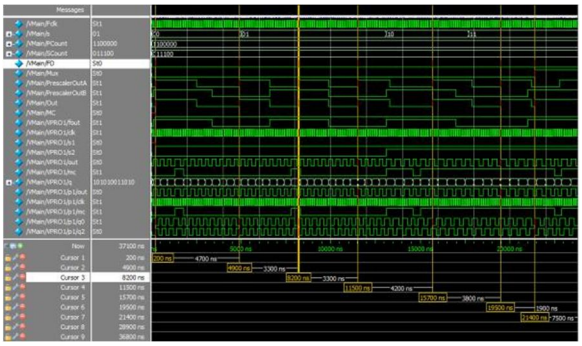

Fig.10 Top Module

As per synthesis report the time taken by the signal to reach FD(Frequency Division Output) from 'P' Counter is 1.364ns.By the outputs of Program counter and Swallow counter output FD generates.The two controls of Swallow counter and Program counter maintains the total control of multimodulus prescalar divisions.

V. CONCLUSION

In this paper, a new wide-band high resolution programmable frequency divider is proposed. The wide band and high resolution are obtained by using the all-stage programmable topology in both counters, The high-speed frequency divider is a key block in frequency synthesis. The prescaler is the most challenging part in the high-speed frequency-divider design because it operates at the highest input frequency. From the synthesis report the minimum period and the maximum frequency required to maintain the functionality are 3.606ns and 277.316MHz.

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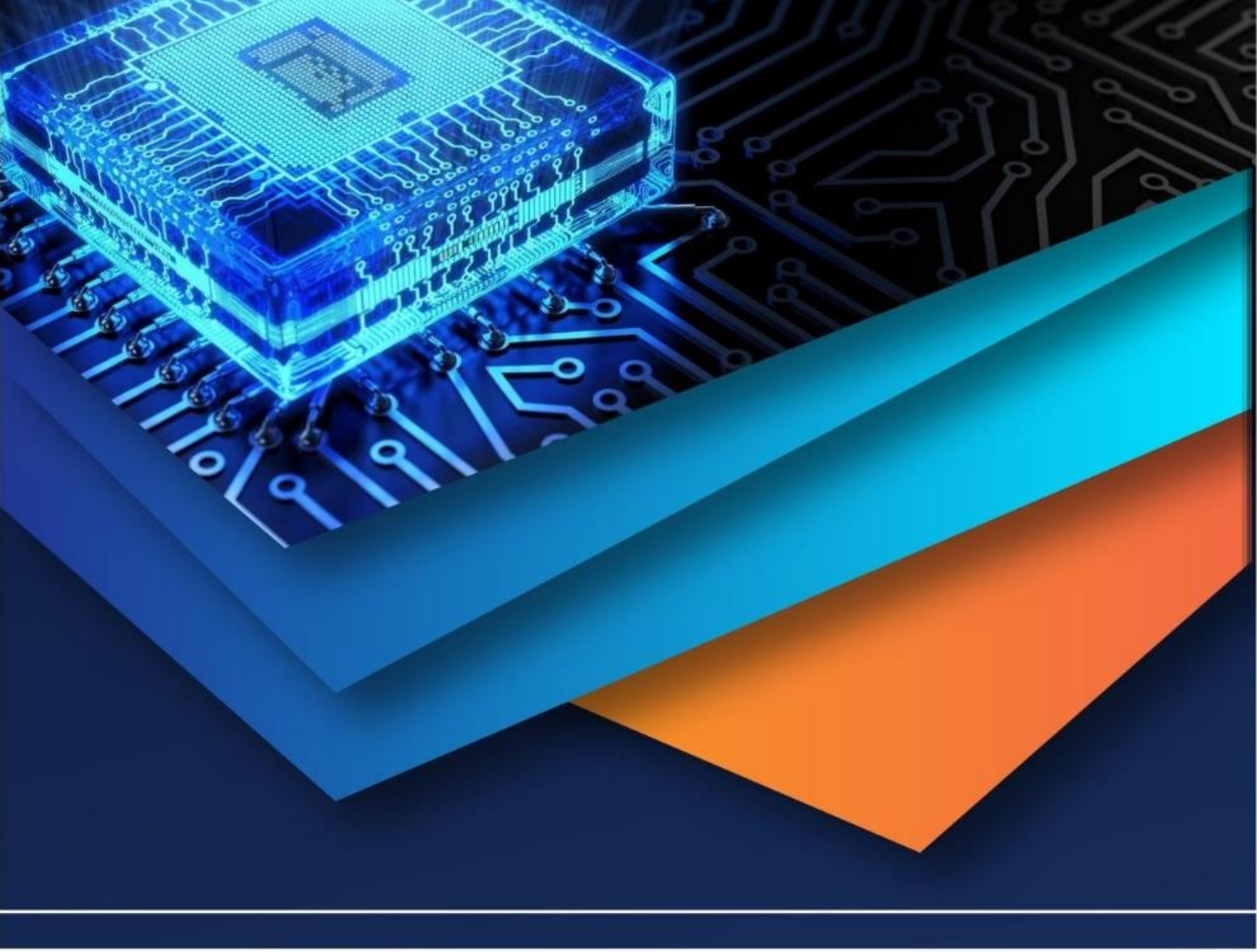

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