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Single Electron Transistor Based IC Architecture Design for Car Intrusion Prevention: A Case Study

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Abstract— Single Electronics, a fascinating technology is a novel alternative of conventional electronics in post CMOS era. This emerging field is rapidly getting attention both in fabrication oriented empirical study and logical modelling; all from the point of view of consumer electronics. Single electronics uses the tunnelling effect of single electron alone to represent binary data values. Another unique character is that it requires much less power than conventional technologies while operating at much higher speed. Several such merits of the single electron transistor made devices have been cited in referred journals. Thus undoubtedly Single Electron Transistor (SET) has the potentiality to usher innumerable applications in modern technological progression. Present day only a few Researchers took the pain to emphasize SET in security systems, although industrial production requires deep research further. Moreover, ample study revealed the art of employing SET in next generation consumable electronics because of its unique decision making capabilities which in turn has now discovered greater impact in extending the boundary of its acceptance to human world. Here in the present work, we have articulated a case study of modelling a SET based on-chip car intrusion prevention IC.

Keywords— Single Electron Transistor, Coulomb Blockade, Tunnelling of Electrons, e-beam Lithography, device modelling

I. INTRODUCTION

Much before the dawn of 21st century Scientists categorically acknowledged the 'More Than Moore' technology to replace FET based large scale integrated circuits. This attributed post CMOS era envisaged the demand of low power consuming nano dimensional device which developed numerous scopes for newer technologies in the field of nanodevice research. Apparently, several nano devices were empirically demonstrated in research labs world wide and got reported in reputed scientific publications [1-6]. Among all other significant conceptions, Quantum Electronics technology, Single Electronics technology and Spintronics technology are mostly accredited because of their higher practicability in today's existing research environment. Device fabrication techniques with its unmatched revolution from old age process to the present day advanced e-beam lithography technique ensured that intensive device scaling down leads to novel nanotechnology innovations without compromising any performance criteria. This has predominantly increased the quest of consumers to integrate higher number of applications in one tiny platform; thereby amplifying the possibility of incorporation of nanotechnology in industrial production.

Fulton and Dolan empirically demonstrated the formation of SET by keeping two layers of aluminium that are evaporated in-situ from two angles through the same suspended mask formed by direct e-beam writing [7]. David Berman et al, in 1997 for the first time used beam energy of 40 keV and a current of 20 pA to produce a beam diameter of 20 nm [8]; it is considered as a major success in

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SET research. Ken Uchida, et al., reported a compact, physical, analytical SET model for real time application of SET circuits in 2000 [9]. The uniqueness lies in the orthodox theory of 'correlated single-electron tunnelling' and the 'steady-state master equation method' that got incorporated in the designed model. Yong Yang et al, in 2005 [10], Qiliang Li, et al, in 2007 [11],

Jun Hyuk Cheon et al. in 2009 [12], reported the formation of high quality SETs at room temperature having greater Coulomb Staircase. Further it was found that from the very inception of Single electron device research, Researchers have been hard pressing the consequences of back ground charge and room temperature operational problem. Besides fabrication oriented experimental device research several simulation oriented research publications caught much attention. C. Wasshuber designed SIMON simulator based on Monte-Carlo technique [13]. But this was not all.

The necessity to design SET based logic circuits with its simulation besides fabrication oriented research show tremendous impact to replace present day CMOS technology in near future. Eminent Researchers have comprehended this importance and thus have now stirred their focus on realizing application oriented SET design. Undoubtedly, it is a much new approach and very few of the Researchers have tried their hands in this sector. Employing SET technology in real life applications is not only thrilling but also a challenging field to explore. Accomplishment of SET logic devices for real time circuit realization is still lagging far behind; even though it is a rising field of low dimensional device structure oriented research that has opened a new horizon for present and future device application. In the present day to deal with the desire of low power consuming high speed nano devices, Researchers now consider that it is a high time to initiate broader research related to application areas of SET such as Logic Gates, Memories and many more [14-18]. Presuming such, here the focus of the authors were much centered on designing low power consuming, portable, nano dimensional new generation extremely efficient SET based car security IC designs that are to be incorporated for mass production.

II. A Brief But Analytical View Of SET Structure

An The device structure of SET is analogous to the FET having three terminals; i.e., the outside terminal of each tunnel junction namely the source and drain, and the "gate" terminal which remains capacitively coupled to the node between the two tunnel junctions. The capacitor operates like a third tunnel junction, however it is much thicker than the others ensuring that no electrons can tunnel through it; the schematic view is shown in Fig1. The capacitor provides the path of setting the electric charge on the Coulomb Island.

This Coulomb Island is one of the most interesting units of the SET structure. Study revealed that the blocking state, also referred as the Coulomb Blockade state holds the accessible energy levels at much higher range than the tunnelling range of the electron on the source contact. All energy levels on the island here are occupied with lower energy electrodes. The customary is to apply positive voltage to the gate electrode; thereby the energy levels of the island electrode are lowered. The three pre-conditions to achieve the Coulomb Blockade are

1. The bias voltage (V_{bias}) is supposed to be lower than the elementary charge (e) divided by the self-capacitance (C) of the island, i.e., $V_{bias}<e/C$.

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2. The thermal energy that lies close to the source contact along with the thermal energy in the island is denoted by k_{BT}; it is required to be lower than the charging energy, i.e., $k_BT < e^2C$.

3. The tunnelling resistance R_t needs to be higher than (h/e^2) (derived from Heisenberg's uncertainty principle).

In conventional methodology it is observed that by neglecting all the effects of thermal and other forms of energy, the only energy source available is the bias voltage V_{bias}. If the said V_{bias} is considerably smaller than the threshold voltage V_{th} which is also identical to e/C (i.e., V_{th}=e/C), then no electron can tunnel in as the available energy as it is not enough to charge the island. This condition is labelled as Coulomb Blockade. With incremented V_{bias}, the electrons will occupy the granule with one, then two and continue in this mode; this marks a stair case like characteristics as shown in Fig. 2 [19,20].

Investigations showed that tunnelling of an electron occurs from one point of a tunnel junction to an opposite point of the tunnel junction, in this manner the charge distribution of that particular circuit changes. The basis of the tunnelling lies in the fact that we require Coulomb Energy E_C to charge an island with an electron where $E_C=e^2/(2C)>K_BT$, considering that C is the overall capacitance of an island and KB is Boltzmann's constant (KB=1.38×10-34 J/K). Now this Coulomb energy is typically greater than the available thermal energy; hence one can manipulate and control the movement of electrons by controlling the available energy supplied by voltage source as shown in Figure. 3.

The next fundamental issue under scanner is how a SET will operate: the solution lies in the structure of the SET itself. The tunnelling occurs in the following way - if an electron comes at point 'A' and if the pulse Φn-1>5mV is applied then the electron crosses the tunnel junctions (J1 and J3) to C or E as shown in Fig. 4. It consistently depends on whether the Coulomb energy $[E_c=e^2/(2C)]$ along with the applied energy is greater than the potential height of the barrier energy of junction(s) J1or J3. Based on this, the electron follows the path ABCD or ABEF following the pre condition that the signal X_i>5mV and the corresponding total energy i.e., Coulomb energy plus the applied energy is greater than static potential junction energy of J2 or J4. This path ABCD or ABEF is denoted profoundly to be '1'-branch or '0'-branch. Several Tunnel Junctions made Digital Logic Circuits are designed using the same tunnelling phenomena. Some SET based logic circuit synthesis is detailed below in Fig 5, 6 and 7, different SET based models based on this logical realizations have been reported in reputed journals [21-24]. The same SET logic circuits have been incorporated to design the car intrusion prevention IC in the subsequent section.

III. IC Design Of SET Based Car Intrusion Prevention

The architecture of SET based on chip logic IC circuit for car intrusion prevention is modelled in Fig.8. For simplification the circuit is parted in five segments. Simple motion sensors are fitted into the window pane. The motion sensors when activated passes signal to the corresponding nodes defined as V_{gA}, V_{gB}, V_{gC} and V_{gD}. We definitely argue that if the motion sensors can be built on the basis of nanosensor technology, the oriented circuit will be much more robust and competent. The critical issues like room temperature operation or background charge of the circuit require extensive study to make it ready for industrial production.

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The modus operandi of this circuit is quite fascinating as the logic behind its operation is very simple but effective and has less propagation delay. An alarm is connected in the rear end of the circuit of Fig.8, although such alarm connection could not be included in this work due to space limitation. Eventually the alarm is set ON only if the window of the car is broken or if it senses something moving inside the car but the car is not being towed or the engine is still not on. Ensuing to these conditions we have designed the SET based circuit providing output voltage Vout = $(V_{gB}+V_{gD}).(V_{gA'}+V_{gC'})$ to the alarm to set it ON. The tunnelling of electrons is originated when any of the above conditions become true. Then the Coulomb energy increases which provides the means to tunnel the electrons from V_{gA} to V_{g1} and similarly in other parts of the circuit. The V_{dd} in all the parts of the circuit are of same value to maintain uniformity of the simple structure. The contact areas are made short so as to increase the integration level of the circuit. The detailing of the circuit ponders over the issues like power dissipation, propagation delay, fastness and power consumption.

IV. Merits Of The proposed Modelling Of SET Based Car Intrusion Prevention IC

The modelling of SET based car intrusion prevention IC was largely tested on Monte Carlo based simulation settings for its maximum exploitation. The proposed modelling of this SET based system considerably reduces power consumption but is efficient enough to provide result at a quicker speed. Accordingly, a very high-speed computation is indeed attained with this newly proposed SET configuration. The power dissipation for switching a single bit as shown in the table below is of few µW which is extensively lesser when compared to conventional CMOS devices. With such ample distinguishing merits the SET designed circuit shows tremendous prospect of providing much more component density thereby reducing the future IC sizes. Besides, all other phenomenal individuality of SET circuit the model reflects its robustness than any conventional CMOS based circuit.

TABLE I
Comparison Of SET & CMOS Performance

Sl. No	Circuit Name	Propagation Delay time / Gate	Faster times	Power dissipation / Gate	Consume Power
1	CMOS	12 ns	1	0.01 / 10-12 mW	1
2	SET	6 ns	2	~1µW	$1/10^3$

V. Conclusions

The Single Electron technology is built on the robust effects of the electronic charge discreteness. Its unmatched importance is also increased with size reduction. In this modeling single charge is efficiently incorporated to manipulate and control the correlated electron tunneling in small capacitance structure. Modern era that demands superiority in consumer electronics can be achieved only if advantageous power consumption technique can be adopted and if the size can be absolutely reduced for easy portability like considerations. In this scenario SET technology stands much ahead. Further the logical operations create greater prospect in future SET based Logic Circuits. Sophisticated mankind show a positive response in adopting several decision-making technologies and thus this quest has moved the Scientists and Researchers to devote themselves in hardware implementation of such technologies.

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VI. List Of Figures

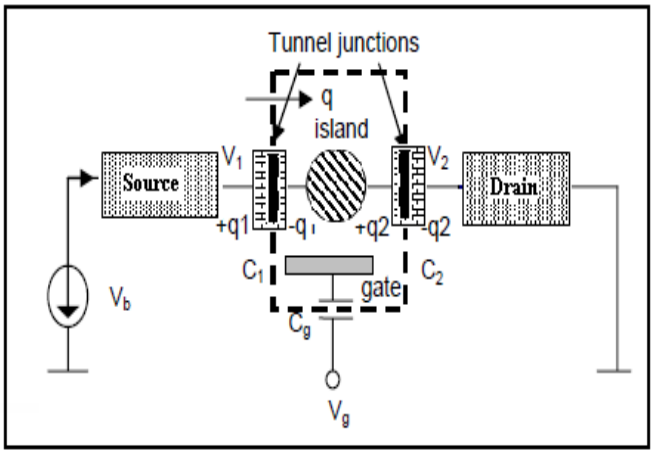

Fig. 1 Schematic view of SET

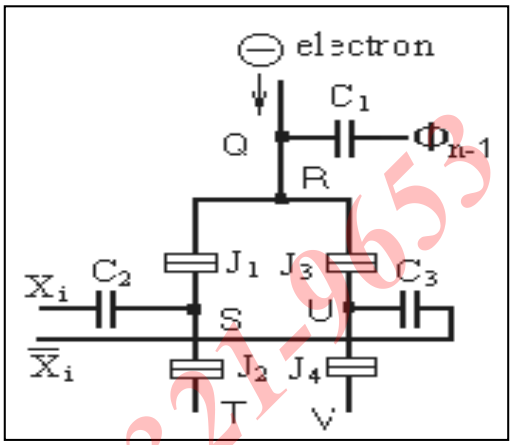

Fig. 4 SET electron flow path

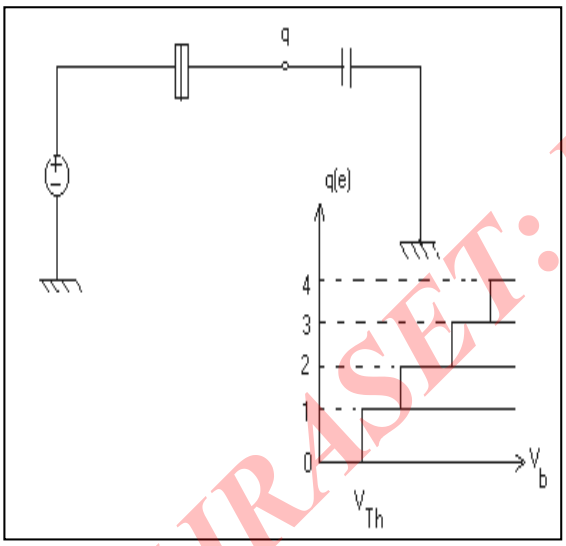

Fig. 2 Coulomb Staircase Structure

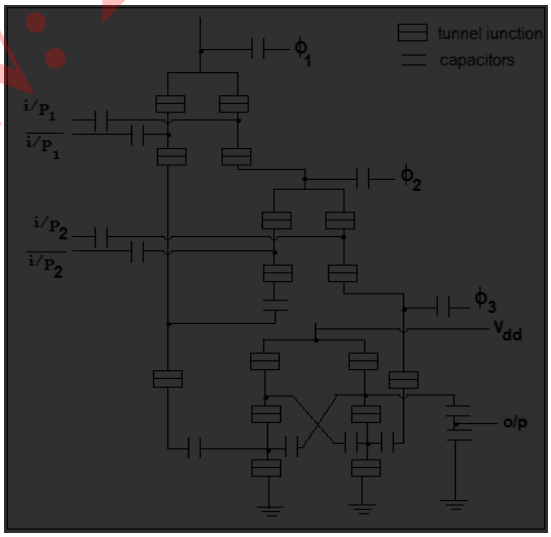

Fig. 5 SET based AND Gate Representation

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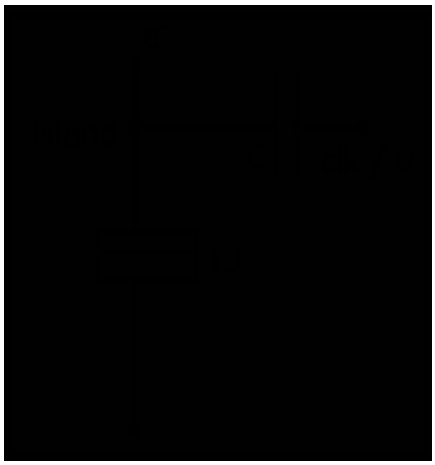

Fig. 3 SET Tunnelling Phenomena

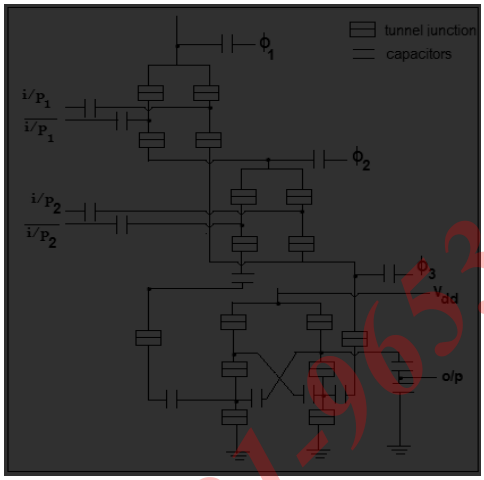

Fig. 6 SET based OR Gate Representation

Fig. 7 SET based NOT Gate Representation

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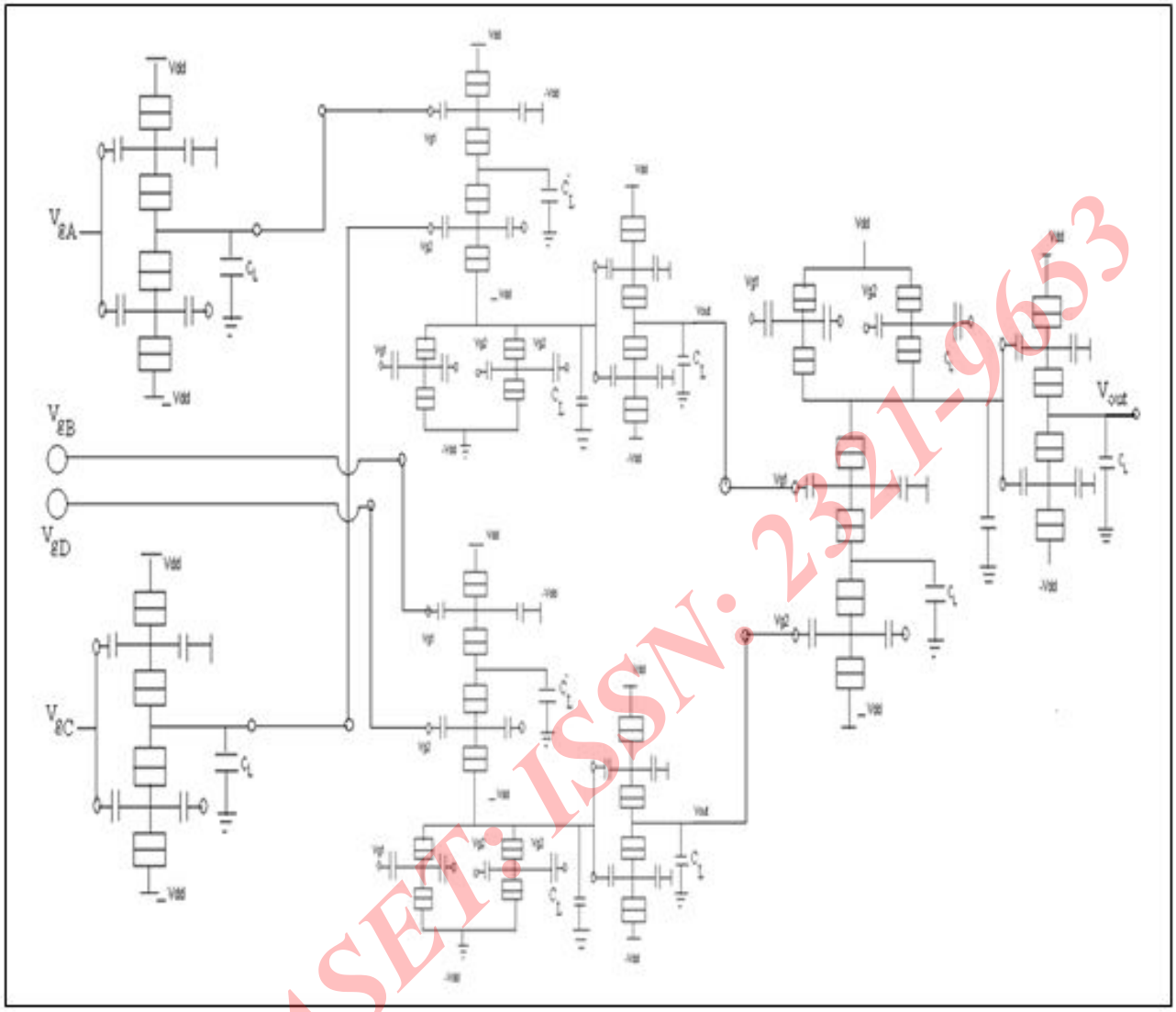

Fig. 8 Internal Structure of SET based IC for Car Intrusion Detection and Prevention