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A Review of Efficient Low Power High Speed Flash ADC Design Techniques

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Abstract— Analog to digital converter is the important component in signal processing and communication system. It is a mixed system which converts the analog signals into the digital signals for transformation of sensor data. There are many types of ADC's available such as pipeline ADC, successive approximation ADC, delta sigma ADC etc. In present day CMOS technology the flash ADC is composed by utilising the dynamic method, it reduces the power, and delay. A flash ADC is extremely valuable for fastest speed operations when it is compared with the other ADC architectures. Comparator and Encoder are vital part of flash ADC. This paper presents review of Efficient Low Power High Speed Flash ADC Techniques.
Keywords—ADC, Flash ADC, Resolution, Conversion rate, Comparator, Conversion speed, Encoder.

I. INTRODUCTION

The signals in the real world are analog in nature for example light, sound, video etc. In order to achieve digital signal, analog signal has to be converted into digital form by using a circuit called analog to digital converter. Whenever analog signal is needed back, digital to analog converter is required. Analog to digital converters are important block in many modern systems that require the integration of analog signals with digital systems.

II. FLASH ADC

The flash ADC is known for its fastest speed of operation compared to other ADC architectures. So it is used for high speed and very large bandwidth applications such as radar processing, optical communication links, digital oscilloscopes, high-density disk drives and so on. The flash ADC is also called as the parallel ADC because of its parallel architecture.

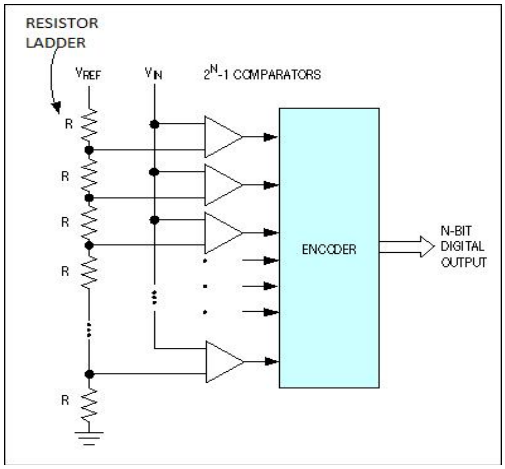

Fig. 1 Flash ADC.

Figure 1 shows Flash ADC architecture. It can be seen from the figure, that 2^N - 1 comparators are required for "N" bit flash converter. The resistor ladder network is formed by 2^N resistors, which is used to generates the +reference voltages for each of the comparators. Reference voltage for each and every comparator is 1 least significant bit which is less than the reference voltage for the comparator instantly above it. When the input voltage is above the reference voltage of comparator it will generate a "1" otherwise, the comparator output is "0". The comparators will generate a thermometer code of an input signal. This code is known as thermometer code because it is similar as mercury thermometer, where in the mercury column,
the mercury rises to the suitable temperature and no mercury is above that temperature. This thermometer code will be then encoded into a binary form by thermometer to binary encoder [11].

III. LITERATURE REVIEW

This paper gives survey on various techniques of Flash ADC design. Researchers have implemented flash ADC with different number of bits and different CMOS technologies.

Steven B. Kaplan et.al [1] proposed a complete transient digitizer system consisting of a superconductive flash ADC, on chip acquisition hardware, a room temperature interface and HYPRESS to digitally reconstruct the input signal. Transient digitizer with a near term performance of at least 6 effective bits at 10 GHz and 8 effective bits at 2.5GHz are obtained. The wide bandwidth of the digitizer front end has been demonstrated in beat-frequency tests up to 30 GHz.

Yun-Ti Wang et.al. [2] proposed an 8-Bit 150-MHz CMOS ADC with 0.6µm CMOS technology with 8 bits Resolution. An 8-bit 150-MHz CMOS ADC has been described that incorporates sliding interpolation, distributed sampling, interleaving, clock edge reassignment, and punctured interpolation.

Siamak Mortezapour et.al. [3] proposed a 1-V, 8-Bit Successive Approximation ADC. The ADC consumes less than 0.34mW and has an ENOB of 7.9 for a 1-kHz input with close to rail-to-rail signal swing. This design demonstrates that low-voltage ADC with medium accuracy can be realized without requiring special enhancements to CMOS technology.

Conor Donovan et.al. [4] proposed a 6-bit prototype converter built in a standard 0.25µm digital CMOS process which dissipates 150mW from a 2.2-V supply at 400 MS/s. It occupies 1.2 mm^2 and describe a digital technique that can removes the accuracy constraints from the comparators.

Christoph Sandner et.al. [5] proposed a 6 bit flash ADC, large analog bandwidth and low power in 0.13 µm CMOS copper technology with 1.2GSps. This ADC attains to an effective resolution bandwidth (ERBW) of 700 MHz when working at 1.2 GSps requires 160mW power and at 600 MSps accomplishes an ERBW of 600MHz with just 90mW power consumption from 1.5V supply. The chip area is 0.12mm^2 and requirement for reference resistor step, implicit sample and hold operation, no edge impacts in the interpolation network when contrasted with resistive addition and input capacitance is low of just 400fF and because of that safely drivable analog converter can be interface. This configuration demonstrates the efficiency of the capacitive interpolation construction modelling with distributed sample and hold for flash ADC in GHz range.

Sunghyun Park et.al. [6] proposed 4-GS/s 4-bit Flash ADC in 0.18-um CMOS. It achieves a measured DNL and INL of less than one quarter LSB at 4 GS/s. The measured ENOB is 3.89 bits at 4 GS/s with a 10 MHz input, and 3.47 bits at 3.4 GS/s with an 800 MHz input.

Mingzhen Wang et.al. [7] proposed a 4 bit flash ADC with high spurious free dynamic for high data transmission correspondences using 130nm CMOS technology. They proposed timed digital comparator with dynamic offset concealment to enhance the ADC dynamic performance. This flash ADC has two and half clock cycle latency. It has low input capacitance of 300fF. The power consumption is 1.35mW with 1.2V supply. It has 2.5GHz conversion rate using a multi-stage pipelined design. This flash ADC enhances high sampling rate, low power, low input capacitance and there is no need of any reference resistor stage.

M. Maruyama et.al [8] proposed a design of a superconductive flash ADC with a complementary configuration. A 4 bit A/D converter function in gray code are confirmed at low frequencies for both the QOS circuits with the ordinary comparators and with the dc-SQUID-type comparator.

Prof. S.S. Khot et.al. [9] introduced the design of 4-bit ADC. Threshold Inverter Quantization (TIQ) comparator is used with the input frequency of 1GHz and is designed using standard CMOS technology. The power consumption of ADC is less than 145µW. The DNL is observed as less than 0.5 LSB and INL is less than 0.7 LSB. The ADC design is simulated in Microwind 3.1.

H. Suzuki et.al. [10] proposed a 5-bit flash-type SFQ ADC's, which had used CQOS comparators integrated with error correction and bit-interleaving circuits.

Bui Van Hieu et.al. [11] proposed new approach which coordinates a bubble error identification circuits and it can declined all types of bubble error when contrasted with the past methodologies and the main advantage is that it consumes low power. This method has great structure, very high speed and little chip area when contrasted with different structure. With the help of this ROM based technique it can reduce the latency and power dissipation and can rectify both first and second order bubble error. This system just distinguishes all bubble errors as opposed to attempting to rectify bubble error, which still can't cover all errors. At whatever point bubble error happen, there is at least one violent move from 0 to 1 in the thermometer input code. By identifying the violent move bubble error can be uncovered. One two input AND gate distinguishes violent move of every input and afterward all outputs of AND gates are gathered to recognizes bubble errors.

Pradeep Kumar et.al. [12] introduced 3 bit flash ADC using 0.18 um technology with 1.3V power supply. This paper was proposed and clarified how the flash ADC is quick contrasted with other ADC. So it required as a part of uses where the latency is paramount and the hardware multifaceted nature is unassuming. The one limitation of the ADC converter is the exactness on

account of easiness of the circuits. For high resolutions the flash ADC's are very costly as a result of complexity is exponentially increments with the quantity of bit increments. The normal power consumption was 36.273mW.

Panchal S. D et.al. [13] proposed a 4-bit flash ADC in 180nm technology with 2.5V power Supply. In this paper pipelined flash Analog to Digital Converter (ADC) is designed to achieve high speed using 0.18um CMOS technology. ADC is designed using folding technique in cadence tool.

Arunkumar P. Chavan, et.al [14] proposed design and pre-simulation of a 3 bit and a 4 bit ADC for low power CMOS. The design operates with an input frequency of 25MHz with 1.5V supply. A conversion time for 3-bit is 2.162ns and 4-bit is 6.182 ns is obtained. The design and Pre-simulation are carried out in cadence tool under 90nm technology.

Mamta Gurjar et.al. [15] proposed implementation of TIQ based comparator that exhibits low power consumption compared to other types of comparator based design. A Speed of 15.3 Gs/s is observed for 3 bit ADC that has been simulated by cadence tool at 45 nm technology. TIQ based ADC provides the lower bandwidth of 16.65MHz and low SFDR 1.57dB.

H. Suzuki et.al. [16] proposed a 5-bit A/D converter by means including increasing the current density of the junction, reducing the size of the CQOS comparator and adopting the structure of locally isolated ground (LIG).

Amol Inamdar et al. [17] proposed different flavours of Flash comparators. One flavour uses differential quasi one junction SQUID quantizer with low inductance clocking scheme. The second flavour uses a differential SQUID wheel quantizer, and the third flavour uses a symmetric differential SQUID wheel quantizer with time interleaved clocks. Three flavors of the Flash comparator are designed to reduce its phase dependent nonlinearities by reducing the βL of the comparator. The powerful sampling scope reconstruction technique are also developed that enables to quantify the comparator SNR, duty cycle distortion, and sensitivity to duty DC bias using a single bit comparator..

Dheepak Mohanraj [19] proposed design of a High speed ADC system. The system described 8-bit ADC designed in a 0.25µm CMOS technology and simulated in Win Spice. ADC can sample at 1.7875 MHz and the total sampling speed of ADC is becomes 14.3 Ms/s.

Gulrej Ahmed et.al. [20] proposed a 6 bit flash analog to digital converter using variable switching voltage CMOS Comparator with 65nm standard CMOS technology. The measured maximum differential and integral non-linearity (DNL and INL) for a ramp input are found to be 0.3 LSB 0.6 LSB respectively. This designed exhibits significant improvement in terms of power and speed.

Parthasarthy K.P.et.al. [21] introduced the usage of the low power consumption flash ADC for very high end receivers. The demanding issue in this paper was to design a low power latched comparator using 90nm technology with 0.8V DC supply. This technique consumes low power of 7.67mW, which consumes a low power of around half for a sampling frequency up to 1.2GHz. This configuration can be extended to high speed applications because comparator utilized as a part of this plan can work up to 5GS/s.

Xiaochen Yang et.al. [22] proposed a flash ADC architecture to achieve a better power Efficiency. Partially active flash ADC is designed with improved power efficiency in the 10 GS/s speed range. 6 bit four-way time-interleaved ADC prototype in 65 nm CMOS demonstrated. This ADC architecture offers better power efficiency than other ADC architectures in the 10 GS/s speed range.

S. S. KHOT [23] proposed a 6-BIT CMOS flash ADC. In this paper, a comparison of 6-bit flash ADC exercising TIQ comparator is manifested at 2.5 V and 3.3 V. A CMOS Flash ADC was schemed with 0.250 µm CMOS technology. Cascaded CMOS inverters is used as a comparator, fat tree encoder has been used to designed ADC.

TABLE I
LITERATURE REVIEW

Author	Architecture	Resolution	Input voltage	Technology	Improved Parameters
Mamta Gurjar et.al [15]	3 bit flash ADC	3 bit	0 V to 0.7 V	45 nm COMS	Speed-5.3 Gs/s Bandwidth-16.65 MHz
Mingzhen Wang et.al [7]	4 bit flash ADC	4 bit	1.2 V	130 nm CMOS	Power consumption- 1.35 m Conversion rate- 2.5GHz
Pradeep Kumar et.al [12]	3 bit flash ADC	3 bit	1.3 V	0.18um CMOS	Power consumption- 36.273mw
Parthasarathy K. P. et.al [21]	6 bit flash ADC	6 bit	0.8 V	90nm CMOS	Power dissipation- 7.67mW.
Gulrej Ahmed et.al [20]	6 bit flash ADC	6 bit	1.2 V	65nm CMOS	Speed-1 GHz

Conor Donovan et.al [4]	6 bit flash ADC	6 bit	2.2 V	0.25um CMOS	Power dissipation- 150 mW
Prof. S.S. Khot et.al [9]	4 bit flash ADC	4 bit	0.7V	45nm CMOS	Power consumption- 145µW
Panchal S. D. et.al [13]	4 bit flash ADC	4 bit	2.5 V	0.18um CMOS	Gain- 72.5 dB at 150Hz 14.1 dB at 100MHz Bandwidth-2.511E6 Hz
S. S. Khot [23]	6 bit flash ADC	6 bit	2.5 V and 3.3 V	0.25 µm CMOS	Speed- 500- 565msps
Sunghyun Park et.al [6]	4 bit flash ADC	4 bit	1.8 V	0.18 µm CMOS	Power consumption- 78 mW

IV. CONCLUSIONS

In this paper different methods of designing flash ADC are examined. Comparator and encoder is vital part of designing Flash ADC. Different methods of designing Flash converter by various authors are compared for performance parameters like power consumption, conversion speed, gain, bandwidth, accuracy, and different technologies employed for obtaining better results.

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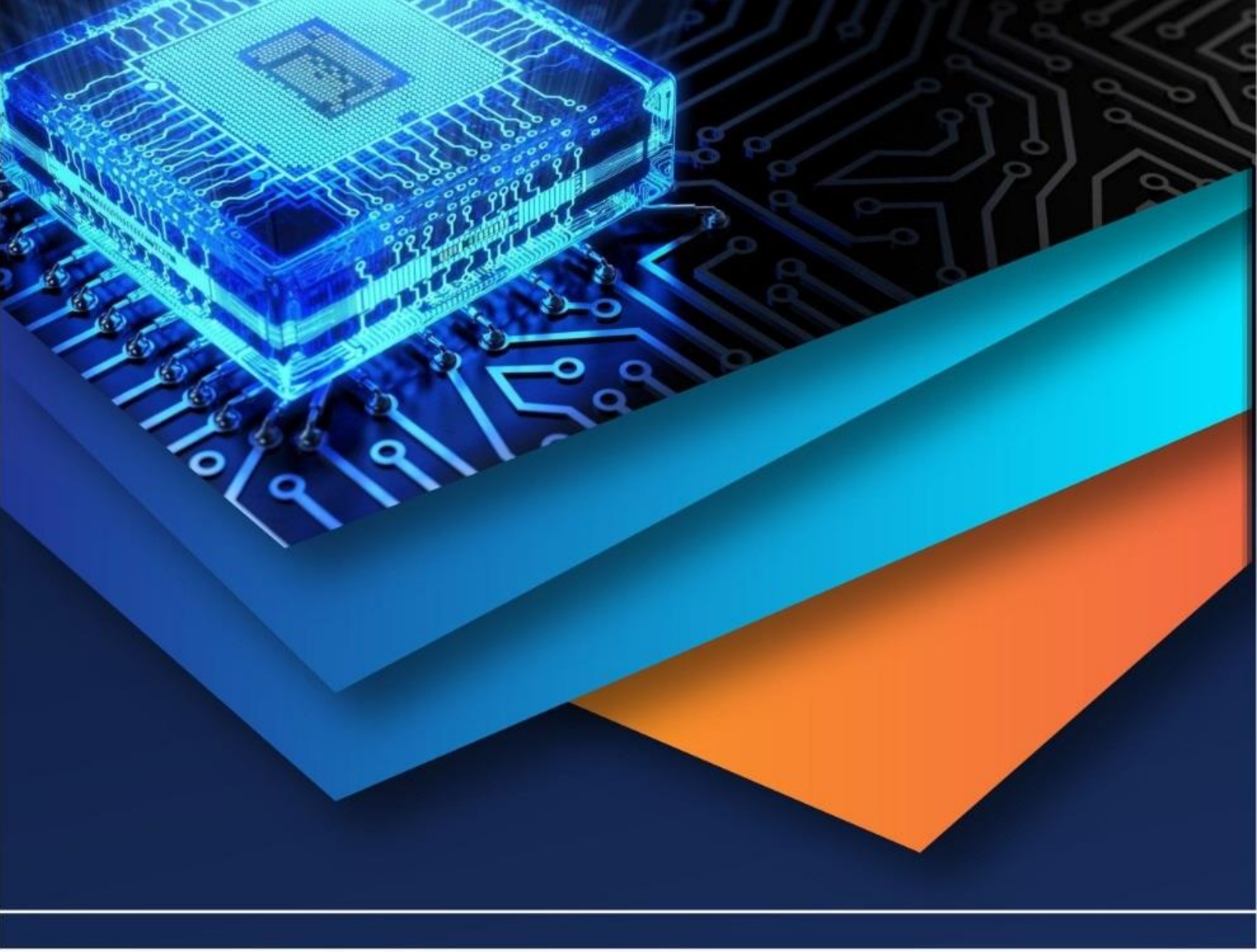

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