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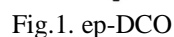
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**Keywords:** *Flip flop, low power, Conditional discharge, Pulse triggered.*

Flip flop design are basic storage elements used in all types of digital design. Flip flop design and performance has a effect in reducing the power dissipation and in high performance system. Microprocessors basically uses master slave and pulse triggered flip flop. Master slave are made up of two stages, one master and one slave characterized by their hard-edge property. Pulse triggered reduces two stages into one and are characterized by soft-edge property. Pulse triggered is more popular than master slave because of its single latch structure and high speed operation. The main advantage of pulse triggered is that it allows time borrowing across cycle a boundary which leads to high performance. A Pulse triggered flip flop consists of pulse generator and a latch. Pulse triggered flip flop can be static, or semi-static, or dynamic, or semi dynamic. Pulse triggered flip flop can also be classified into single-edge triggered clocked flip flop and double edge triggered clocked flip flop.

To provide a comparison few existing design are discussed here. Fig. show a classic explicit data close to output(ep-DCO). In this the FF, three inverters are used to determine the pulse width. The drawback of this design is that internal node X discharge on every rising edge of clock in spite of static input 1.



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simplified and consists of an inverter and a pull up pMOS transistor.

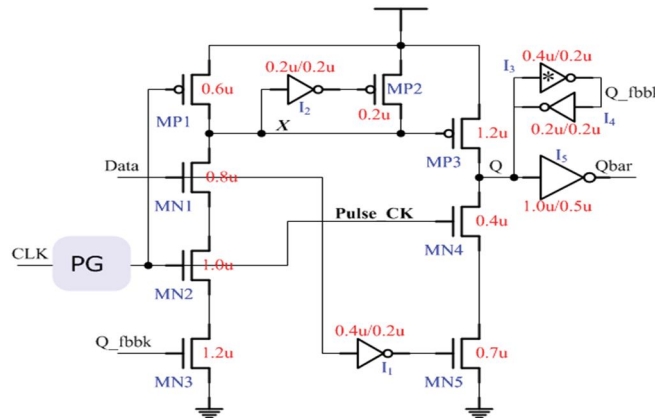


Fig. 2. CDFF

Similar to CDFF, static CDFF, fig (c), is proposed. The difference is in latching structure. Here node X is exempted from periodical precharge. It also exhibit longer D to Q delay as compare to CDFF. Both the design face a worst case delay because of three stacked transistor in the discharging path.

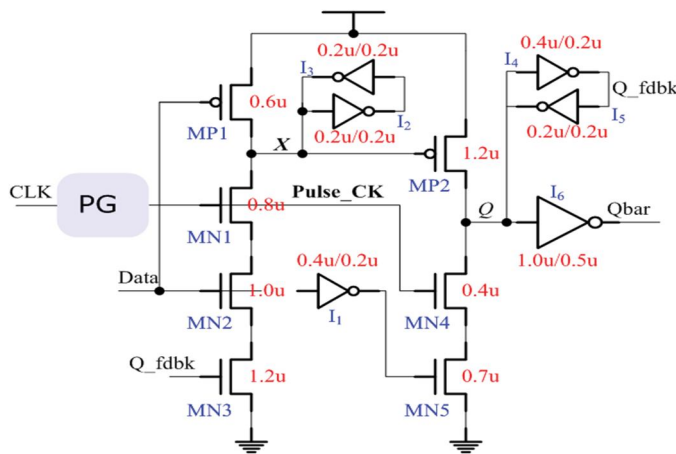
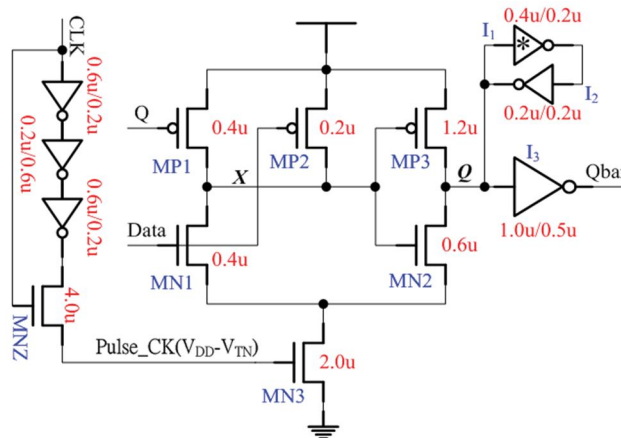


Fig. 3. Static-CDFF

To overcome this delay MHLFF, fig (d) is introduced. MHLFF also uses static latch. The keeper logic at X is removed. But the drawback with this is that X floating in certain cases and its value may drift causing extra dc power.



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### III. COMPARISON TABLE AND SIMULATED RESULTS

The simulation results for all the flip flop were obtained in a 90nm CMOS technology at room temperature using Tanner Tool 13, the supply voltage is 1.8V. A clock frequency of 250MHz is used for single-edge triggered flip flops, whereas double-edge triggered flip flops uses a a frequency of 125MHz. Comparison table shows the simulation results of various flip flops. In view of power consumption and PDP, CDFF has least value as compare to other flip flop.

TABLE I

Flip Flop	No. of Transistor	Propagation Delay of Q (n)	Propagation Delay of QBAR (n)	Power Consumption (f)	PDP of Q (n*f)	PDP of (n*f)QBAR
Ep-DCO	28	22.516	13.5259	31.1	699.75	420.47
CDFF	30	22.511	13.5141	12.37	278.46	167.16
Static-CDFF	31	22.512	13.51	13.79	308.414	185.08
MHLFF	19	22.50	25.47	49.8	1120.50	1268.4

FEATURE COMPARISON OF VARIOUS FF DESIGN

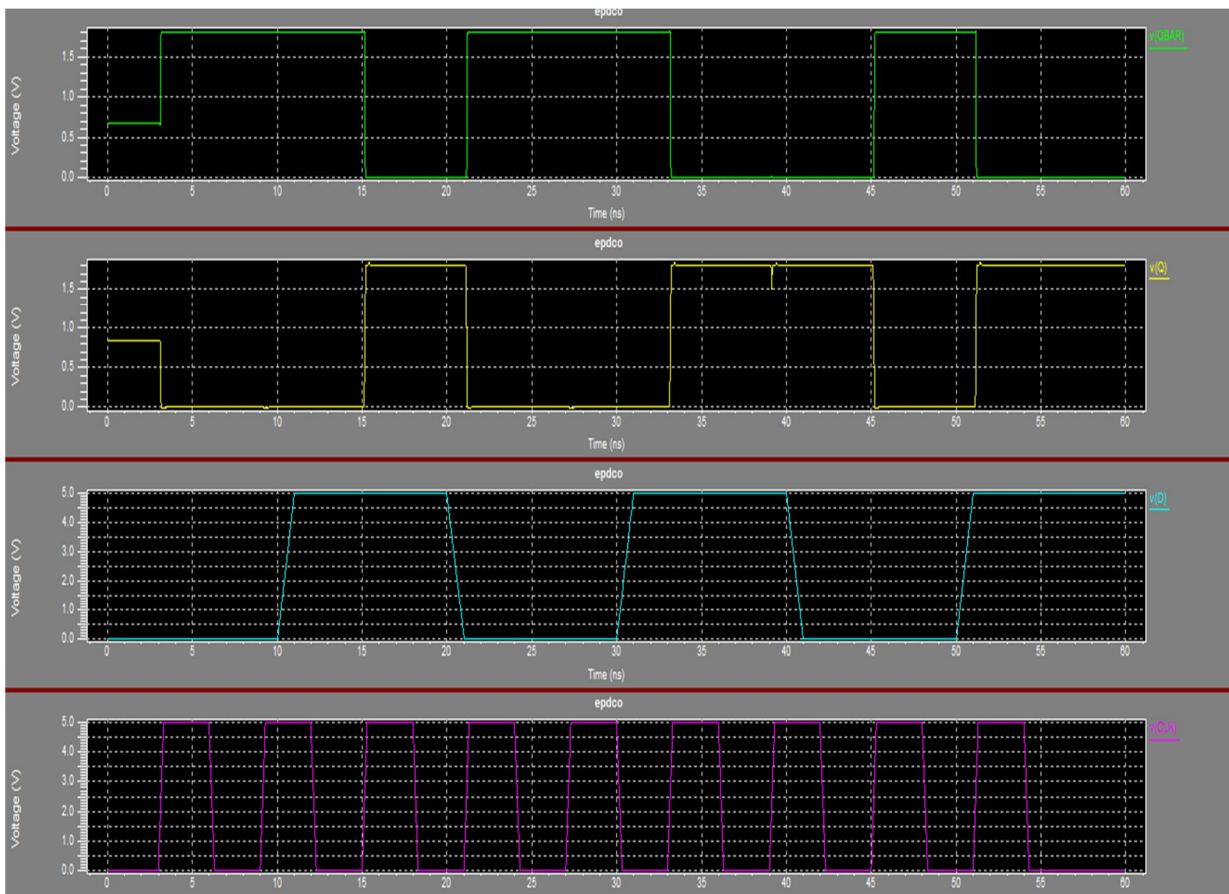


Fig.5. Waveform of ep-DCO



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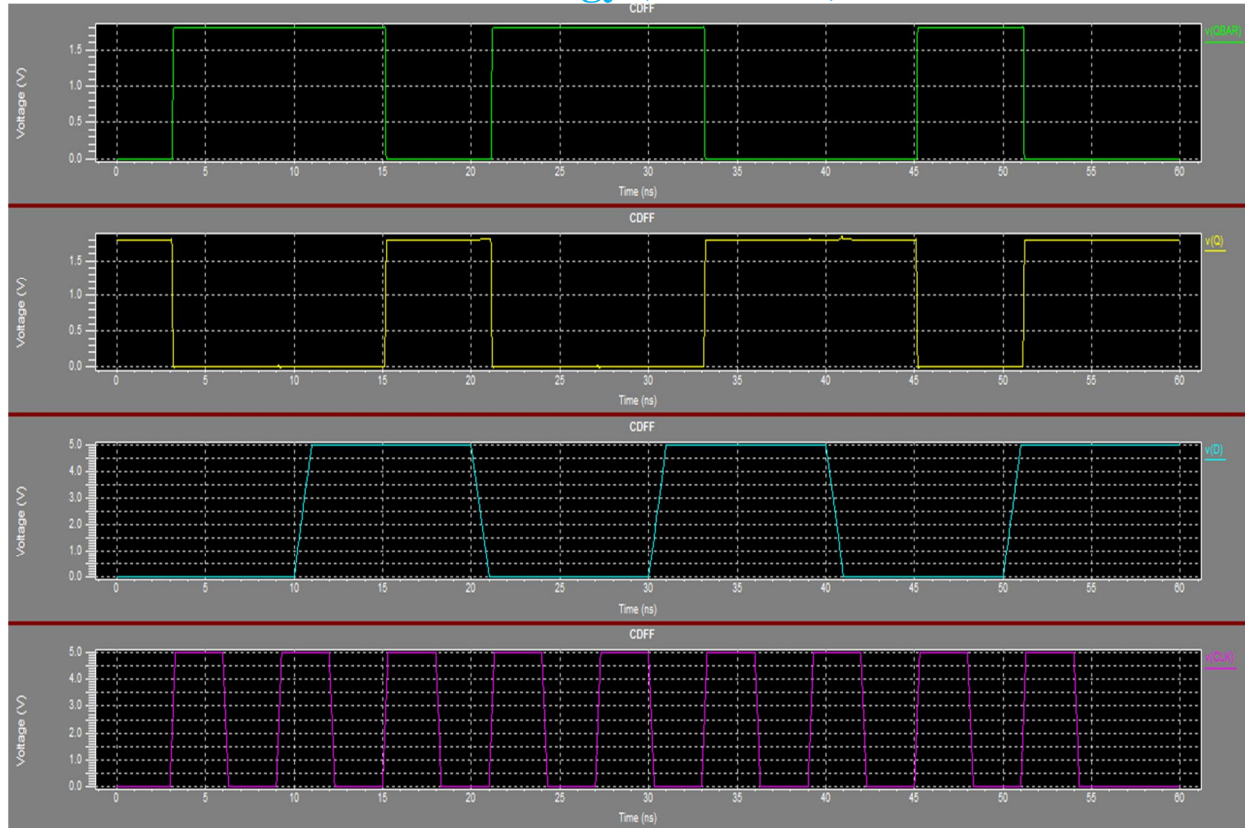


Fig.6 Waveform of CDFF.

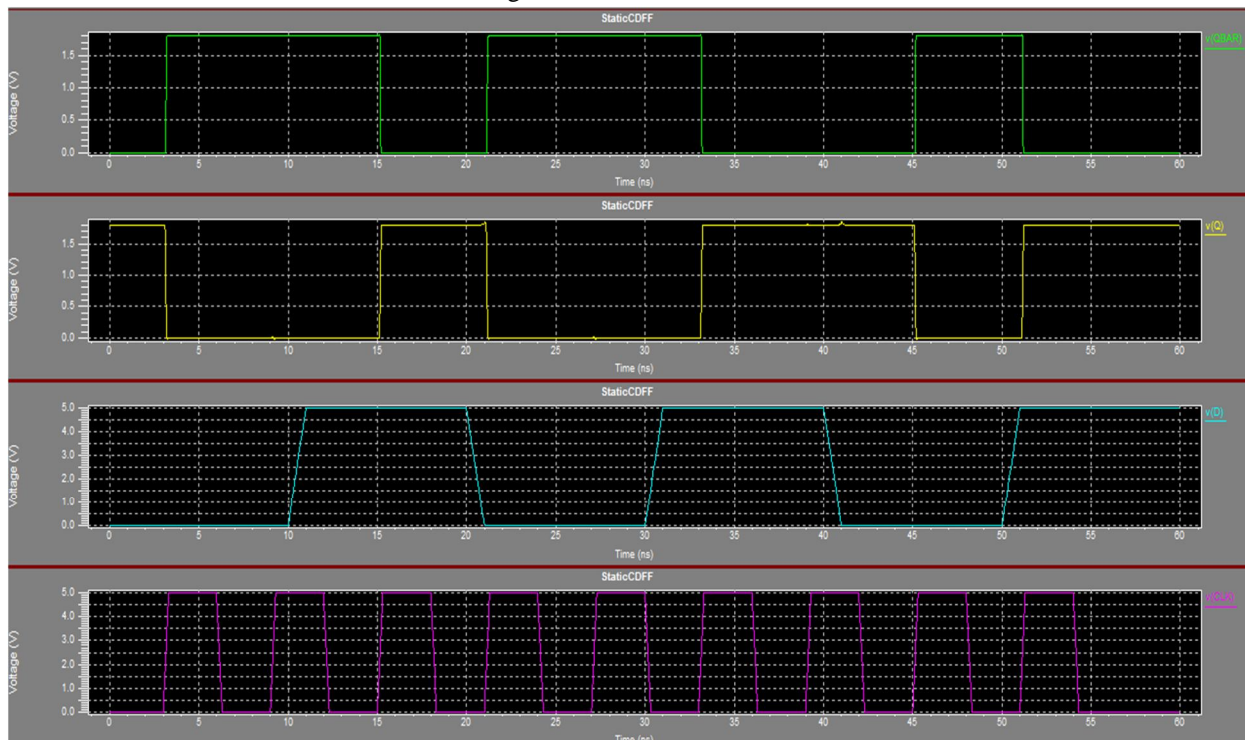


Fig.7. Waveform of Static-CDFF.

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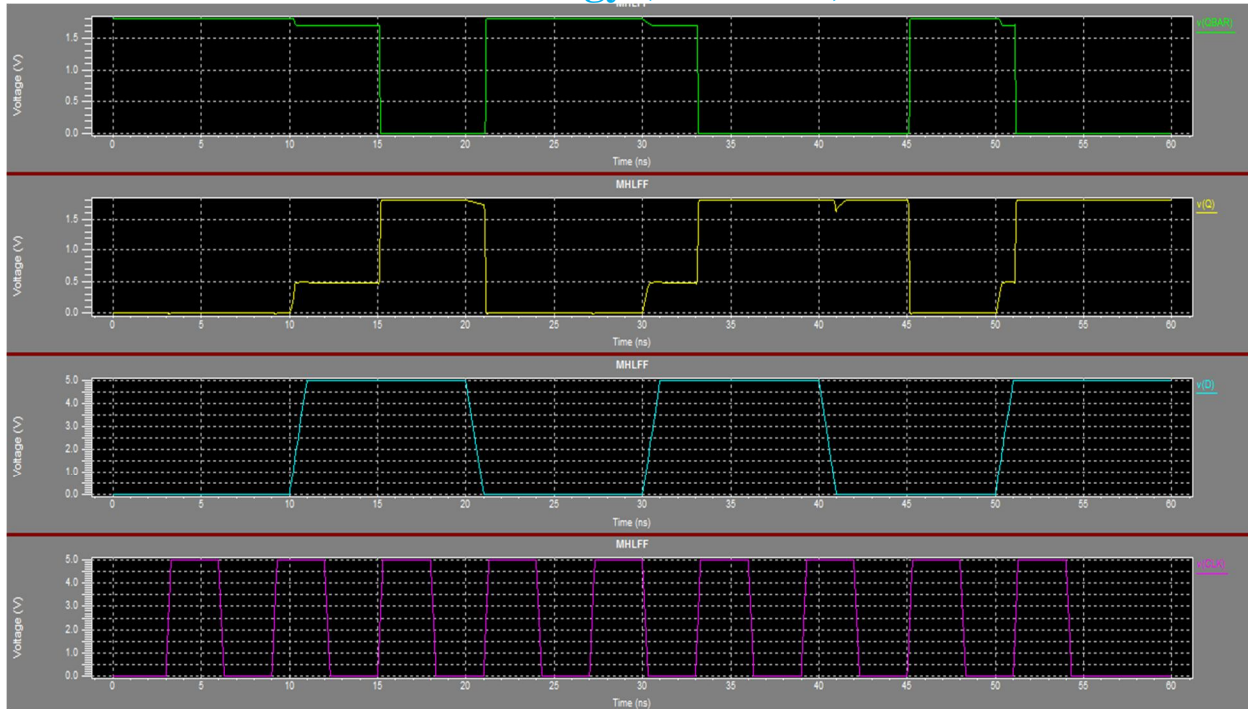


Fig.8. Waveform of MHLFF.

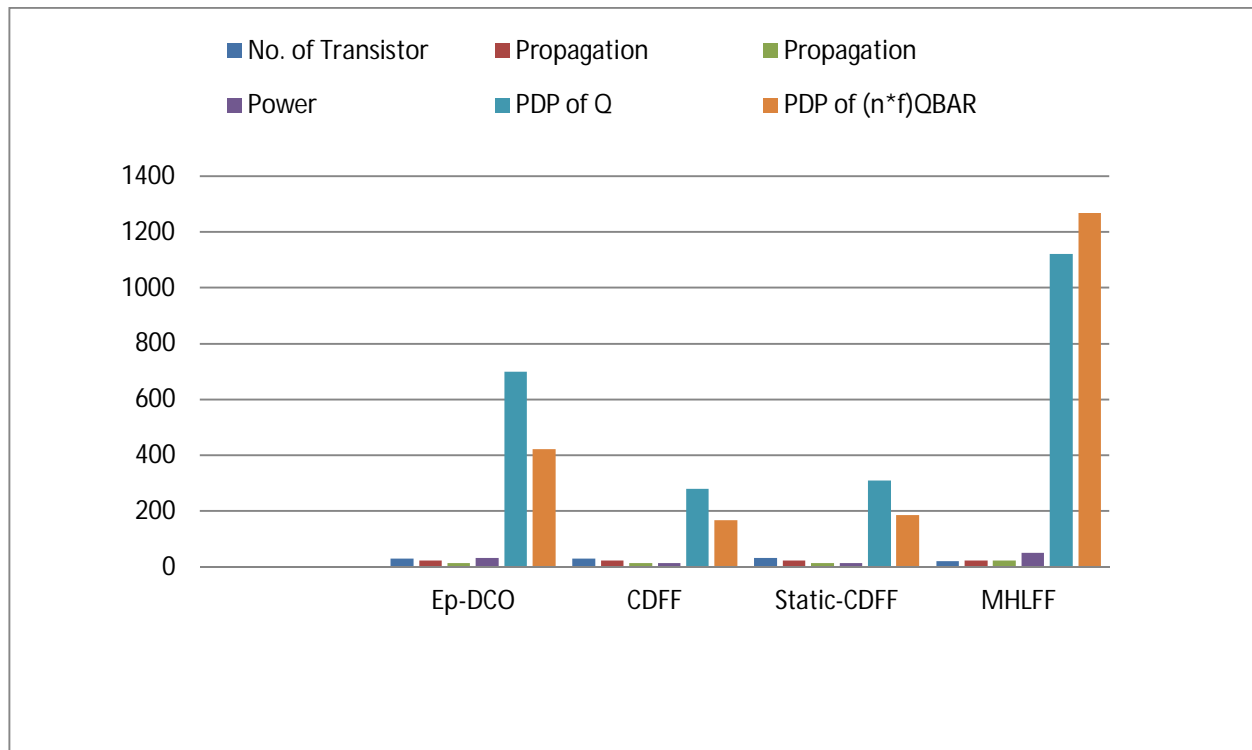


Fig.8. Comparison of different characteristics Flip-Flop.

### IV. CONCLUSION

In this paper, four flip flops are studied and compared. Both single edge and dual edge clocked flip flop are discussed. Dual edge triggered clocked flip flop consumed less power. Delay, number of transistor, average power consumed and power delay product of different flip flops designs is compared. The quality and performance of a CMOS process and gate design is measured in terms of

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power-delay product. The power-delay product can be interpreted as the average energy required for a gate to switch its output from low to high and from high to low. The simulation is performed in 90nm technology CMOS technology, using power supply of 1.8V and clock frequency of 250MHz.

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