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Design and Simulation of Three StagespHEMT LNA At C-Band

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Abstract—Thispaper represents the designing of three stage LNA using EC2612 pHEMT technology.pHEMT technology gives high transconductance and shows better reliability. This three stage amplifier has been designed for C-band applications. The GaAlAs LNA is suitable for transceiver front end due to the low input output VSWR, high stability and redundancy. The LNA is designed at 5 GHz using lumped parameters and over RT duroid (ε_r= 2.2). This structure is simulatedusing ADS software. The simulated result shows the minimum noise figure of 0.3dB and a maximum gain of 33dB.

IndexTerms—LNA,pHEMT technology.

I. INTRODUCTION

Nowadays, LNA is the key component in any front end receiver system. As the progress of front end receiver, the data rate has been speed up in several high frequency applications such as wireless communication, satellite communication, radar systems and smart antennas. These systems require low noise performance to deliver high speed data.At high frequency thecircuit deviates from their actual behavior and are difficult to implement. Many researchers presented several LNA systems with operating frequency at S to X band [1] with wide band frequency characteristics.

In recent years, several LNA‘s designs have been reported using pHEMT, MESFET and HBT technology using package type transistors. pHEMT technology is preferred in LNA front end receivers due to low noise, high gain, high transconductance and highreliability. This paper demonstrated LNA system using chip type transistors. The 3 stage LNA is designed using pHEMT technology which has 33dB of gain and 0.3dB of noise figure. Here source series inductor is used for better stability and tuning is done to improve gain flatness.

The objective of this design is to obtain the low noise, high gain, good input/ output return loss, high reliability and miniaturization of the circuit. This design has several applications in commercial and defense systems.

II. CIRCUIT DESIGN

LNA is one of the most important building block of communication receiver system. The most important design considerations are stability and noise. So, here main function is to provide enough gain to overcome the noise of subsequent stages while adding as little noise as possible. Fig 1[2] depicts thegeneral block diagram of three stage LNA. The figure shows the RF source and RF output along with the matching circuit.Here, interstate matching used to connect the cascading of two or more transistor.

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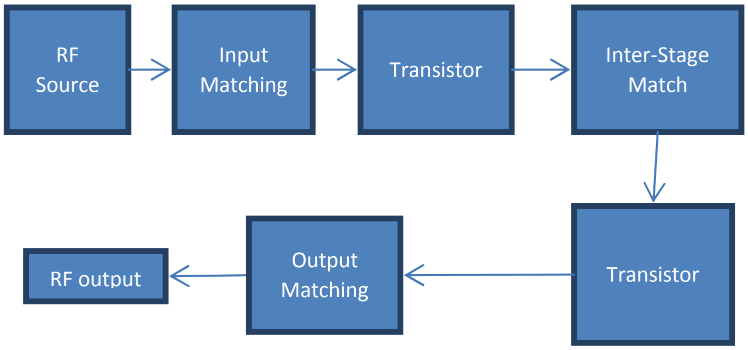

Fig.1 : General block diagram of three stage LNA.

The 3 stage cascaded LNA operating with 2V power supply and drain current of 14mA was designed using EC2612 transistor. Fig 2 shows the schematic diagram of the amplifier circuit consisting of distributed parameters.

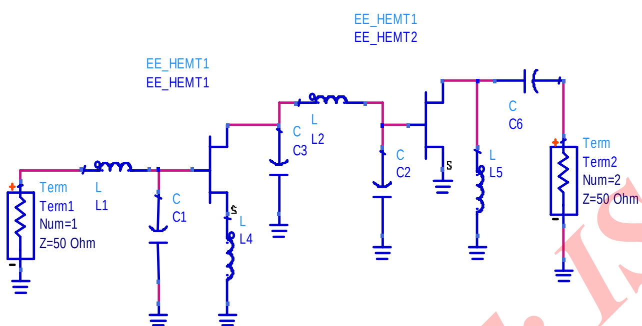

Fig. 2: Schematic diagram of LNA.

One of the important characteristics of an amplifier design is unconditional stability. Whereas Series feedback inductor at source is placed to improve the amplifier stability. Inductive reactance should be as small as possible so that gain would be maximum. Source degeneration provides negative feedback so it reduces the effect of non linearity. Blocking capacitor were used at the input & output of every stage to resist the dc powerentering into the transistor. In this design, pHEMT transistor of width 0.15µm is introduced at every stage.

The characterization of transistors has been done using S-parameters. The device parameters at 5 GHz are S11=-3.15∟-159.8, S22=-9.18∟-149.1, S21= - 7.40∟58.0, Rn = 7.965, NFmin = 0.762 and ┌ opt= 0.514∟91.037. The size of the chip transistor is 0.63* 0.37* 0.1 mm which works only at 25ºC temperature. The circuit design was based on the S2P parameters and noise parameters issued by the foundry.Here. out of the four biasing techniques we opt this circuit so that dc should come to the gate and RF should not enter into the dc. Two power supply is used one is positive and other one is negative to prevent the burn out of GaAspHEMTFig. 3 depicts the biasing circuit which was used in this designing to get a good Q point.

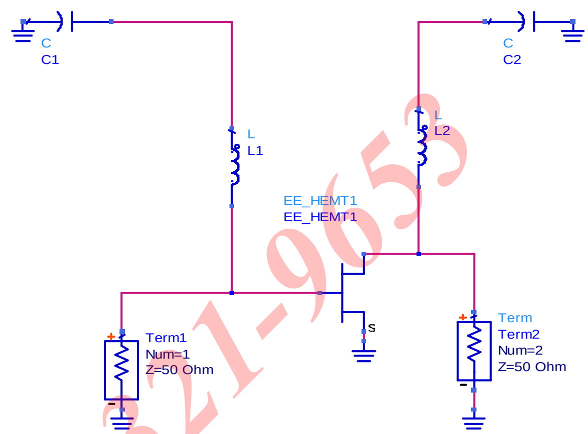

Fig. 3: Baising circuit of LNA.

To achieve the optimum performance in a microwave amplifier proper input and output matching is required which is obtained using smith chart .The first step in designing of LNA was stability check of the device. The stability can be verified by k and | Δ| which is mathematically shown below :

$$K = \frac{1-|S11|^2-|S22|^2+|\Delta|^2}{2|S12\ S21|}$$

$$\Delta = S11S22 - S12S21$$

The condition for unconditionally stable device is K >1 and |Δ| <1. In this case, pHEMT transistor is stable as its showing K>1.

Constant gain and noise circles have been drawn to find a valid point on smith chart for ɼs so that we have acceptable gain and noise figure values. in and out are calculated using formulas 1 and 2.[3,4]

$$\Gamma_{in} = S11 + \frac{S12\ S21\ \Gamma_L}{1-S22\ \Gamma_L}$$

$$\Gamma_{out} = S22 + \frac{S12\ S21\ \Gamma s}{1-S11\Gamma s}$$

III. SIMULATIONS AND RESULT

The designing of matching network has been done by choosing proper point on the desired noise figure and gain values.ADS software is used for designing of LNA using RT-duroidsubstrate having εr = 2.2, thickness = 0.251mm and loss tangent= 0.0009 for lower losses.The matching network is designed on smith chart using smith utility tool and are shown in Fig. 4 and Fig. 5.

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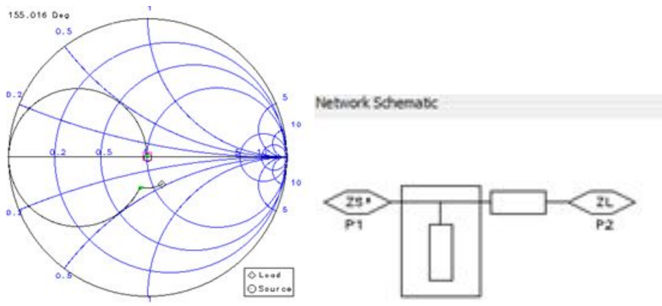

Fig. 4: Smith chart and schematic diagram of Output Matching Circuit.

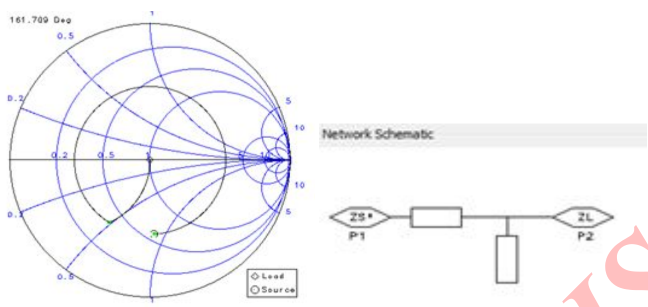

Fig. 5: Smith chart and schematic diagram of Input Matching Circuit.

The input and output return loss at 5 GHz is -24dB and -33dB respectively as shown in Fig. 6 and Fig 7. The noise figure of 0.3dB and gain of 33dB of 3 stageLNA from 3 GHz to 7 GHz range are shown in Fig 8 and Fig 9.

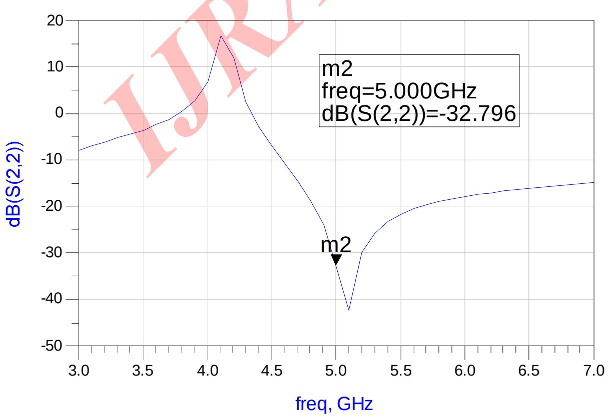

Fig 6 :Graph showing $S_{22}$of pHEMT LNA

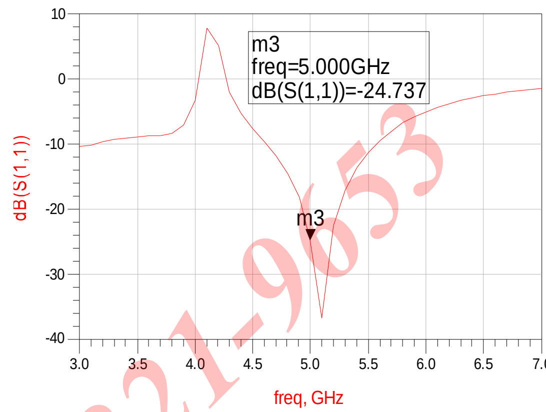

Fig. 7:Graph showing $S_{11}$of pHEMT LNA

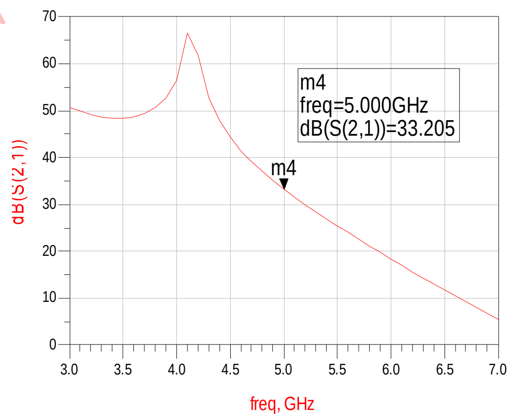

Fig. 8: Graph showing gain S_{21} of pHEMT LNA

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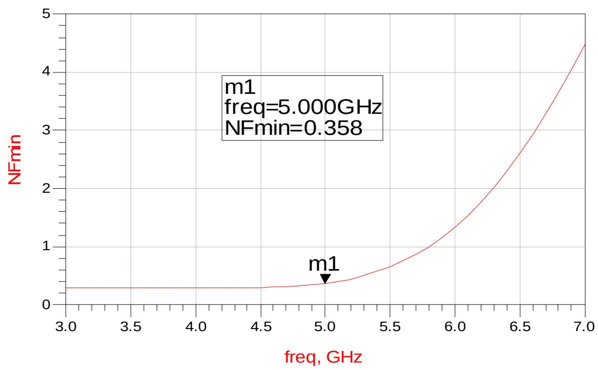

Fig. 9: Graph showing$NF_{min}$of pHEMT LNA

The TABLE 1 lists the comparison of this amplifier to other pHEMT LNA at different frequency. From this comparison, the best result for noise figure is reported by this pHEMT LNA design.

TRANSISTOR	FREQ	S_{21}	S_{11}	S_{22}	NF_{MIN}	K
SKY65048	2.5	15-25	-18	-11	0.7	>1
EC2612	5	33	-24	-32	0.3	>1
MGA-665P8	4.2	16	-21	-23	1.38	>1
NE76000	5.3	15	-22	-32	1.26	>1
WIN	19	11	-22	-12	3.6	>1
Semiconductor						

TABLE 1: COMPARISON OF DIFFERENT TRANSISTORS

IV CONCLUSION

In this paper, the design method of 5 Ghz 3 Stage low noise amplifier based on pHEMT technology has been demonstrated. GaAs gated pHEMT with good dc, low noise performance and high uniformity has the minimum noise figure, which can be as low as 0.3dB with an associated gain of 33dB . Furthermore, very good thermal stability for noise performance and associated gain can be seen. As the results show, InGaP/InGaAs/GaAspHEMTs are promising for MIC applications that require excellent uniformity and good thermal stability.

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