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Study on Performance of Vedic Multiplier Based On the Adders Used

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Abstract— In ALUs, DSPs, and microprocessors addition and multiplication are most commonly used arithmetic computation. Multipliers play a key role in determining the overall performance of the system design. But multipliers use more processer time thus diminishing the overall system performance. Thus to maintain high throughput it is important to select high speed multipliers in terms of low area, low power, less delay. Multiplier involves generation of partial products and also their addition. Vedic mathematics is considered to be a powerful tool for enhancing the calculation speed. It speeds up the multiplication by generation of partial product. Vedic multiplier is considered to be faster multiplier when compared to the other multipliers. The speed of multipliers is based on the adders used for the addition of partial products. In this paper performance of Vedic multipliers are discussed based on the adders used.
Keywords— Vedic multiplier, Urdhva-Tiryakbhaym sutra, 2x2Vedic multiplier, 4x4Vedic multiplier

I. INTRODUCTION

Many instructions in Microprocessor and most of the DSP algorithms perform operations like addition and multiplication; hence addition and multiplication operation play a crucial role in execution time. The demand of high speed processors is increased due to the increasing demand of computer and signal processing applications. To achieve desired performance in many real-time applications, it is highly essential to select high performance multiplier with low power, area and delay. Employing Vedic techniques in computation algorithm of processors reduces the complexity, execution time of the system, power, area etc. Vedic multiplier (VM) is the fastest multiplier and it is based on Vedic multiplication formulae called sutra. Advantage of VM is that the generation of partial product and their addition are done concurrently. Vedic Mathematics is mainly based on 16 sutras where 2 sutras commonly used for multiplication are “Urdhva-Tiryakbhyam (UT) and Nikhilam Sutra”. Nikhlim sutra is basically used for larger numbers which are nearer to their base. Urdhva-Tiryakbhyam sutra means “vertical-crosswise” multiplication. In this technique the partial products and sums are generated parallelly. This sutra is applicable for all cases of multiplication. Here in this paper we consider the Vedic Multiplier based on Urdhva-Tiryakbhyam sutra. Since speed of adders is also considered for speed of multiplication it is important to select adders with high throughput. Reducing delay is advantages since it increases the speed.

II. VEDIC MULTIPLIER

Vedic Mathematics is simple to understand than the conventional mathematics. After eight years of research by Swami Bharati Krishna Tirthaji Maharaja Vedic Mathematics was reconstructed from the “Ancient Indian Scriptures (called Vedas). Multipliers’ using Vedic mathematics reduces the complexity in computation and helps to achieve the desired performance of the system i.e. integrating Vedic Mathematics in Multiplier design enhances the speed of operation. In this paper the discussed multiplier architecture is based on Urdhva-Tiryakbhyam sutra. The line diagram for 4-bit multiplication of UT sutra is as shown in Figure1. Considering an example of decimal numbers (192 x 135) in step1, first the product of 2 LSBs of multiplier and multiplicand is taken, i.e. The product obtained is stored and the carry generated is added to the result of next stage. In next step, the two LSBs (of multiplier and multiplicand) are multiplied crosswise and their product generated is added with the previous carry from step1. In further step the product of middle bits are taken and summed and carry is propagated to next stage. In the last step the 2 MSBs are multiplied and added with carry propagated from previous stage. Therefore the final result is obtained from concatenating the product from each step and carry in last step.

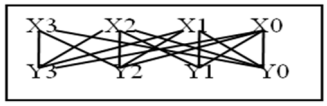

Fig 1: line diagram for 4-bit multiplication of UT

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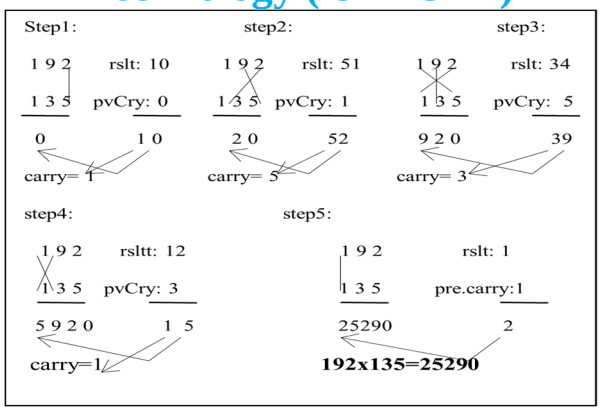

Fig 2: illustration of UT sutra using decimal numbers

Let us consider two numbers x= x_0 x_1 and y= y_0 y_1 as shown in line diagram. First the final product is obtained by taking the product of 2 LSB's i.e. x_0 and y_0 ,in second step the product of the LSB of x with the higher bit of y is taken in crosswise manner, the output carry generated is added to the result of the next step. Next step is to take product of 2 MSB's.

$$S_0= x_0y_0 \ldots\ldots\ldots\ldots\ldots\ldots \quad (1)$$

$$C_1S_1= x_1y_0+x_0y_1\ldots\ldots\ldots\ldots\ldots\ldots(2)$$

$$C_2S_2= C_1+x_1y_1\ldots\ldots\ldots\ldots\ldots\ldots \quad (3)$$

The final result obtained is C_2S_2 C_1S_1 S_0. The 2x2 Vedic multiplier consists of four AND gate and two half adder. The advantage of this multiplier is that as the bit increases the area and delay increases very slowly, hence it is faster when compared with other multipliers. Hence total delay is the sum of delay of 2 half adders after partial product generation.

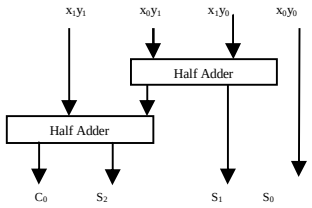

Figure 3: 2x2 Vedic Multiplier

For 4x4 multiplication let us consider two 4-bit numbers x and y i.e. x= x_3 x_2 x_1 x_0 and y= y_3 y_2 y_1 y_0. The procedure for multiplication is explained in the line diagram shown above (figure1). Therefore the final result is C_6S_6 C_5S_5 C_4S_4 C_3S_3 C_2S_2 C_1S_1 S_0. Since the partial products are calculated parallelly the delay can be reduced as the number of bit increases.

$$S_0= x_0y_0 \quad (4)$$

$$C_1S_1= x_1y_0+x_0y_1 \quad (5)$$

$$C_2S_2=C_1+x_0y_2+x_2y_0+x_1y_1 \quad (6)$$

$$C_3S_3=C_2+x_0y_3+x_3y_0+x_1y_2+x_2y_1 \quad (7)$$

$$C_4S_4=C_3+x_1y_3+x_3y_1+x_2y_2 \quad (8)$$

$$C_5S_5=C_4+x_3y_2+x_2y_3 \quad (9)$$

$$C_6S_6=C_5+x_3y_3 \quad (10)$$

The 4x4 multiplication can be implemented using four 2x2 vedic multiplier modules and three ripple carry adders of 4-bit size is used. 4-bit RCA is used for the addition of two 4-bit numbers. The arrangement of RCA is as shown in the figure, which reduces the computation time thus reducing the delay to give better performance

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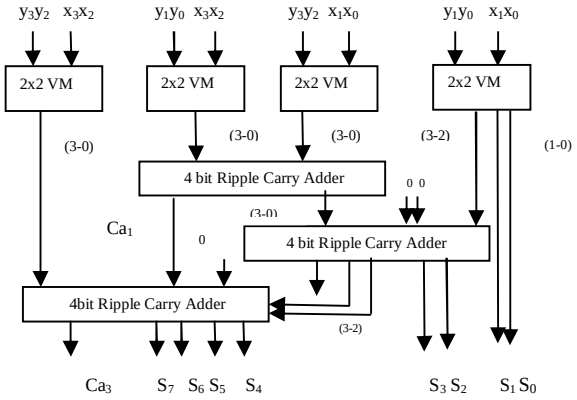

Figure 4: 4x4 Vedic Multiplier

III. SURVEY DESIGNS

J. Thomas et.al [1] has compared the performance of Vedic multiplier in terms of area, delay and power on the basis of adder used. Here they compared 8x8 Vedic multiplier based on different adders used and the factors considered are delay, area and power. This analysis is done to find the suitable design of multiplier to achieve the desired applications like low area, low power and low delay. These factors are compared for different adders such as carry Lookahead adder (CLA), carry select adder (CSLA), parallel prefix adders like Kogge stone adder (KSA), Ladner Fischer adder (LFA) and Brent Kung adder (BKA) in Vedic multiplier. This paper gives information about Urdhva-Tiryakbhyam algorithm of Vedic Mathematics that is utilized for multiplication and also gives brief description about adders that can be used in Vedic multiplier ,to improve the speed and area of multiplier.

CADENCE &XILINX	Adders	Area (slices)	Power(mW)	Delay (nsec)
	CLA	89	57.2	29.981
	CSLA	93	42.2	28.644
	KSA	105	57.3	31.788
	LFA	89	57.2	28.981
	BKA	91	57.0	29.944

Table 1: Comparative study of various adders used in Vedic multiplier

The above table gives the analysis report of the 8x8 Vedic multipliers with fast adders on the basis of parameters area, delay and power. Among parallel prefix adders in terms of area and delay LFA shows the better performance but the disadvantage is that it has larger fan-out. Though KSA has large area and delay compared to LFA and BKA it has lesser fan-out when compared to both. CLA is better in terms of speed and delay when compared with other adders. Thus after analysis it is sad that CSLA being the fastest adders, it will best adder for designing of Vedic Multiplier (VM).

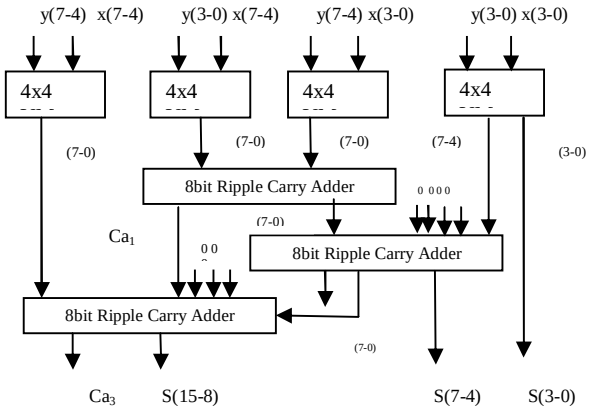

Figure 5: 8*8 vedic multiplier

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S.Tamilselvan et.al [2] in their paper they have mainly focused on the reducing the time delay of the multiplication operation. The Vedic multipliers (VM) are implemented with the adders having lesser time delay. The comparison is done in between ripple carry adder, carry lookahead adder, carry skip adder and carry select adder. Comparison says that carry select adder has lesser time delay compared to others. Hence CSLA is used in VM for addition process. VM can be used in FFT algorithms.

	Adders	Area(slices)	Delay(nsec)
XILINX	CLA	10	6.494
	RCA	6	7.682
	CSLA	6	6.494
	CSkip	8	6.494

Table 2: Comparison of 4 Bit Adders Based On Time Delay

P.Devpura et.al [3], in their paper, a novel 8*8 bit Vedic multiplier which is based on "Urdhva triyakbhyam sutra" is proposed and it uses Binary to Excess-1 code converter, as its key component to increase the speed and reduce the area utilized by the multiplier. They have also compared area, delay and power with the existing topologies. The proposed architecture shows the better performance when compared to others. thus fulfilling the motivation of both reduced delay and area.

Vedic Architecture	Delay (ns)	Logic Delay(ns)	Route Delay(ns)	Slice Utilization
Conventional Architecture	21.644	10.893	10.751	119
Carry Save Adder Based Architecture	21.608	11.372	10.236	104
Carry Save Adder+BEC based Architecture	18.139	9.996	8.143	100

Table 3: Comparison of BEC-1 based multiplier with existing topology

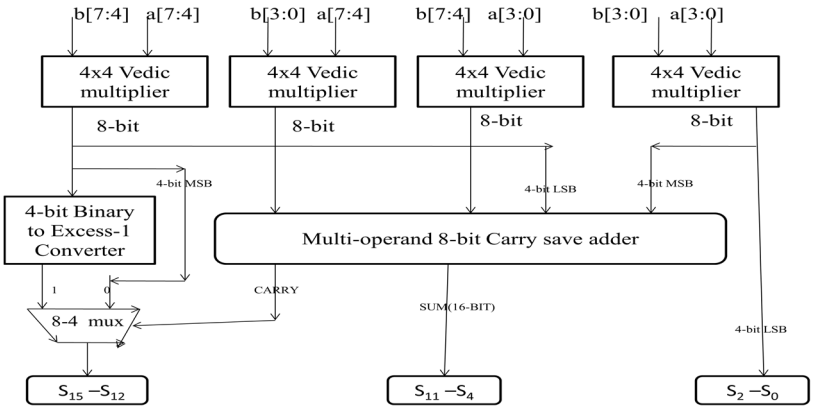

Figure 6: Proposed BEC-1 based Vedic multiplier

In this proposed architecture is divided into 4 blocks
4x4 Vedic multiplier
Multi-operand carry Save adder
Binary to Excess-1 Converter
8:4 Mux
The multi-operand carry save adder reduces the addition on 3 numbers into 2 numbers. The purpose of using BEC-1 is to reduce the

computation time for addition and decrease the delay. The 8:4 Mux is used for conditional addition, it selects the output of BEC-1 if the carry generated by Multi-operand carry save adder is zero else output is taken directly from the partial product generated by 4x4 VM if the carry =1. The 4x4 VM uses 2x2 VM modified by multi-operand carry save adder.

Bhavani Prasad.Y et.al [8], have described the design of low power and high speed Modified Carry Select Adder for 16 bit Vedic Multiplier. In this paper, a high speed and low power 16x16 Vedic Multiplier is designed by using low power and high speed modified carry select adder. This gives less power consumption when compared to other multiplier techniques because the number of additions gets reduced by applying Urdhva-Tiryakbhyam which is a short approach form of multiplication. In this paper the proposed 16-bit modified CSLA consists of

Ripple Carry Adder

Basic Unit (Binary to Excess-1 Converter)

Multiplexer

Ripple Carry adder (RCA) is called as Ripple carry adder because each carry bit "ripples" to the next full adder. RCA is designed using multiple full adders, which allows for fast design time since RCA layout is simple. Binary to Excess-1 converter (BEC) is designed using XOR, AND and NOT gates, which reduces the area, time delay and power consumption since it uses less number of gates compared to normal RCA. The expressions for 4-bit BEC is given below

$$E_0 = \sim B_0 \quad (11)$$

$$E_1 = B_0 \wedge B_1 \quad (12)$$

$$E_2 = B_2 \wedge (B_0 \& B_1) \quad (13)$$

$$E_3 = B_3 \wedge (B_0 \& B_1 \& B_2) \quad (14)$$

Multiplexers (Mux) are used for the selection of output between RCA and BEC. Multiplexer is also called as Data selector. It has 2^n inputs and n select lines. Depending on the select lines the input is send to the output . Therefore this 16- bit modified CSLA reduces the computation time such that the delay decreases. The proposed 16x16 VM using Modified CSLA is as shown

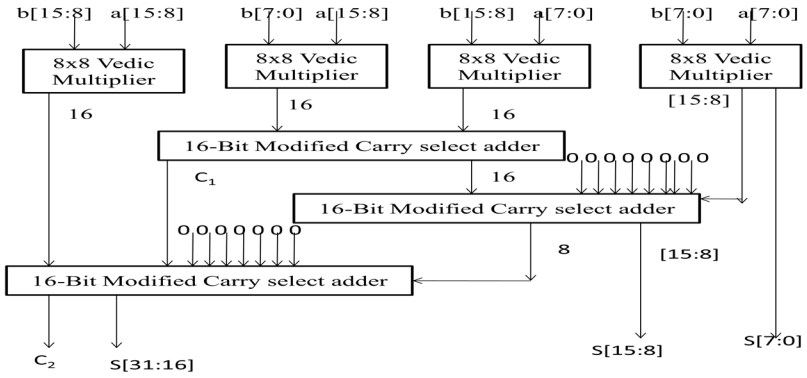

Figure 7: Proposed 16x6 VM architecture [8]

This proposed multiplier has very less delay, because of the addition of new 16-bit modified CSLA module. This proposed VM consumes less power because the number of addition is reduced by applying UT sutra, which is the short approach for multiplication. This technique can be used for DSP applications and also for low power applications.

III. CONCLUSION

This paper presents the brief study on Vedic multiplier based on adders used. Vedic multiplier is designed using various adders to achieve high speed, low area, low power consumption, and reduced delay. Vedic multipliers can be used in different fields of applications like Digital Signal Processing (DSPs), FFT algorithms, Convolution, Multiplication and Accumulation (MAC) unit and in many microcontroller and microprocessors.

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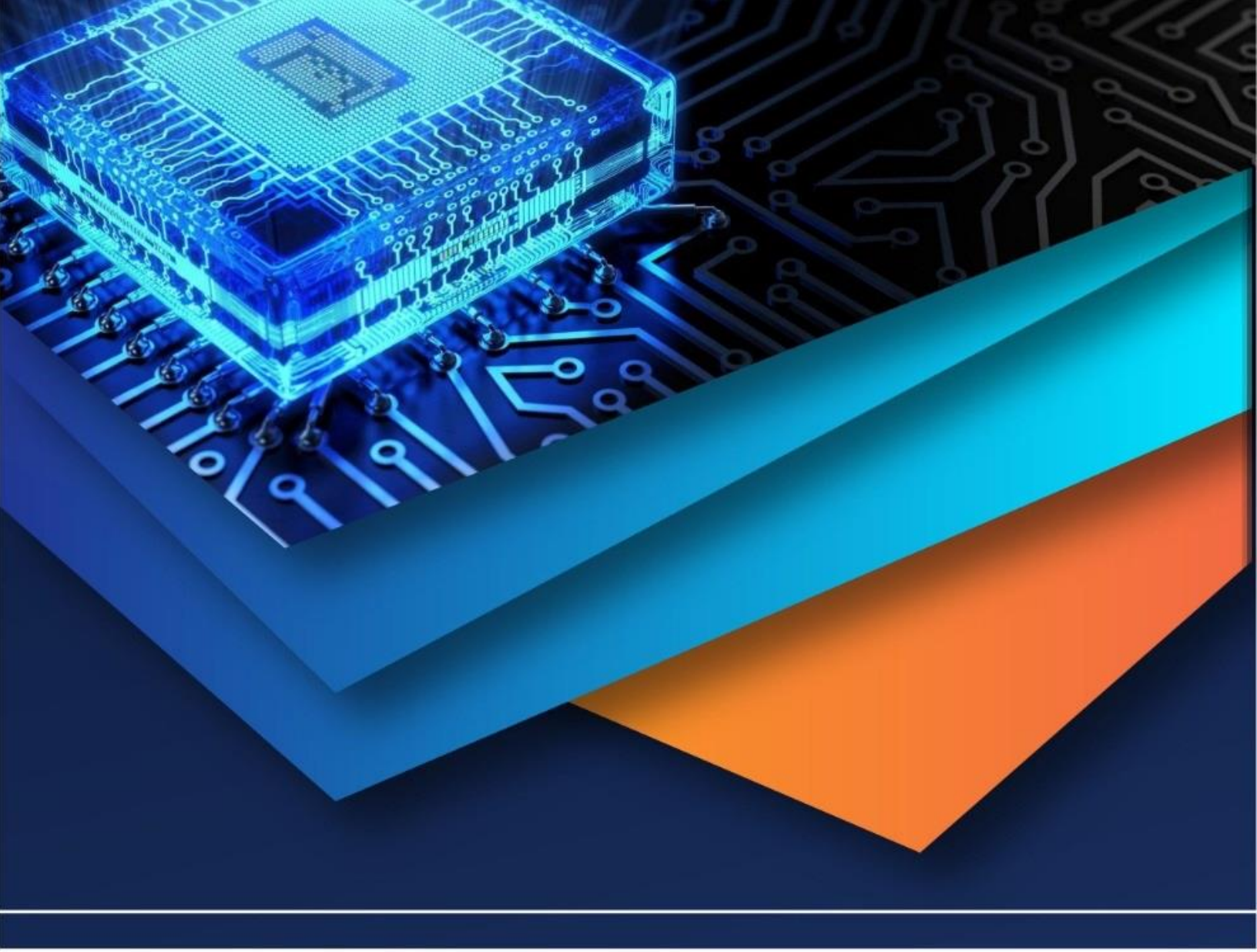

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