iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 4 **Issue:** VI **Month of publication:** June 2016

DOI:

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)

Reconfigurable Fir Filter for Software Defined Ratio Based On VHBCSE Algorithm

Yuvaraju.M[1], Naraina.A[2], Sethulaksmi V S[3]
[1]Assistant Professor, Department of EEE, Anna university Regional campus Coimbatore, Tamilnadu, India
[2,3]PG Scholor, Department of EEE, Anna university Regional campus Coimbatore, Tamilnadu, India

***Abstract*: To reduces the number of multiplications per input sample(MPIS) and additions per input sample(APIS) an optimization technique consist of two-step is used in the design of reconfigurable interpolation filter for multi standard digital up converter(DUC). . For the better efficiency of the constant multiplier a vertical-horizontal binary common sub-expression elimination (VHBCSE) algoritm is used (FIR filter whose coefficient dynamically changes).This reducing the area and as well as power.**
Keywords: VHBCSE algoritm, FIR filter, Software defined radio, Digital up converter.

I. INTRODUCTION

Nowadays the communication devices should provide two main features first it should provide global roaming and second is the interfacing with different systems and standards. The existing technologies for different systems such as voice, video, data etc uses different data type, signal processing techniques and packet structures.
According to Joe mitola in 1991"A radio that defines in software its modulation, error correction and encryption processes, which control over the RF hardware and can be reprogrammed is clearly as software defined ratio".Finite – Impulse Response(FIR) filters is used for variety of tasks such as channel equalization, spectral shaping, interference cancellation and matched filtering
There are various architectures and implementation methods have been proposed to improve speed and performance. The multiplier in the FIR filter defines the performance such as speed and less area of it. An algorithm called multiple constant multiplication has been proposed in the design can be categorized into two groups 1) Graph based algorithms and 2) Common sub-expression elimination (CSE) algorithm.
But MCM design is not suitable for SDR because the filter coefficient in Software define ratio will change system dynamically according to its needs .The coefficients are programmable in SDR and also highly computationally efficient.
Another method used for constant multiplication is binary common sub-expression elimination (BCSE) algorithm. The algorithm can eliminates the common sub-expression in binary. But this algorithm increasing the adder step and also the hardware cost. So this algorithm is insufficient for SDR. Many algorithms like MCM and BCSE are discussed before. In this paper a VHBCSE algorithm is discussed to overcome these problems.

II. MERITS OF USING VERTICAL-HORIZONTAL BINARY COMMON SUB-EXPRESSION ELIMINATION (VHBCSE) ALGORITM

The vertical-horizontal binary common sub expression elimination (VHBCSE) algorithm solve the problem efficiently that other existing method. The product of original filter coefficient and its complemented value is taken for the signed decimal data representation. This step is done based on the most significant bit of the filter coefficient.
At layer 1 of MAT 2-bit BCSE is applied vertically. After that at layer 2 section 4and 8-bit BCSE's horizontally is done. This process is done in layer 3also such that hardware usage is reduced .Again this technique is done in the lower layer also which helps to reduce usage of power. Repeated use of 2-bit,4-bit and 8-bit BCSE at different layer also decrease area.

III. DESIGN OF RECONFIGURABLE FIR FILTER

In this architecture parameters based on which selection of different interpolation factor and roll off factor are selected. These parameters are represented as INTP, FLT. Interpolation factor is defined as the ratio of output rate and input rate. While the roll off factor is defined as the measure of the excess bandwidth. In this design four clocks are used the first clock is used to sample the output (a master clock (CLK)).The other clocks are denoted as CLK4 (master clock divided in four equal parts), CLK6 (master

Volume 4 Issue VI, June 2016
ISSN: 2321-9653

clock divided in six equal parts), CLK8 (master clock divided in eight equal parts). The value 4,6,8 are the three interpolation factor represented the three different systems. These 3 clock are used to sample the input RRCIN. The processed architecture consist of data generator (DG), a coefficient generator(CG), a coefficient selector(CS), and an accumulation unit block(FA).

A. Data generator

Data generator task is to sample the input data (RRCIN) based on the interpolation factor selection parameter(INTP_SET), here 7 branch filters are used because the design is for 25, 37 and 49 tap filter (ie,[25/4]=[37/6]=[49/8] =7,here 4,6,8 are the interpolation factor).

B. Co-efficient generator block

The task of coefficient generator block is to multiplexer the input with the coefficient filter. Here a two phase optimization technique is proposed to reduce the hardware usage, low computation time and low complexity. Coefficient generator block consist of first coding pass(FCP unit), second coding pass(SCP unit), partial product generator(PPG unit) and multiplexer unit.First code pass block consist of three coding blocks. These three coding blocks are running according to the three interpolation factor.

The output of the first code pass block is given as input to the second code pass block. The output of the second code pass will be the final In the next stage of partial product generator shifting of the data and addition process is executed. This operation gives the multiplication output of input and filter co-efficients sets.

In multiplexer unit and in additional unit summing of partial product generator output is done. This operation is followed by eight multiplexer.

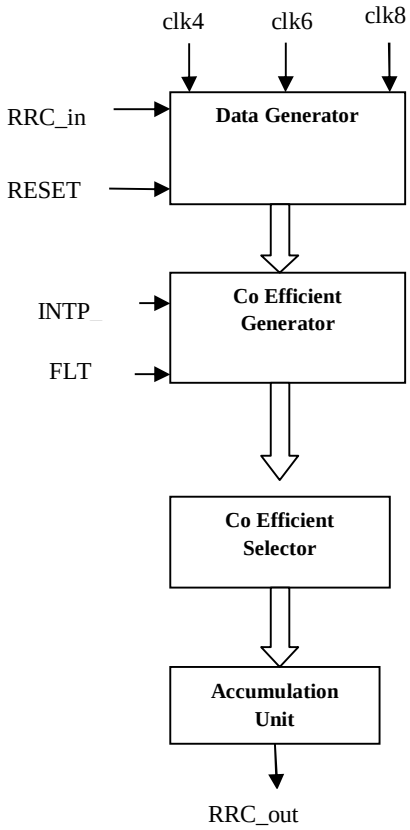


Fig. 1.Block Diagram of Proposed System Architecture

C. Coefficient Selector

The appropriate data which are generated are selected properly and it is provided to the Data accumulation block. The data will be

selected according to the interpolation factor and roll off factor.

D. Data Accumulation Block (FA)

Transposed direct form architecture is used in proposed reconfigurable FIR filter. It consist of six adders and six registers.

IV. VHBCSE ALGORITM

The steps for the vertical-horizontal binary common sub-expression elimination (VHBCSE) algoritm :

The inputs of 16 bits (x[15:0]) are received.

17-bit coefficients is stored in look up table,(h[16:0]).

Except the MSB of take the 1's complement of the coefficient h1[15:0].

Check whether the most significant bit is 1,if it is one the complemented coefficient matrix h[15:0] to generate the multiplexed coefficient matrix m[15:0].

The multiplexed coefficient matrix m[15:0] is divided into static groups of 2bits used for the select lines to M7-M0 multiplexer.

The multiplexer group is again partitioned into 4 bit each matrices (m[15:12],m[11:8], m[7:4], m[3:0]).

Compare the matrices m[15:12] and m[11:8].If they match the output of A2 adder is avoided.Then output of A1 is shitted by 4-bit right and given as an input to adder A5.If they do not match, output of A2 adder is taken instead.

Compare the matrices m[15:12] and m[7:4].If they match the output of A3 adder is avoided.Then output of A1is shifted by 8 bit right and given as an input to A6.Else compare the matrices m[11:8] with h[7:4]if they matches avoid A3 adder's output use take the 4 bit right shifted output of the adder A2 and give it as input to the adder A6.Else use the output of A3.

Compare the matrices m[15:12] and m[3:0].If they match the output of A4 adder is avoided. Then output of A1is shifted by 12 bit right and given as an input to A6.Else compare m[11:8] with h[3:0] .If they matches avoid A4 adder's output ,use the 8 bit right shifted output of the adder A2 and give it as input to the adder A6.Otherwise compare the matrices m[7:4] and m[3:0].If they avoid output of adder then avoid output of adder A4 .For that use the 4bit right shifted output of A3 adder and give it to input to adder A4.Else use the A4 adder's output.

Again partition the multiplexed coefficient into 8 bit group m[15:8],m[7:0].

Compare the matrix m[15:8] and m[7:0].if they matched the output of A6 adder is avoided. For that use the 8 bit right output of A1 adder and give it as an input to A7.Else take adder A6 for output.

The final addition result is performed by 1-bit right shift on the output of the A7 adder.

2"complement of A7 adder is taken.

If 17^{th} bit of MSB of h[16] is 1 then choose the complement otherwise consider the original A7.

Multiplication is done .The result is stored in the register.

A. Flow Chart Description

The flow chart describes the method of finding h*X in VHBSCE algoritm .In this VHBSCE algoritm first input X[15:0](ie 16 bit input is taken).The 17bits coefficient (ie h[16:0]) is saved in the look up table ie LUT.

The algoritm first check whether 17 bit ie h[16] is '1' or not. If 17 bit is '1' the coefficient matrix is 1's complemented excluding MSB (that is only 16 bit is 1's complemented 17^{th} bit is avoided).Thus we get a multiplexed coefficient m[15:0] which is denoted as MC. If 17 bit is '0'not '1' then the original version coefficient matrix is taken to produce the multiplexed coefficient(MC),here also the MSB is ignored.

The Multiplexed coefficient (MC)(m[15:0]) thus obtained is divided into 2 bits of groups which is be used as select lines of multiplexers (M7-M0).The multiplexer coefficient (MC) (m[15:0]) is also divided into 4 bits of groups which are denoted as m[15:12],m[11:8],m[7:4],m[3:0].After this partition m[15:12] is compared with m[11:8]. If they matches the output of Adder A1 is right shifted by four bits and used as the input to Adder A5.The output of Adder A2 is avoided. If the match is not find just use the output of Adder A2 as input of Adder A5.

Volume 4 Issue VI, June 2016
ISSN: 2321-9653

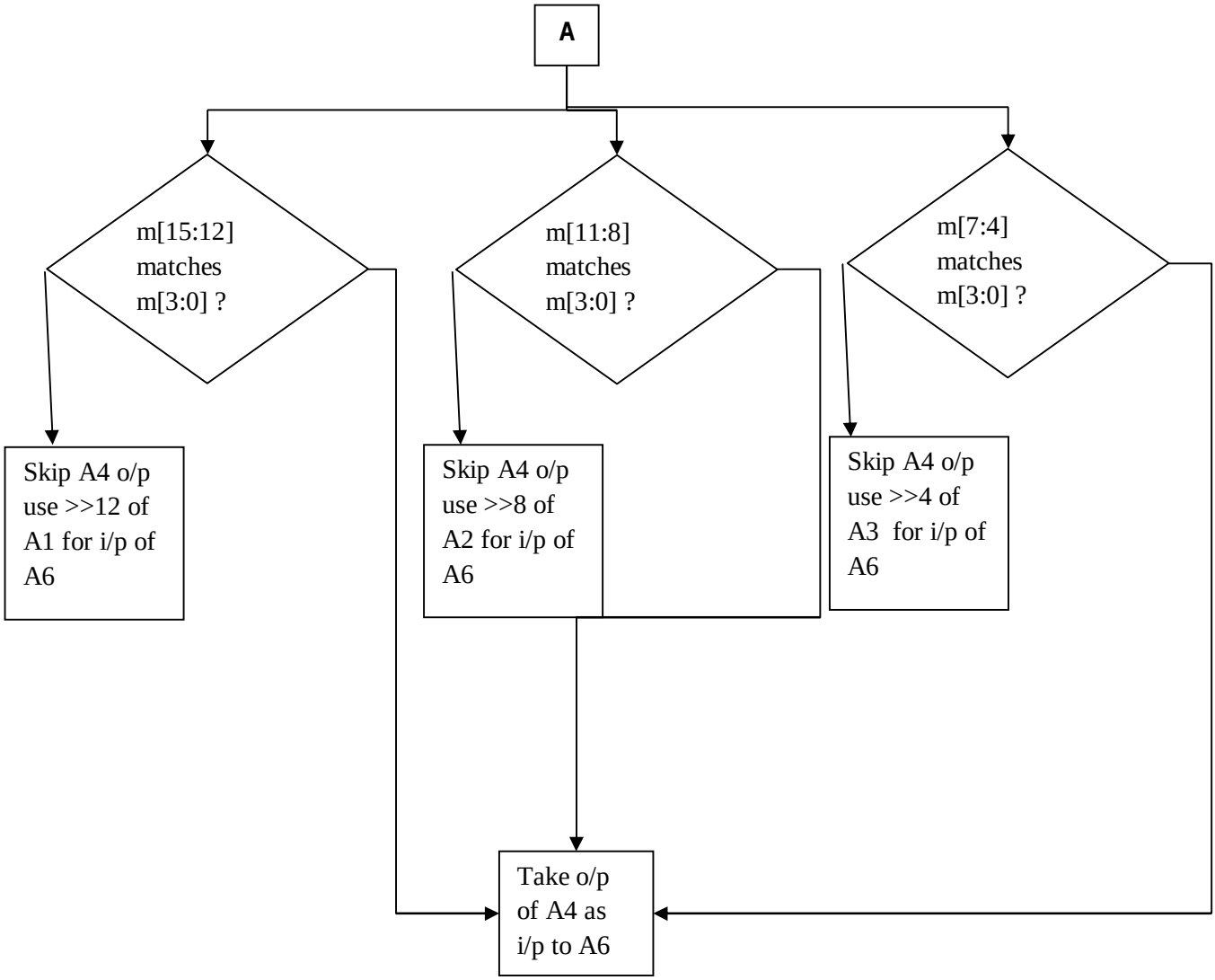


Fig 2. Flowchart 1

Volume 4 Issue VI, June 2016
ISSN: 2321-9653

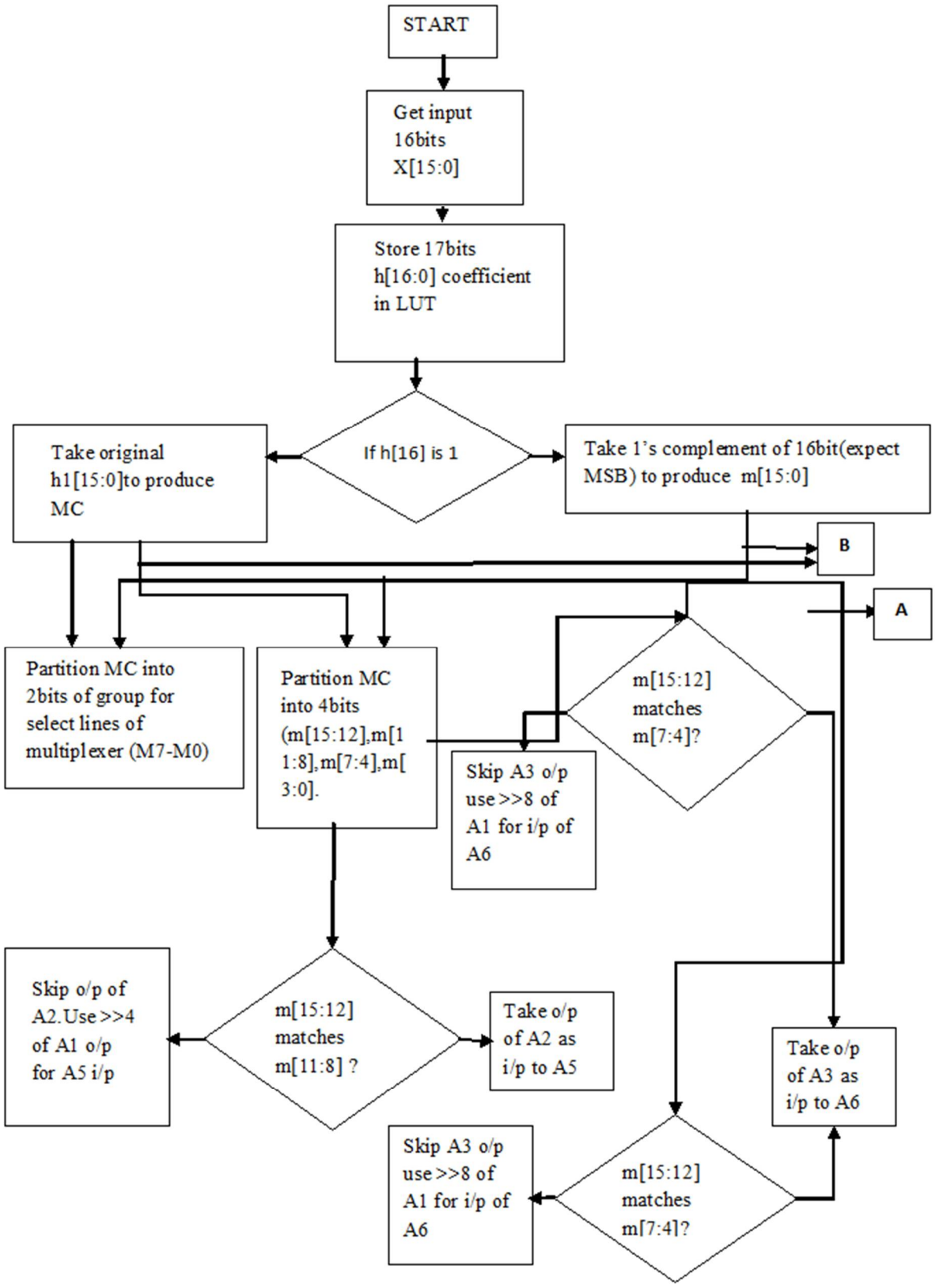


Fig:3 Flowchart 2

Again the m[15:12] is compared with m[7:4]. If they matches the output of Adder A1 is right shifted by eight bits and used as the input to Adder A6.The output of Adder A3 is avoided. If the match is not find just use the output of Adder A3 as input of Adder A6. Again compare m[11:8] and m[7:4]. If they matches the output of Adder A2 is right shifted by four bits and used as the input to Adder A6.The output of Adder A2 is avoided. If the match is not find just use the output of Adder A3 as input of Adder A6. After these steps m[15:12] and m[3:0]. If they matches the output of Adder A1 is right shifted by twelve bits and used as the input to Adder A6.The output of Adder A4 is avoided. If the match is not find just use the output of Adder A4 as input as of Adder A6.

Also consider m[11:8] and m[3:0]. If they matches the output of Adder A2 is right shifted by eight bits and used as the input to Adder A6.The output of Adder A4 is avoided. If the match is not find just use the output of Adder A4 as input as of Adder A6. Again consider m[7:4] and m[3:0]. If they matches the output of Adder A3 is right shifted by four bits and used as the input to Adder A6.The output of Adder A4 is avoided. If the match is not find just use the output of Adder A4 as input as of Adder A6.

The MC ie the multiplexer coefficient is again divided into eight of groups m[15:8] and m[7:4].

The m[15:8] and m[7:0] is compare.If they matches each other the output of Adder A5 is right shifted for eight bit and used as the input to Adder A7.The output of Adder A6 is avoided. If the match is not find just use the output of Adder A6 as input as Adder A7.

Volume 4 Issue VI, June 2016
ISSN: 2321-9653

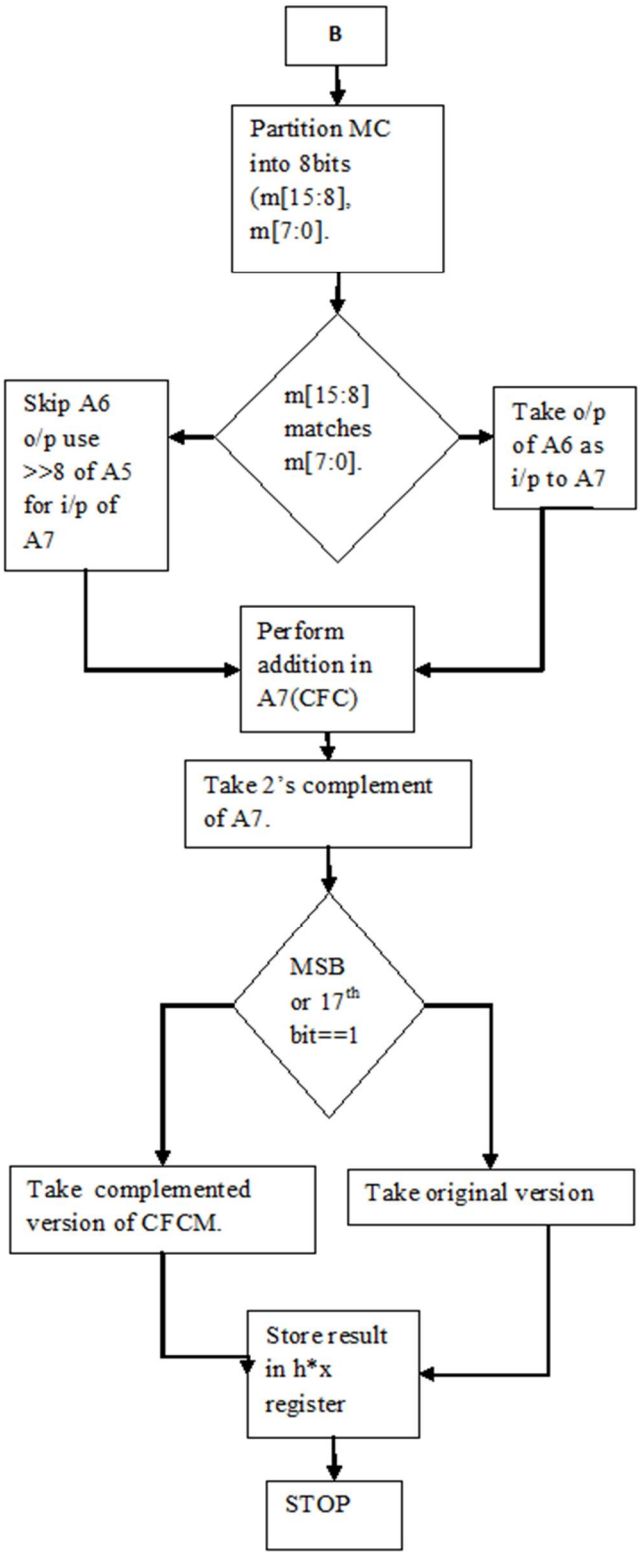


Fig:4 flow chart 3

Volume 4 Issue VI, June 2016
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

Perform the addition in Adder A7 which is denoted as CFC. The 2's complement of the output of Adder A7 is obtained.

If the most significant bit ie 17th bit is '1' take the complemented version otherwise take the original version. At last store the result h*X in h*X register.

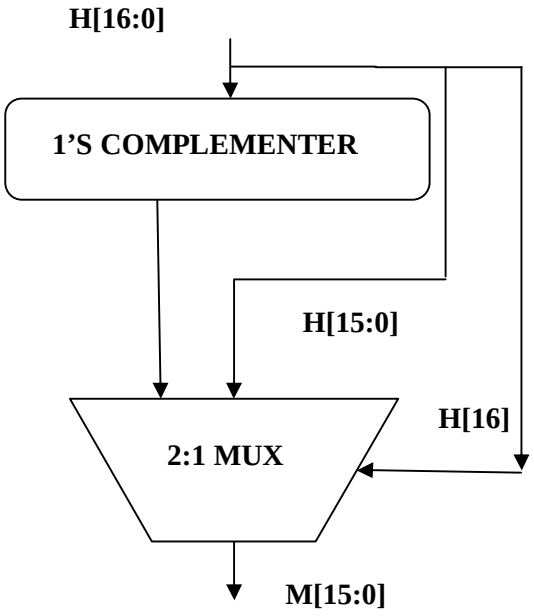


Fig 5. Sign Convention Unit

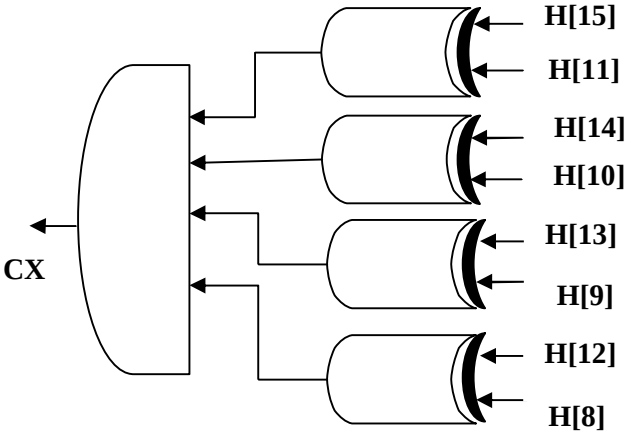


Fig 6. Logic Control Block

Volume 4 Issue VI, June 2016
ISSN: 2321-9653

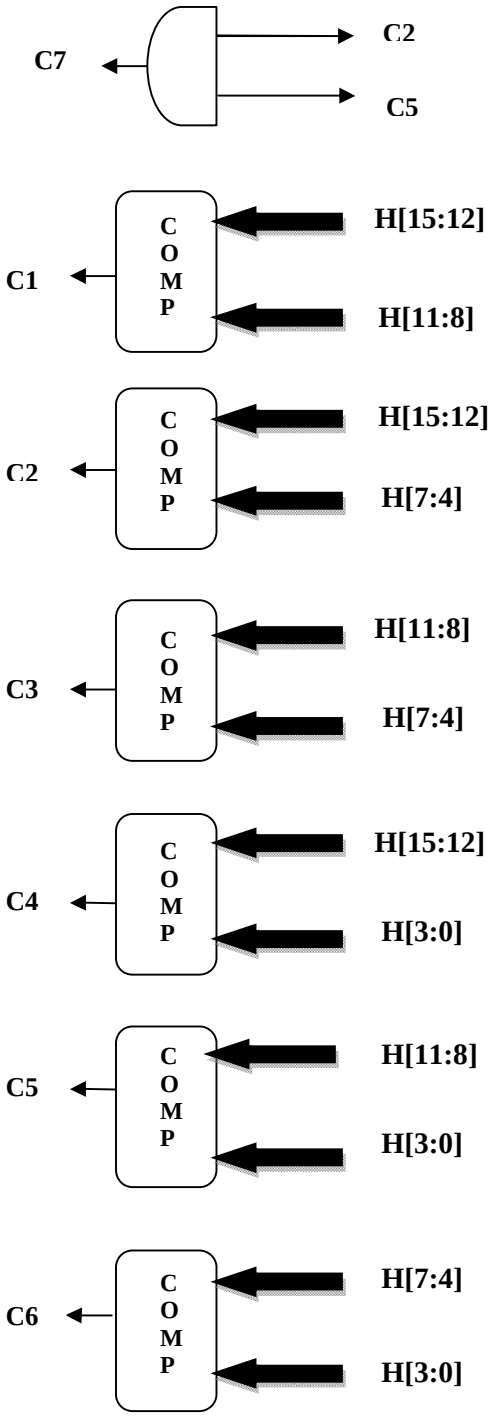


Fig 7. Logic Control Block

Volume 4 Issue VI, June 2016
ISSN: 2321-9653

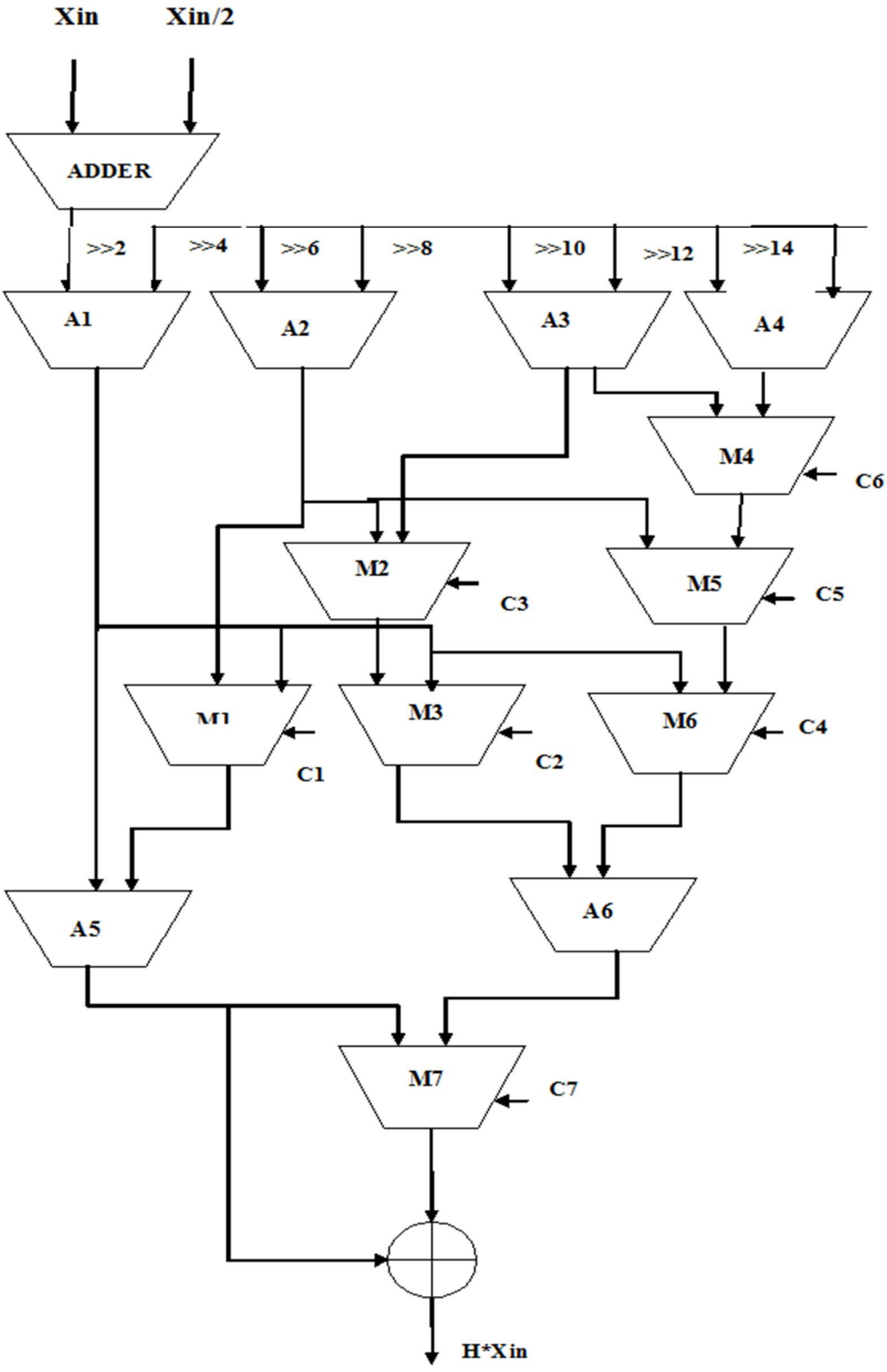


Fig 8. Final Addition Unit

Volume 4 Issue VI, June 2016
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

V. RESULT AND DISCUSSION

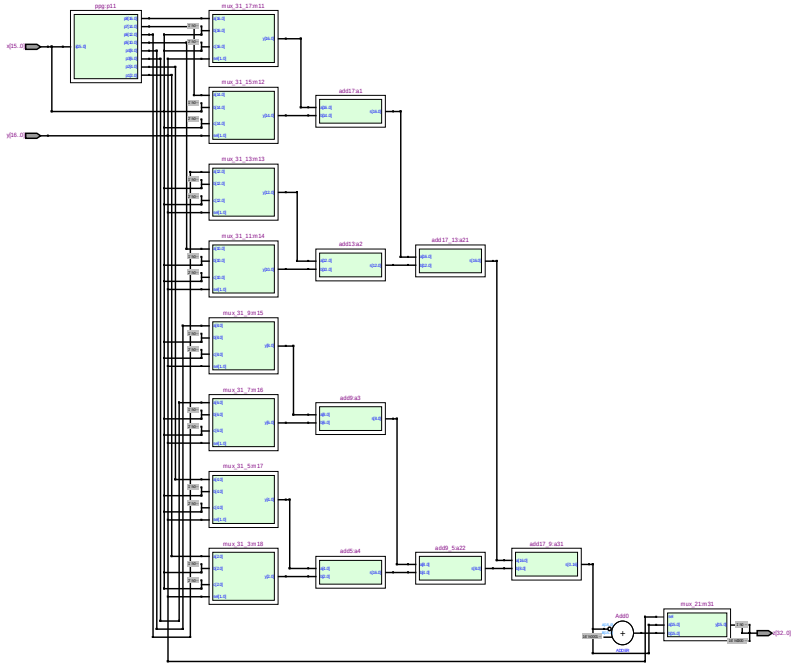


Fig.9 RTL Viewer

The above figure shows the RTL viewer of the VHBSCE algoritm based Reconfigurable FIR filter for SDR.

The next figure shows the waveform generated by the circuit

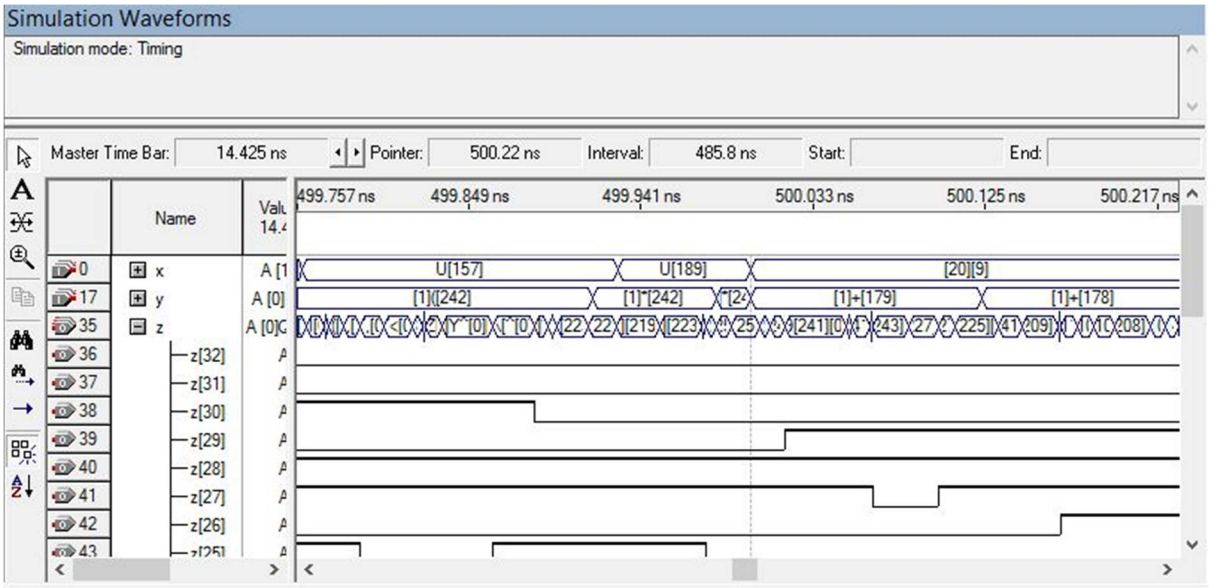


Fig.10.Simulation Result

VI. CONCLUSION

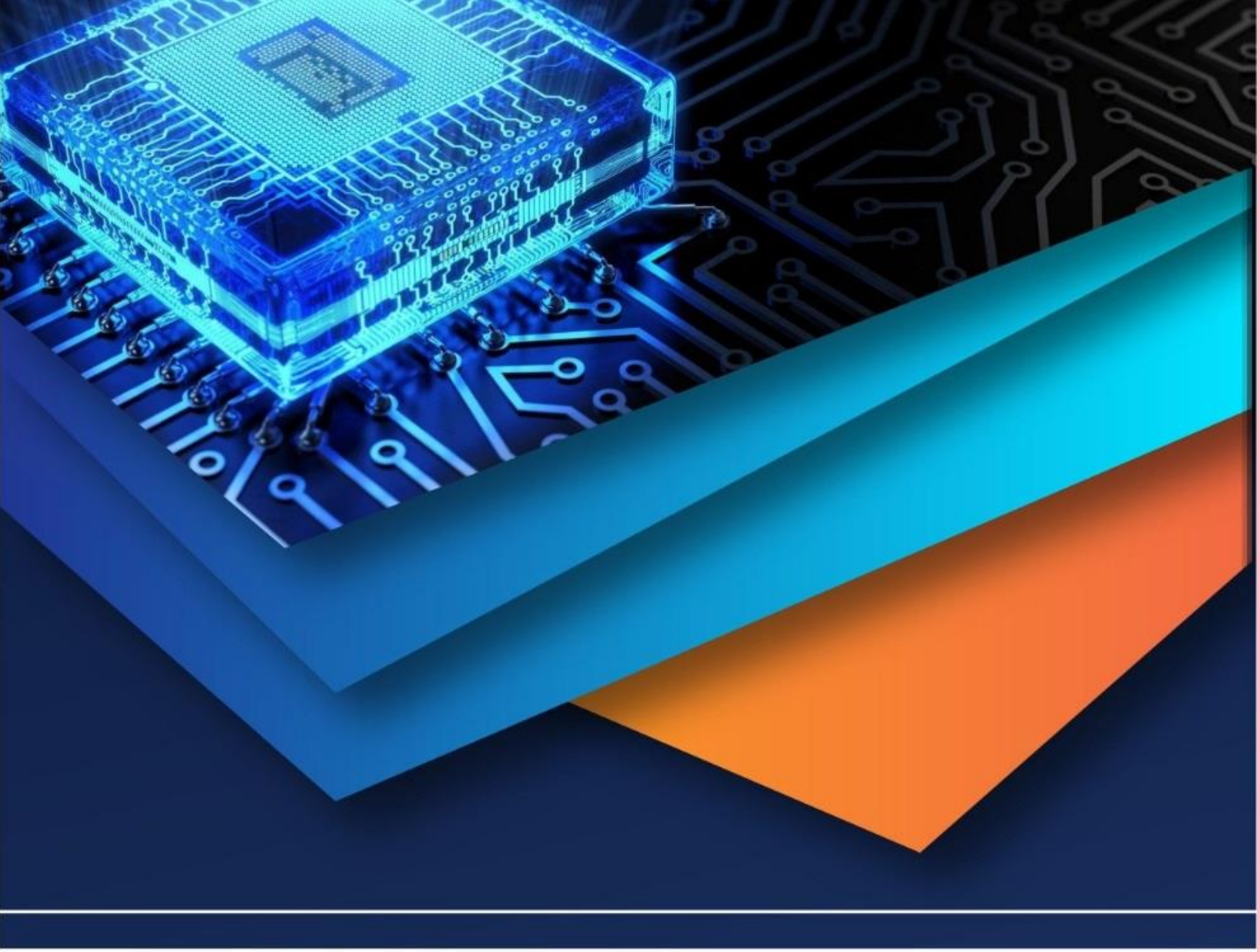
The proposed reconfigurable filter architecture suitable for multistandard DUC, the important component of SDR. Here a two step optimization technique is used to make the desired filter more efficient by reducing area and power along with improvement in the maximum operating frequency. The proposed constant multiplier based on VHBCSE algorithm will maximize the efficiency and this algorithm also supports the signed decimal data representation of input and coefficient. This system is more suitable for next generation efficient system of SDR.

VII. ACKNOWLEDGEMENT

This research and material reported in this document are supported by the Anna university regional campus Coimbatore.

REFERENCES

[1] J. Mitola, "The software radio architecture," IEEE Commun. Mag., vol. 33, no. 5, pp. 26–38, May 1995.
[2] Hatai, Indranil, Indrajit Chakrabarti, and Swapna Banerjee. "An Efficient Constant Multiplier Architecture Based on Vertical-Horizontal Binary Common Sub-expression Elimination Algoritm for Reconfigurable FIR Filter Synthesis", IEEE Transactions on Circuits and Systems I Regular Papers, 2015.
[3] S. Im, W. Lee, C. Kim, Y. Shin, S. H. Lee, and J. Chung, "Implementation of SDR-eared digital IF channelized dechannelizer for multiple CDMA signals," IEICE Trans. Commun., vol. E83-B, no. 6, pp. 1282–1289, Jun. 2000.
[4] S.-F. Lin, S.-C.Huang, F.-S.Yang, C.-W.Ku, and L.-G. Chen, "Power-efficient FIR filter architecture design for wireless embedded system," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 51, no. 1, pp. 21–25, Jan. 2004.
[5] Y. Son, K. Ryoo, and Y. Kim, "1:4 interpolation FIR filter," IEEE Electron.Lett., vol. 40, no. 25, pp. 1570–1572, Dec. 2004.
[6] P. K. Meher, S. Chandrasekaran, and A. Amira, "FPGA realization of FIR filters by efficient and flexible systolization using distributed aritmetic," IEEE Trans. Signal Process., vol. 56, no. 7, pp. 3009–3017, Ju l. 2008.
[7] J. Xie, J. He, and G. Tan, "FPGA realization of FIR filters for high-speed and medium-speed by using modified distributed aritmetic architectures," Microelectron. J., vol. 41, no. 6, pp. 365–371, Jun. 2010.
[8] K.-H. Chen and T.-D.Chieueh, "A low-power digit-based reconfigurable FIR filter," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 53, no. 8, pp. 617–621, Aug. 2006.
[9] O. Gustafsson, "Lower bounds for constant multiplication problems," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 54, no. 11, pp. 974–978, Nov. 2007.
[10] D. Shi and Y. J. Yu, "Design of linear phase FIR filters with high probability of achieving minimum number of adders," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 58, no. 1, pp. 126–136, Jan. 2011.



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY