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Low Power Cam Gain High Speed with Parity Bit and Power Gated Ml Sensing Technique

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Abstract: ***Content addressable memory (CAM) it compares input search data against a table of stored data and returns the address of matching data. It have a single clock cycle throughput and make them faster than other hardware, software based search system. It uses various applications requiring high search speed. Applications include parametric curve extraction Huffman coding/decoding and image coding. The primary application of CAM is to classify into forward Internet protocol packets in routers. In networks messages are sent by e-mail or web page is transferred into first breaking up the message into small data packets of few hundred bytes and then sending each data packet individually in the network. These packets are transferred from the source through the intermediate nodes of the network that reassembled at the destination to reproduce the original. The function of router is too comparing the destination address of a packet to all possible routes in order to select the best one. A CAM is a good choice for implementing this lookup operation due to its fast search capability.***
Key words- CAM, ML sensing, Parity Bit, CMOS, Huffman coding/decoding, lookup table

I. INTRODUCTION

Content Addressable memory has the input to the system is the search word that is used for the search lines to the table of stored data. The number of bits in a CAM word is always large, with existing implementations ranging from 36 to 144 bits. A CAM employs a table size ranging between a some hundred entries to 32K entries, corresponding to an address space ranges from 7 bits to 15 bits. Each stored word has a match lines that indicates both the search word and stored word are identical or are different. The match lines are fed to an encoder that generates binary match location corresponds to the match line that will be in the match state. An encoder is used in systems has only a single match is expected. In CAM application has more than one word may match, a simple encoder is not used but priority encoder for this applications. A priority encoder selects high priority match location to map to the result with words in low address locations receiving higher priority. In addition, there is often a signal hits that flags in which there is no matching location in the CAM. The whole function of a CAM is to take a search word and return the matching memory location. The operations are fully programmable arbitrary mapping of the large space of the input word to the smaller space of the output match location. The operation of a CAM is that it tag portion of a fully cache. The portion of a cache is to compares its input that is an address, to all addresses stored in the tag memory. In the process of match a single match line goes high indicates the location of a match. CAM caches won't use priority encoders since only a single match occurs the match line directly activates a read of the data portion of the cache associated with the matching tag. However, focus on large- capacity CAMs rather than on fully associative caches, has target smaller capacity and higher speed.

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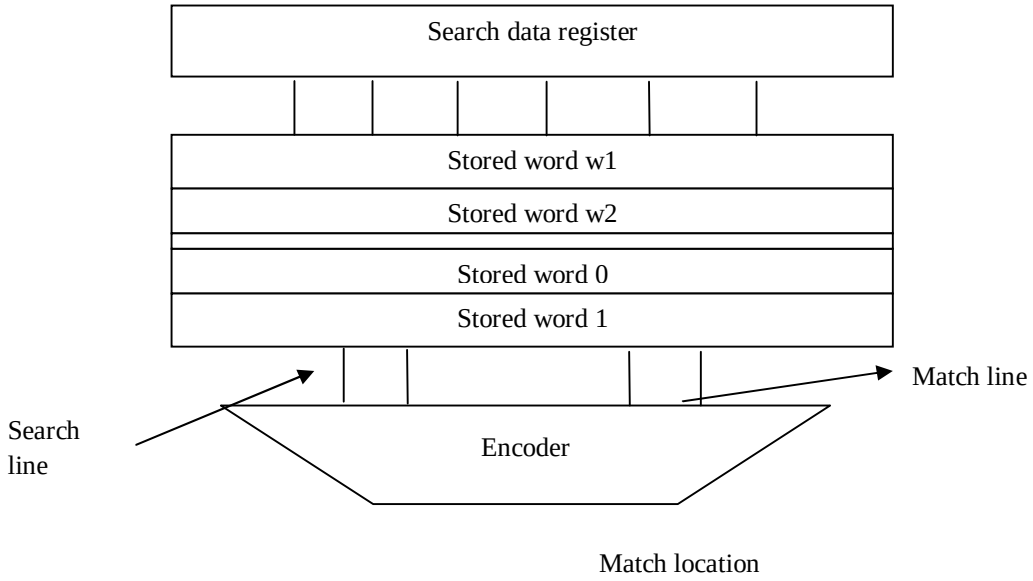

Fig 1. Conceptual view of CAM containing stored words

II. LITERATURE REVIEW

A. *Using Cache To Reduce Power*

C-CAM uses caching to save power in CAM. Simulation and early test chip measurements that has a cache added to a 32k CAM can save as much as 80% of power consumption for hit rates of 90%. Even hit rates as low as 50% the power savings are still 40%. C-CAM that use cache to save power in CAM.

B. *Match Sensing Using Match-Line Stability*

A match-line (ML) sensing scheme that distinguishes match from a miss by shunting every ML sensing fixed with a negative resistance, then exciting the MLs with an initial charge and subsequently observing their voltage developments. It has the voltage on the matched ML will grow to VDD as in an unstable system, and then the voltage on a missed ML sensing will be a decay to zero in a stable system. The initial excitation charge on the ML's can be as low as the noise level in the system it approach the minimum possible energy consumption level for match-line sensing. In CMOS 0.18m a 144 ternary CAM array that includes the stability-based sensing scheme along with two previously-reported sensing. The measured results that confirms the power savings of the already used sensing. The CAM including a pipelined search-line (SL) architecture that can reduce the SL portion of CAM power by up to 50%. Two techniques for reducing CAM power is stability based match sensing scheme and pipelined SL driving. In stability-based sensing, the system stability of the MLs to minimize the amount of energy delivered to mismatch MLs.

C. *A Tutorial And Survey*

A CAM is memories that will implements the lookup-table function into a single clock cycle using desired comparison circuitry. CAM used in network routers for packet classification and packet forwarding, but they are also useful in a variety of other applications that require high-speed lookup table. The main CAM challenge is to reduce power consumption respect to the large amount of parallel active circuitry, without sacrificing speed or memory density. CAM circuits and architectures, an emphasis on high-capacity CAM. CAMs can be applied to the packet forwarding in network routers. The approach for driving search lines, and the power saving which eliminate the search line pre-charge or employ hierarchical search lines. This sensing scheme reduces the ML power by 50% compared to the current-race scheme, and by 30%.

D. *Error –Correcting Match Scheme*

A binary content-addressable memory (CAM) design has the high immunity to SEUs. Conventionally, error-correcting code has been used in SRAM to address this section, but these techniques are not immediately applicable to CAMs because they mostly

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depend on processing the full contents of the memory word outside the array, which is not possible in a normal CAM. An error-correcting-match scheme for CAMs is tolerant to bit errors in the stored contents. The scheme adds parity bits to each search word and modifies the MLSA, so that matches and 1-bit misses constitute a successful search word, and all other process constitute an unsuccessful search.

E. A Mismatch-Dependent Power Allocation Technique

An equal power is consumed to determine whether if a stored word is matched to a search word and mismatched some independent of the number of mismatched bits. The ML sensing allocates power to match decisions based on number of mismatched bits in each CAM word with allocating less power to mismatched MLs and with most MLs beings, these results in a considerable power reduction. The scheme was implemented in a 265 144-bit TCAM for a 0.13- m 1.2-V CMOS logic process. For the use of a 2-ns search time on a 144-bit TCAM word, the scheme uses 60% less power compared to the conventional pre-charge-high NOR scheme and 40% compared .

III. PROPOSED SYSTEM

A. Search Speed Boost Using A Parity Bit

A versatile auxiliary bit to boost the search speed of the CAM at the cost of less than 1% area overhead and power consumption 1-mismatch ML waveforms of the original and the architecture with parity bit during the search operation. This introduced auxiliary bit at a glance is similar to the existing Pre-computation schemes, but it has a different operating principle.

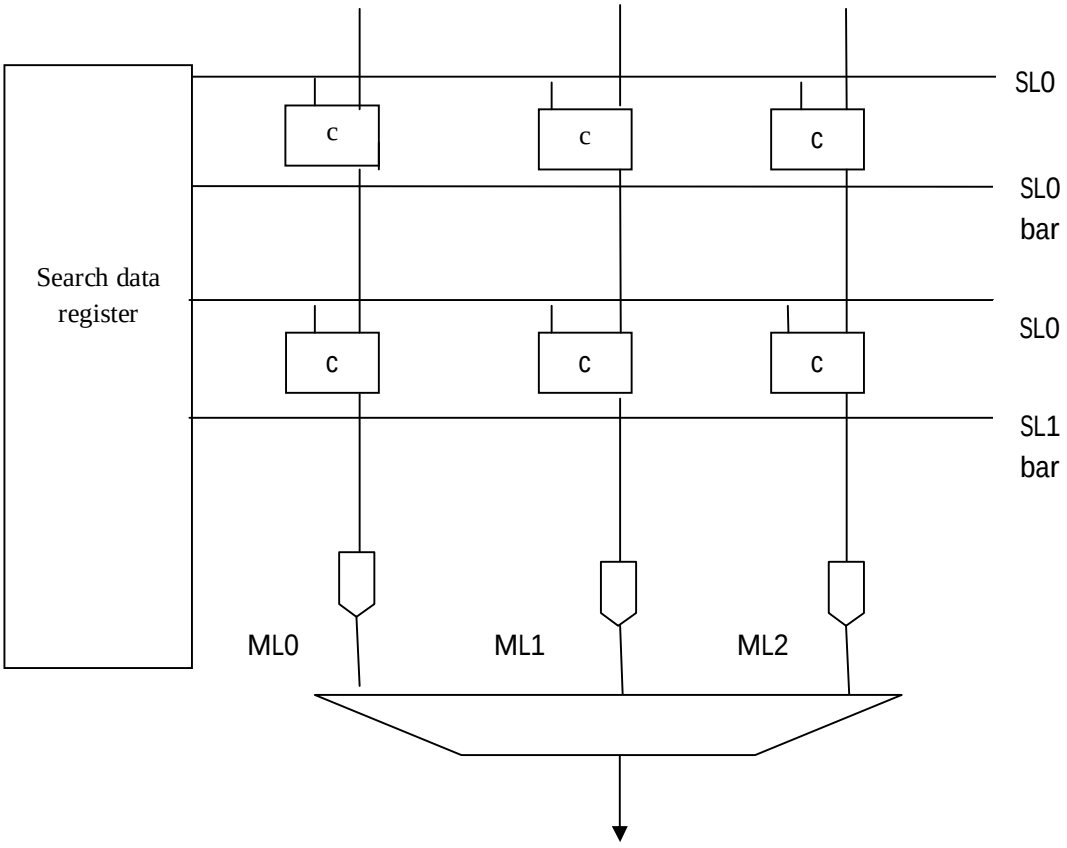

Fig 2. Schematic model of CAM

B. Pre-Computation Cam Design

The pre-computation CAM use additional bits to filter various mismatched CAM words before the actual comparison happen. These extra bits are derived from the data bits that are used as the first comparison stage. The ML sense amplifier has to distinguish between the matched ML and the 1-mismatch ML. That makes CAM designs sooner or later face challenges, since the driving

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strength of the single turned-on path is gets weaker after each process generation when the leakage is getting stronger. This issue is usually referred to as Ion=Io. Thus, it shows that a new auxiliary bit that can concurrently boost the sensing speed of the ML at the same time improve the Ion=Io of the CAM by two times.

C. Cell Variant

The NOR cell variant uses 9-transistors related with the 10-T NOR cell. The bit comparison uses pass transistors (in the previous 9-T NAND type CAM core cells variations for 9-T NOR-type CAM and 10-T NAND-type CAM). The cells are using SRAM-based data-storage cells.

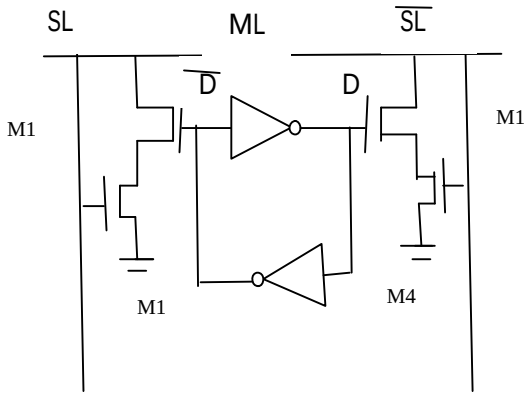

Fig 3. Cell Variant

D. Ternary Cell

Cells store either “0” or “1” in logic sequence. Ternary cells store as a “X” value. The “X” value represented as don’t care condition that represents both “0” and “1”, allowing an additional wildcard operation. A ternary symbol can be encoded into two bits. It represents two bits as D and D [BAR]. Shows that although the D and are not necessarily complementary and its complementary notation for consistency with the binary CAM cell. Two bits can represent 4 possible states and the ternary storage requires only three states, it disallow the state where D and are both zero.

Table 1: Ternary Cell

STORED VALUE	STORED		SEARCH BITS	
	D	D(BAR)		
0	0	1	0	1
1	1	0	1	0
X	1	1	0	0

E. Parity Bit

A parity bit, or check bit is added to the end of a string of binary code that indicates whether the number of bits in the string with the value of one is even and another one is odd. Parity bits are used as the simplest form of error detection code process. These two variants of parity bits are even parity bit and odd parity bit. In even parity, the parity bit is set to 1, if count of ones in a given set of bits is odd, making count of ones in the entire set of bits even. Then the count of one is assigned as even and it is set to a 0. While using odd parity that refers the parity bit is set to 1 if the count of one is assigned as even then the count of ones in the entire set of bits odd.

F. Parity Bit Based Cam

The parity bit based CAM design consisting of original data segment and an extra one-bit segment derived from actual data bits. The obtained parity bit is placed directly to the word. Then the new architecture has the same interface to the conventional CAM with one extra bit. During the search process, there is only one single stage as in CAM. Hence, the use of these parity bits does not

improve the power performance.

G. Gated-Power Ml Sense Amplifier Design

Each cell has the same number of transistors as the conventional P-type NOR CAM and it uses a similar ML structure.

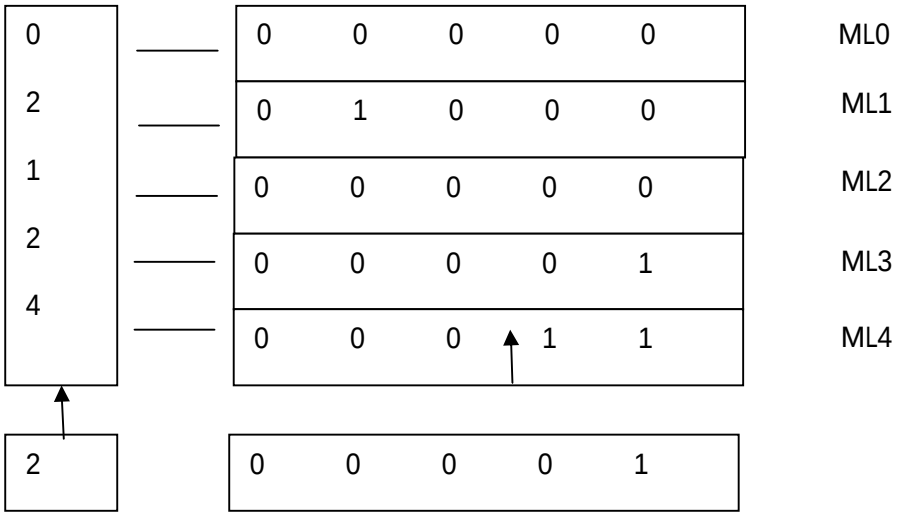

Fig 4. Data register

H. Temperature Variation Analysis

The temperature variation analysis on the four designs it can be seen is the most vulnerable design and thus can work only in a narrow range of temperature variation. Throughout the whole temperature range having more than 30% speed fluctuation. In contrast, conventional design is much more stable with less than 4% of sensing delay variation.

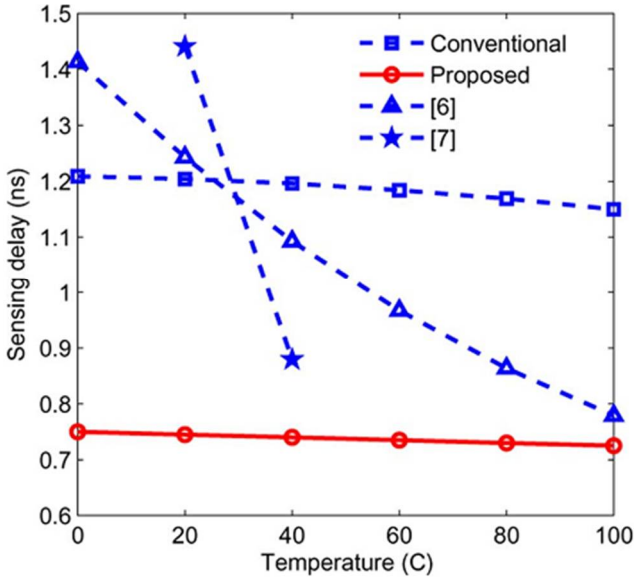

Fig 5 . Temperature Analysis

IV. RESULT AND DISCUSSION

This figures shows that the RTL viewer of the CAM. It clock, we, Data [7, 0] and both the read and write address of 4 bits

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respectively then the clock will be feedback for the enable of the output. Q [7, 0] is obtained.

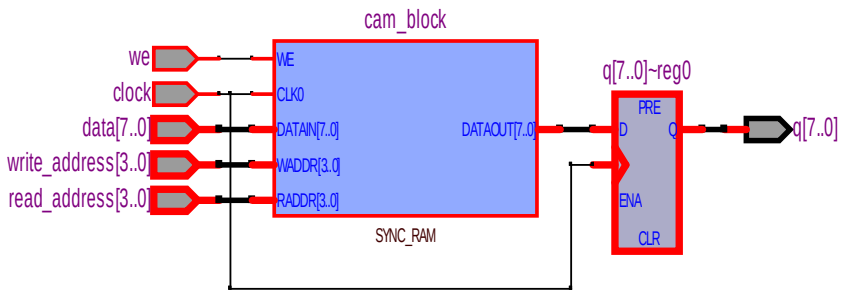

Fig 6. RTL Viewer

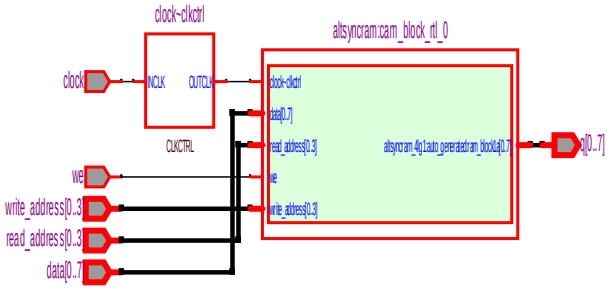

Fig 7. Map Viewer

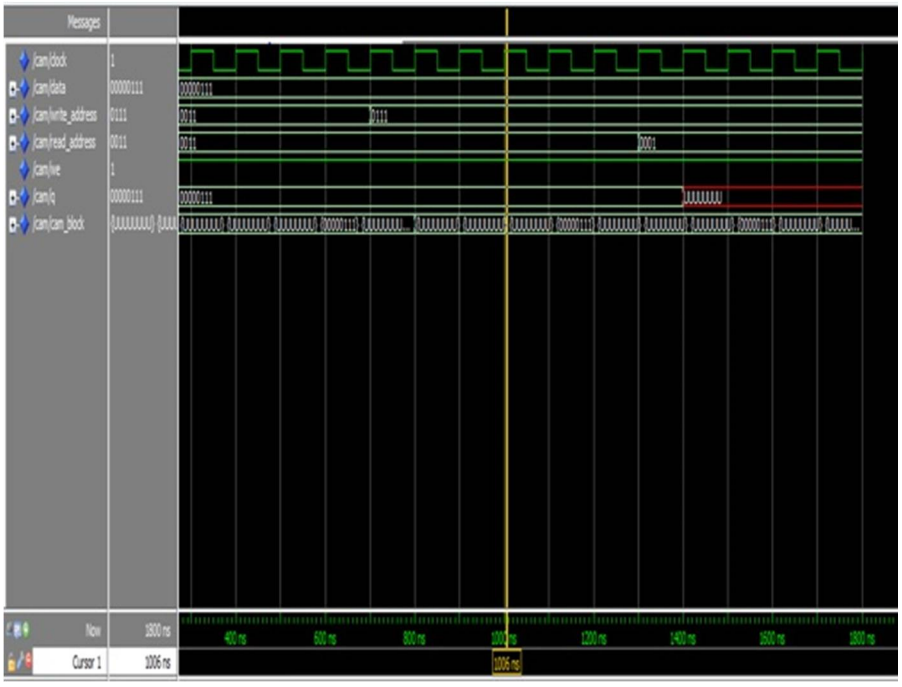

Fig 8. Simulation Result

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A. Power Analysis

Table 2: Power analysis

Power	I(mA)	P(mA)
Total estimated power		
Vccint1.20V	65	78
Vccaut2.50V	8	20
Vcco25 2.50V	2	4
clock	0	0
inputs	0	0
logics	0	0
output		
Vcco25	0	0

V. CONCLUSION

An effective gated-power technique and a parity-bit based architecture offer several advantages it reduced peak current with average power consumption (36%) & boosted search speed (39%) improved process variation tolerance. It is much more stable than recent designs while maintain their low-power consumption property. When related to the conventional design its stability is degraded by 0.6% and only at extremely low supply voltages. At the rate of 1V operating condition both designs are equally stable with no sensing error simulations. Its area overhead is 11% it is best design for implementing high capacity parallel CAM in sub-65-nm CMOS technologies.

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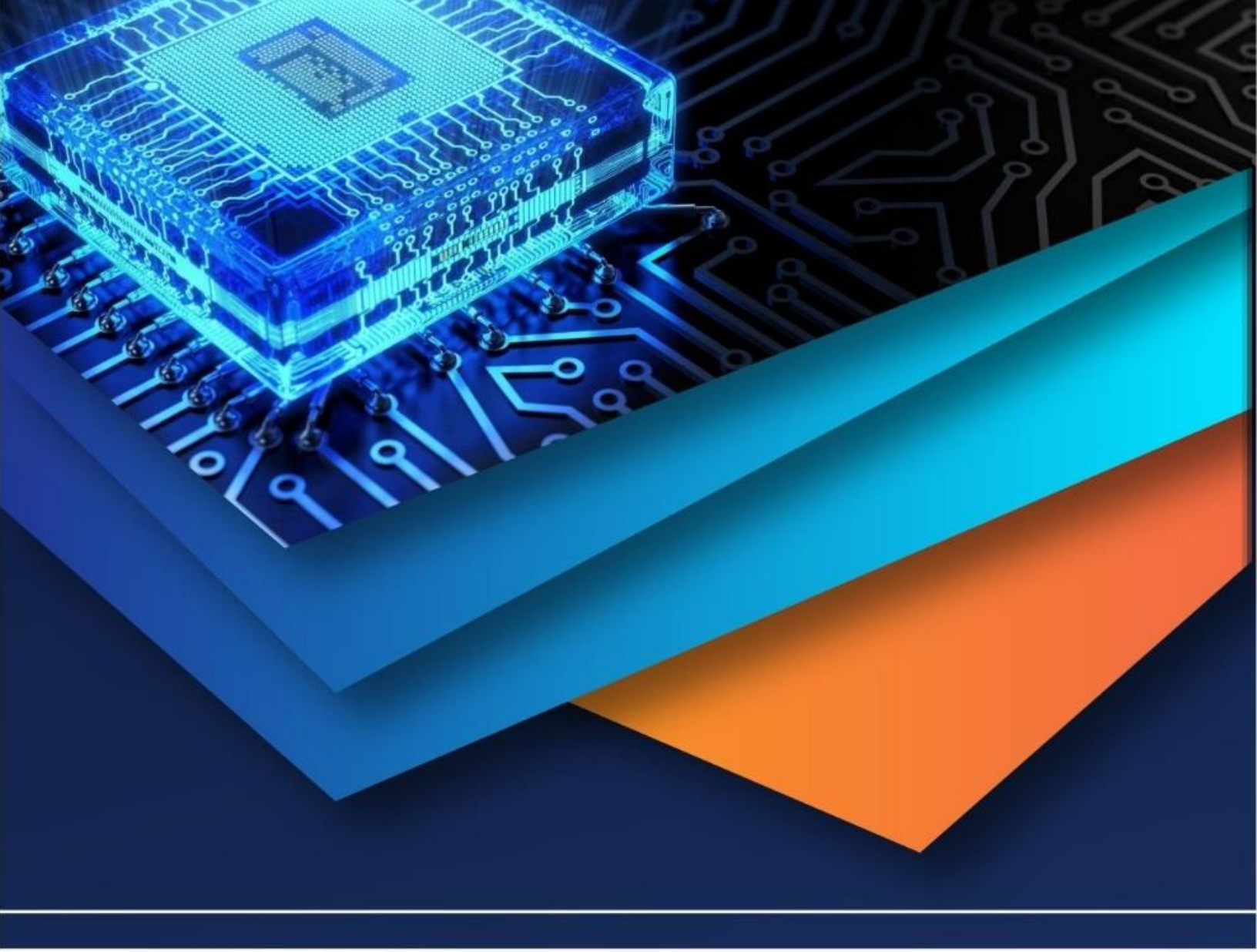

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