iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 4 **Issue:** XII **Month of publication:** December 2016

DOI:

www.ijraset.com

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Volume 4 Issue XII, December 2016
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

Skew Managed Global Clock Network Using Type Matching

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Abstract*—Clock gating has emerged as an effective low power technique these days. Various researches are being made in the optimization of this technique. While clock gating finds its applications in the clock tree synthesis, it's crucial that this additional circuitry does not include skew to the entire chip design. Also when the clock gating involves the use of all gates, (i.e.) NAND, NOR which has different timing behaviours, there is a definite possibility of an increase in skew. Therefore, in this paper a global clock tree design called type matching is proposed, wherein same type of gate at every level of clock tree is maintained, replacing even the buffers with the same type of gate buffers with the proposed mechanism. Also a comparison on the normal clock gated tree and type matched clock tree is done and proved that the clock skew minimization is achieved in type matched clock trees at the cost of clock tree area and power consumption.

Keywords*— Clock tree, Skew, Type matching, Clock gating.

I. INTRODUCTION

One of the most extensively used techniques for dropping dynamic power is clock gating, a number of techniques to diminish the dynamic power have been urbanized, of which clock gating is predominant. Clock gating is a popular technique used in many synchronous circuits for reducing dynamic power dissipation. Clock gating saves power by adding more logic to a circuit to clip the clock tree. Clipping the clock disables portion of the circuitry so that the flip-flops in them do not have to switch states. Switching states consumes power. When not being switched, the switching power consumption goes to zero, and only leakage currents are acquired. Clock gating works by taking the enable conditions attached to registers[7] and utilizes them to gate the clocks. This clock gating process can also save significant die area as well as power, since it removes large numbers of multipliers and replaces them with clock gating logic. This clock gating logic is generally in the form of "Integrated Clock Gating" (ICG) cells[2]. Here the symmetric clock tree is used. All flops of a symmetric clock tree, traced back from the clock tree root are passing the same number of levels and the same cell references at each level. The clock tree is balanced at a specific corner which should fit all corners.

II. PRACTICAL METHODS TO IMPLEMENT CLOCK GATING

A. By the addition of enable into the RTL code in such that it can be implemented into clock gating.
B. RTL designers can directly include the clock gating cells in to design circuit.
C. By the usage of tools like Cadence SoC Encounter, CTS (Clock Tree Synthesis) we can include clock gating in designs.

III. GATED CLOCK TREE

Very often we have the possibility that only a portion of the circuit is active. Therefore, clock gating is an efficient technique to drastically bring down the power consumption.

Making use of the below clock gating circuit in Fig.1, different types of gated clock trees can be designed. A normal clock gating circuit consist of a latch usually D – latch, which is preceded by any gate of the designer's choice. This latch is being added to the circuit such that it can boost the signals so that the clock gating is efficient.

By the use of the above explained clock gating design, the normal gated clock tree can be formed as in fig 2.This design[5], as it is evitable that the area it occupies is small, but the skew is obviously added in addition to the design's skew.

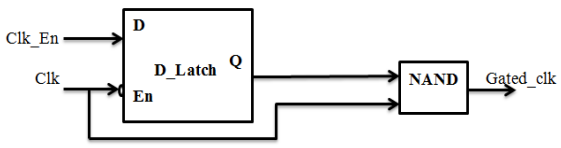

Figure 1: Clock Gating Circuit

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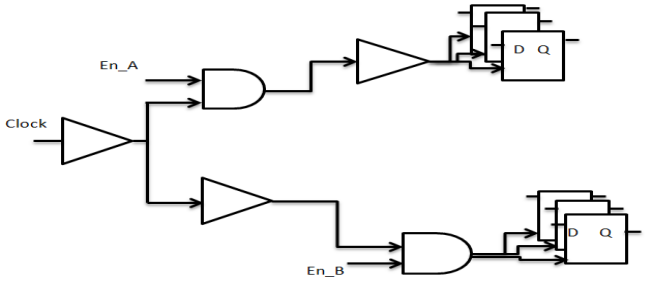

Figure 2: Normal Clock gating circuit

IV. TYPE MATCHING CLOCK TREE

The main alteration that has to be done in a type matched tree design is that, the design of the logical buffers [1]. These logical buffers can be designed in contrary of the buffers which are to be replaced as the same type of gates. In this way, we have the different gate buffers according to the controlling values of the universal gates. The possibility of type matching is proved with the help of two lemmas provided below.

Lemma 1: Any clock control logic can be implemented using only NAND gates.

Lemma 2:Any clock control logic can always be transformed to type-matching clock tree.

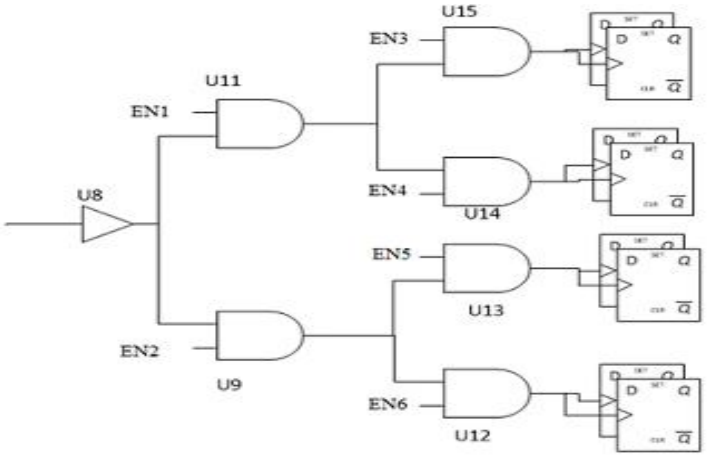

Figure 3: Type matched clock tree

V. BLOCK DIAGRAM OF THE PROPOSED DESIGN

The mechanism in which the proposed design works is given by means of a block diagram in Fig.4.

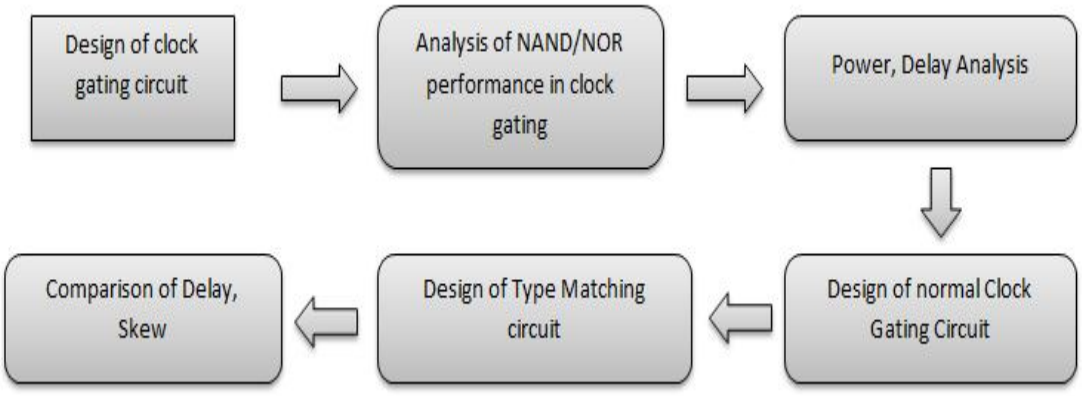

Figure 4: Block diagram of the proposed design

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VI. DELAY AND POWER EVALUATION OF THE CLOCK GATING CIRCUITS

The proposed idea was designed by means of the results analysed from the H-Spice on the clock gating circuits using two types of the universal gates, NAND/NOR[3]. From the results, it is evident that the clock gating circuit involving NAND has less delay (i. e) skew, and therefore the type matched clock tree was designed with the NAND gate. On the other hand, the normal clock gated tree was also designed with the help of the buffers and NAND gates. Finally, the two circuits were simulated using TANNER, and the further analysis was done with the help of H-SPICE and the results are tabulated in the next section.

VII.SIMULATIONS AND EXPERIMENTAL RESULTS

The normal clock gating circuits using NAND, NOR were simulated and verified using TANNER tool. The same architectures were analyzed using HSPICE for its power, delay. Then the normal and type matched gated clock tree were simulated using TANNER and it was verified using HSPICE for its skew. From the table 1, it is evident that the clock gating circuits involving NAND gate[6] produces less delay when compared to the other. Hence the NAND gate was used in the clock gating circuitry. In addition, the H-SPICE signifies that the type matching technique holds good when designed with the NAND gates rather than using various types of gates in different levels of the clock tree design.

Table 1: Simulation results

Circuits	Power	Delay(s)
Gating circuit using NAND	4.225967mw	6.6853E-11
Gating circuit using NOR	2.707036mw	5.0528E-07
Normal gated clock tree	4.939207w	3.8754E-02
Type matched clock tree	8.664184w	4.5936E-04

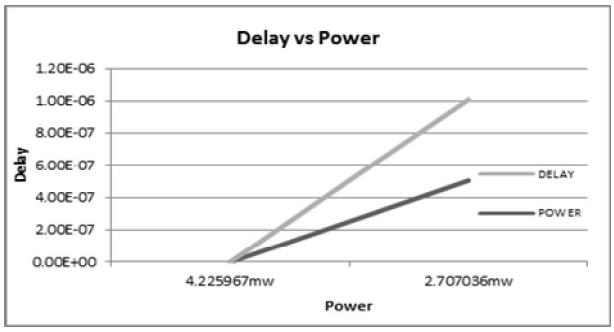

Figure 4: Delay of NAND, NOR as a function of power

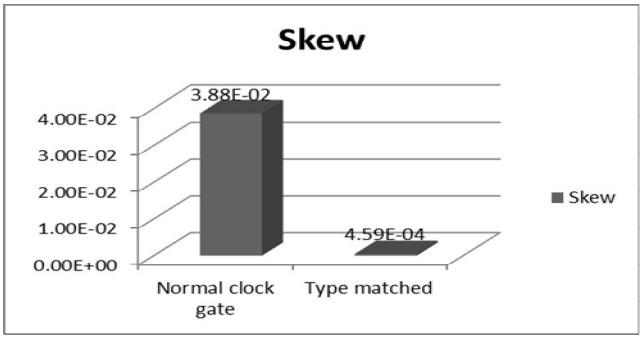

Figure 5: Skew of normal gating and type matched clock tree

VIII. CONCLUSION

In the clock gating circuit, the efficiency of using NAND, NOR gates are analyzed and based upon the results, a global clock tree network involving gating circuits is designed with the new proposed method called type matching circuits. The circuit is compared with the normal clock gated tree and found that it can significantly reduce the clock skew in every process corner with a small penalty on the clock tree area and the clock tree power consumption. This type matched circuit can be used instead of industry strength gated clock tree.

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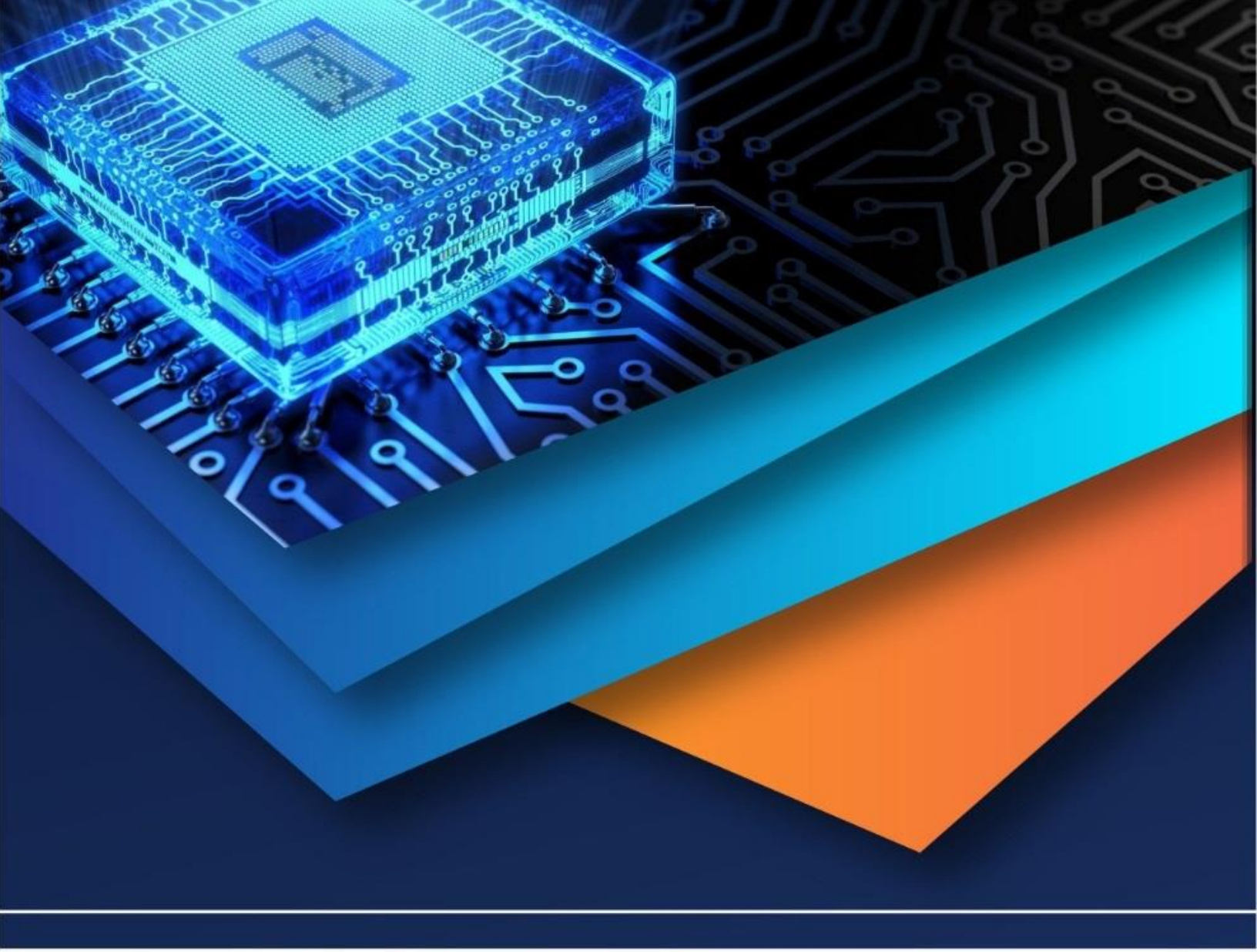

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