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Design of Low Power Double Edge Triggered Phase Detector for DLL Clock Generators

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Abstract--A DLL based double edge triggered phase detector (DET-PD) is proposed for a clock generator in low power systems. The phase detector plays a vital role in DLL clock generators. To reduce the power consumption, the phase detector is designed by combining both the edges of the clock pulse. The phase detector is designed by Truly Single Phase Clock (TSPC) delay flip flop (DFF) logic which has a faster locking speed. The operating frequency of the design ranges between 250MHz-800MHZ. The design is implemented in 180nm and 65nm CMOS process technology and the average power consumed is6.26mW and 3.92mW respectively.
Keywords--DLL, DET-PD, TSPC, DFF

I. INTRODUCTION

Low power consumption is always desired for any electronic products today. Demand for modern measurement systems in CMOS process introduce new challenges in design of low power clock generation systems. With the rapid growth in the digital systems the clock generation becomes a very important constraints. The clock generator is implemented using Delay Locked Loop(DLL) and Phase Locked Loop (PLL). PLL based clock generators can easily change the output clock frequency, but they have the problem of noise accumulation at the output due to the use of voltage controlled oscillators (VCO). The DLL overcomes this problem by using voltage controlled delay line (VCDL), and has better jitter performance. Compared to PLL, DLL is simple to design with first order system, more stable and less jitter accumulation, while PLL is a higher order system and more unstable [7]. There are three types in DLL clock generators analog, digital, mixed mode. The analog DLL clock generators are widely used because of their better jitter performance and they do not suffer from quantization error [11].

II. BLOCK DIAGRAM AND DESCRIPTION

A conventional DLL clock generator, as shown in Fig.1 has four main blocks. The voltage controlled delay line (VCDL) consist of several delay cells (inverters) connected in cascade. The delay cells can be increased to increase the frequency range of delay line. The reference clock, ref_clk drives the input to the VCDL. The output of the VCDL is given to the phase detector(PD), which determines the phase alignment error. The phase detector compares the phase difference between the ref_clk and VCDL_out signal which is the output of the VCDL line[13]. There are two main types of phase detector level sensitive phase detector and edge sensitive phase detector. The level sensitive phase detector uses XOR gate. The edge sensitive phase detector uses D flip flop.

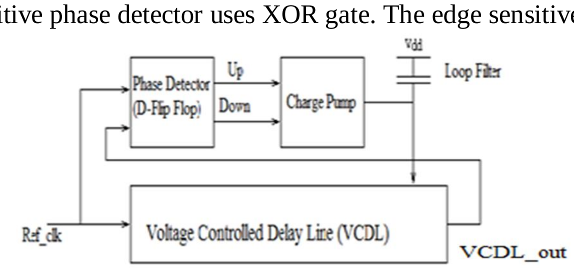

Fig 1. Conventional DLL clock generator

III. PROPOSED ARCHITECTURE

A. Voltage Controlled Delay Line(VCDL)

The various architectures used in the designing of delay cells for voltage controlled delay line falls into two groups: full swing and partial swing. Delay cells are designed using current starved model which fall into full swing group. The VCDL built with current starved inverter model is used to minimize the sensitivity to supply and substrate noise. Working frequency, power dissipation, output voltage are the main design limitations of VCDL. The basic current starved inverter model is shown in Fig 2. The DLL uses

VCDL rather than the VCO since the noise in the voltage controlled delay line does not accumulate over
many clock cycles, hence it is preferred to be used in many cases. It also offers a faster locking time, which allows a system to reduce the wait time required before it can operate. The voltage controlled delay line (VCDL) consist of several delay cells (inverters) connected in cascade.

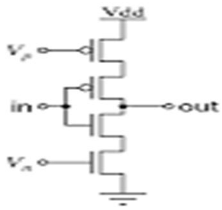

Fig 2. Conventional Current Starved Delay line model.

To control the delay of the inverter two extra transistors are added. This is called current starving technique. Lowering V_n and making V_p high increases the effective drive resistance of the inverter and thus increases the delay. The inverter is designed to limit the current sourcing and sinking capability of the inverter by adding current source and current sink in series with the upper PMOS and NMOS of the inverter. The proposed architecture of VCDL is shown in Fig 3. The control voltage V_{ctrl} is applied to a series connected element. The phase difference provided by each segment of VCDL depends on the delay of each inverter.

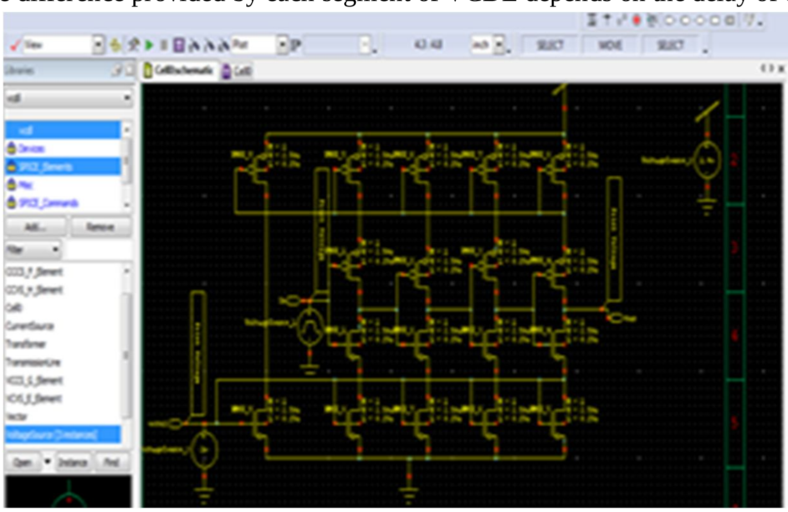

Fig 3. VCDL Architecture

B. Phase Detector

The phase detector used two D- flip flops where the reference ref_clk and VCDL signal VCDL_out which has to be compared enters as clock inputs. The UP and DOWN signals are the output of the flip flop which are given to the NAND gate. The NAND gate output is given as reset input R to both the flip flops. The block diagram of the phase detector is shown in the Fig 4. The phase detector has the probability of working in four states.

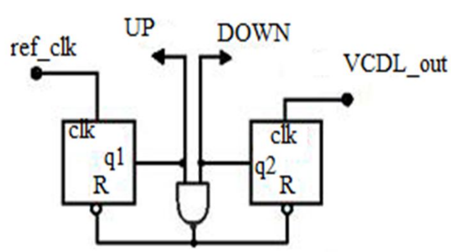

Fig 4. D-flip flop based Phase detector

C. Single Edge Triggered Phase Detector

The single edge triggering phase detector (SET-PD) commonly uses flip flop design where the data is processed at either the positive or negative edges of the clock pulse. The phase detector is designed using Truly Single Phase Clock (TSPC) logic. The TSPC logic based flip flop reduces the transistor count and power consumption of the circuit.The schematic of Positive Edge Triggered (PET) phase detector is shown in Fig 5.The NOR gate is used to reset the flip flop when both UP_PET and DOWN_PET signals are at logic 0 the flip flop gets reset. If the raising edge of the ref_clk leads the VCDL_out signal then the UP output goes high. If the VCDL_out leads the ref_clk then the DOWN output goes high. If both remains low then the UP and DOWN signals will also be at logic low. TSPC logic of Negative Edge Triggered (NET) phase detector detects the phase error at the negative edge of the clock pulse. Herein NOR gate is used to reset the flip flop. The flip flop is rest when both the UP_NET and DOWN_NET pulses are at logic 0. The schematic of NET-PD is shown in Fig 6. The negative Edge Triggered (NET) requires nine transistor. The inverter and inverter delay compensation circuit are added in the negative edge triggered flip flop to avoid the gain mismatch.

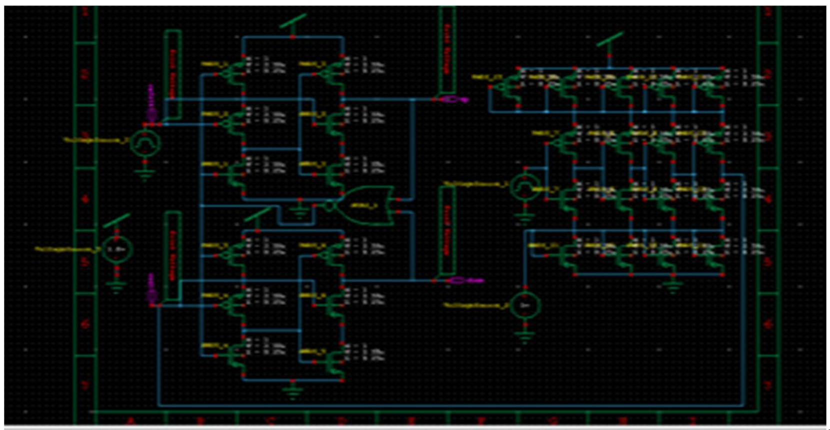

Fig 5. Positive Edge Triggered Phase Detector

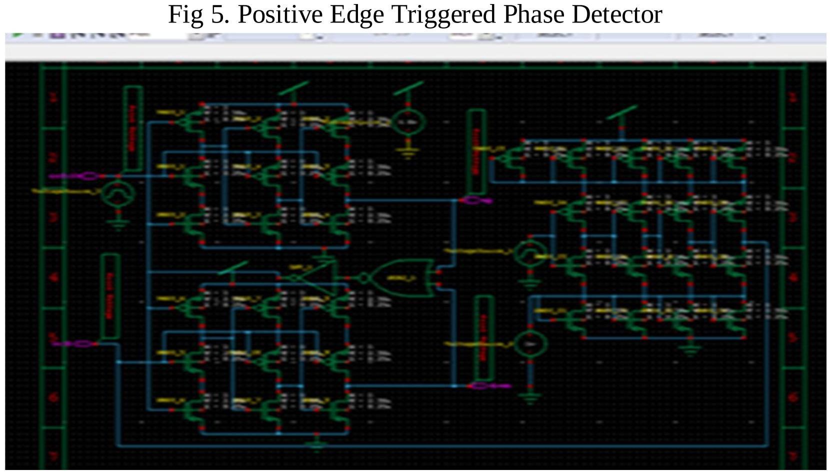

Fig 6.Negative Edge Triggered Phase Detector

D. Double Edge Triggered Phase Detector

The DET-PD effectively reduces the power on the clock network. To improve the lock performance of the clock generator, the ref_clk and VCDL_out signals are compared at both the positive and negative edges. A Double Edge Triggered Phase Detector achieves the same throughput with half the clock frequency compared to the single edge triggered phase detector. The schematic of DET-PD is shown in Fig. 7.The signals from the PET phase detector and NET phase detector are combined using merging circuit,which consist of two NAND gates. One NAND gate combines the UP pulses of PET and NET phase detector. The other NAND gate combines the DOWN pulses of PET and NET phase detector. Since the DET phase detector has the characteristics of the TSPC flip flop it has a wide capture range. The tuning precision of the DLL depends on the characteristics of the phase detector. The widths of the UP and the DOWN pulses are proportional to the phase difference between the inputs.

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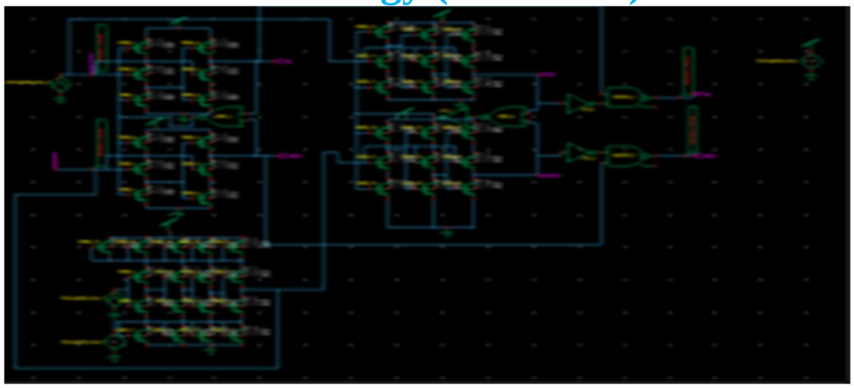

Fig.7 Double Edge Triggered Phase Detector

If the rising edge of the clock and leads the VCDL rising edge, the UP output of the phase detector goes high while the DOWN output remains low. If the VCDL signal leads the clock, UP remains low while the DOWN goes high and we can find the phase difference between VCDL and clock. In locked state, the both UP and DOWN output remains low.

IV. SIMULATION RESULT

The design of VCDL,TSPC based SET-PD and DET-PD are simulated using Tanner EDA 180nm and 65nm CMOS process technology, with a supply voltage of 1.8V and 1V respectively. The frequency of operation for the design is 500MHz. Fig. 8(a) shows the VCDL output. The reference clock leads the VCDL output by 30 degree.

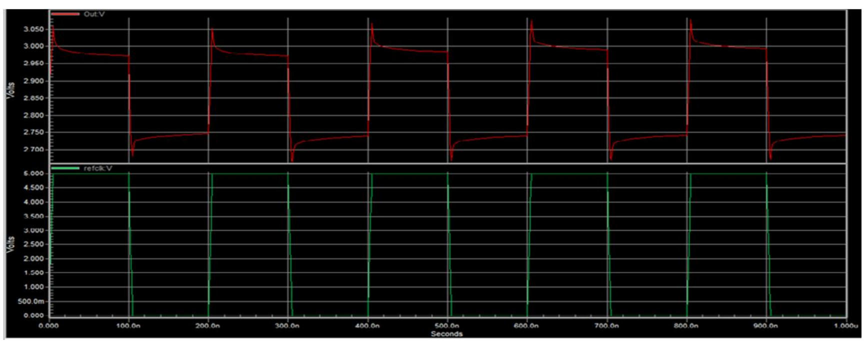

Fig.8(a) VCDL Output

In DET-PD the edge sensitivity problem have to be fixed so as to remove the multiple lock position while pulse merging the outputs. To overcome the dead zone problem the reset pulse gets slender in the phase locked region which provides sufficient time for the UP and DOWN signals to make the charge pump switch completely for very small phase differences. The simulation result of Positive Edge Triggered Phase Detector is shown in the Fig.8(b)

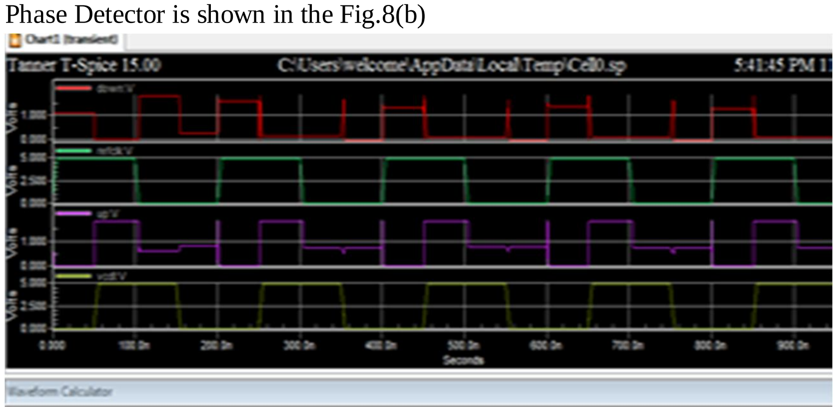

Fig. 8(b) Positive Edge Triggered Phase Detector

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The simulation result of Negative Edge Triggered Phase Detector is shown in Fig.8(c). The NET-PD has the characteristics of the TSPC flip flop design, it has a wide capture range. It produces a large flat gain when the delay difference is twice larger than the liner gain.

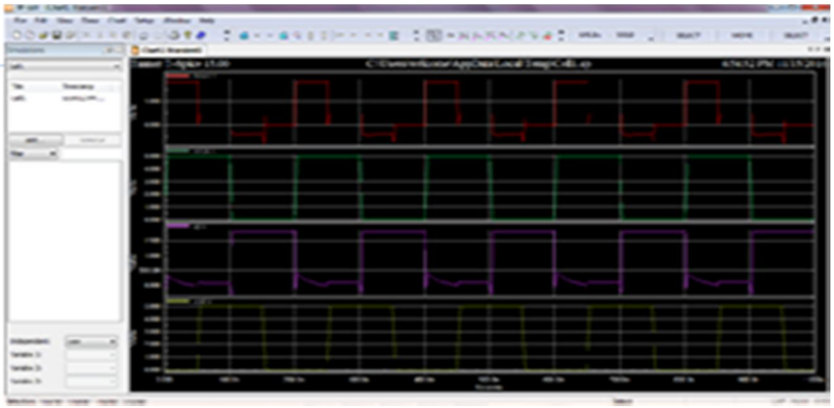

Fig. 8(c) Negative Edge Triggered Phase Detector

The simulation result of Double Edge Triggered Phase Detector is shown in Fig.8(d). To overcome the dead zone problem the reset pulse gets slender in the phase locked region which provides sufficient time for the UP and DOWN signals to make the charge pump switch completely for very small phase differences. The signals from the PET-PD and NET-PD are combined into one signal at the pulse merging circuit which is composed of two NAND gate.

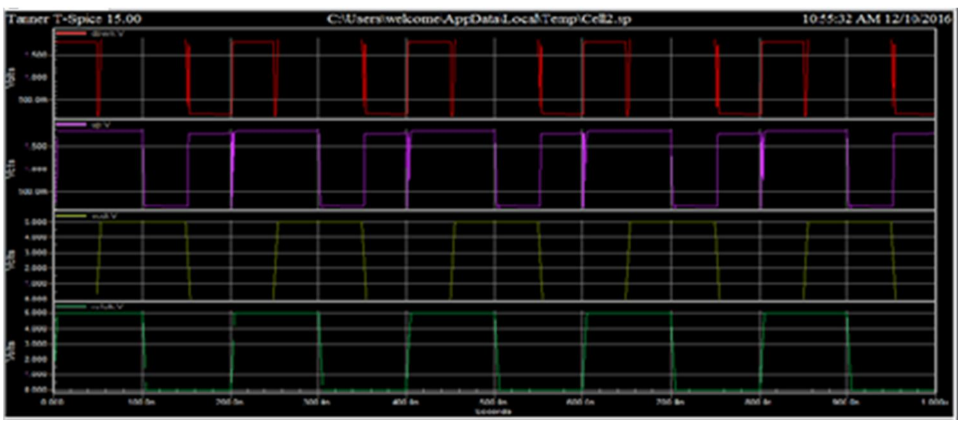

Fig.8(d) Double Edge Triggered Phase Detector

V. PERFORMANCE ANALYSIS

CMOSTech.	PET-PD	NET-PD	DET-PD	Frequency	Supply Voltage
180nm	8.9mW	8.22W	6.29mW	500MHz	1.8V
65nm	5.63mW	4.05W	3.919mW	500MHz	1.3V
32nm	4.32mW	3.32mW	2.33mW	500MHz	1V

Table 1 Performance Analysis of Phase Detector

VI. CONCLUSION

The clock distribution network has huge contribution in DLL design, by using the DET technique the power consumption is significantly reduced. The DET clock generator reduces the frequency to half while keeping the same throughput. The frequency range of analog DLL is increased by using the delay cells. The power consumption of DET phase detector is found to be 6.292mW for 180nm CMOS process and 3.919mW for 65nm CMOS process and 2.33mW for 35nm technology. The phase detector is designed to operate at a frequency of 500MHZ.The speed of the circuit operation is also increased by DET technique. The power consumed by double edge triggering technique is 32% reduced compared to conventional single edge triggering technique.

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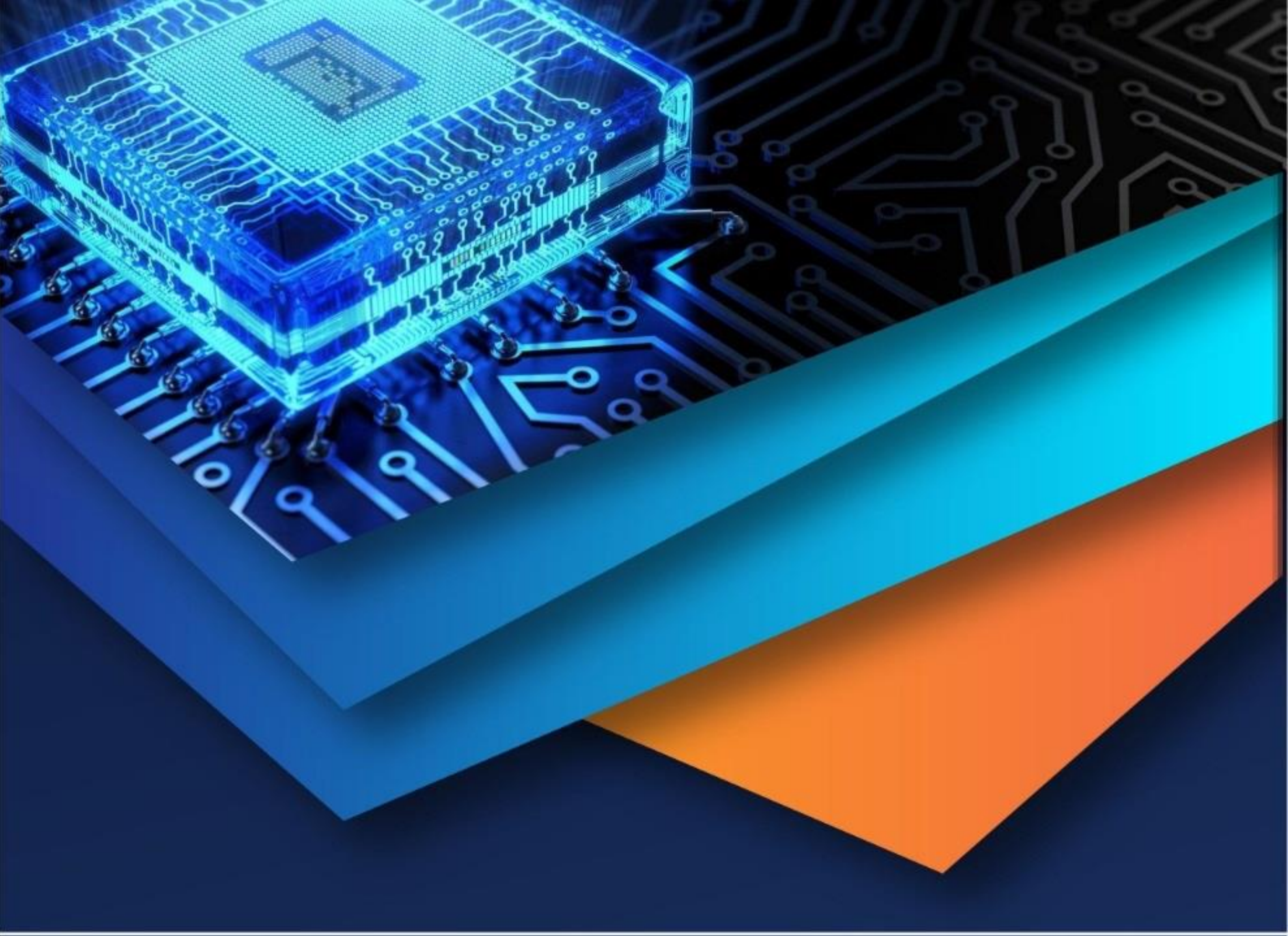

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