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Relaiblity and Fault Analysis in On-Chip Network

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Abstract: ***System on chips towards multicore design for taking advantage of technology scaling and also for speeding up system performance through increased parallelism in the fact that power wall limits the increase of the clock frequency. Network on chip are shown to be feasible and easy to scale for supporting the large number of processing elements rather than point to point interconnect wire or shared buses. As industry moves towards many core chips, network on chips (NOCs) are emerging at the scalable fabric for interconnecting the cores. With power now the first –order design constraint, early-stage estimation of NOC power has been crucially important.***
Keywords: System on chips, parallelism, Point interconnects wire, network on chips.

I. INTRODUCTION

A system on a chip or system on chip (SoC or SOC) is an Integrated Circuit (IC) that integrates all components of a computer or other electronic system into a chip it is a collection of all components and subcomponents of a system on to a single chip. This revolution in design had been used by many designers of complex chips, as the performance, power consumption, cost, and size advantages of using the highest level of integration made available have proven to be extremely important for many designs.
Typically cores are the hardware description of today's standards ICs: digital signal processor, RISC processor or DRAM core. They also use an unprecedented range of technologies, from CMOS logic to DRAM to analog circuits. Cores sometimes come in hierarchical compositions; these so called complex cores incorporate one or more simple cores. Cores come in a range of hardware description levels, categorized as soft (register transfer level), firm (net list), and hard (technology dependent (layout).These three types offer trade off opportunities. Soft core leave much of the implementation to the designer but are the flexible and process independent. Hard cores have been optimized for predictable area and performance of chip, but lack flexibility. However, the practical implementation of the cores based design scenario is fraught with unresolved issues: design methods for building single chip systems; sign off for these systems; and intellectual property licensing, protection, and liability. The most critical challenges of this emerging discipline include manufacturing test and design debug.

II. NETWORK ON CHIP

Network on Chip (NoC) is a new paradigm to make the interconnections inside System on Chip (SoC) system. As SoCs grow in complexity and size, on-chip communication is becoming increasingly important. Furthermore, new classes of optimization problems arise as communication delays and latencies across the chip start dominating computation delays. Therefore, as we enter the network-on-chip (NoC) era, new network-based communication architectures and design flows are needed. Communication design for SoC spy's unique challenges in order to cover a wide range of architectures while at the same time offering new opportunities for optimizations based on the application-specific nature of system designs. The corresponding NoC communication design flow that enables rapid design space exploration through design automation in order to achieve the required productivity gains while supporting a wide range of implementations. In order to automate the NoC design process, a well-defined design flow with clear and unambiguous abstraction levels, models, and transformations is required. The key to the success of this approach are properly defined design models. Arbitrary models without clear semantics do not enable synthesis and verification. Network on Chip are a special case of parallel computing systems characterized by the tight constraints such as resource availability, area and power consumption and cost of the NoC architecture. Many of the currently adopted architectures and protocols derive directly from the distributed computing research area from which NoC are a special case. Each new SoC generation integrates more processing elements (IPs) and offers increased functionality. NoC design flows for ASIC type designs are normally split in several steps as topology selection, mapping, path selection and slot allocation. As prerequisites for NoC design, communication requirements must be derived, and the set of IPs to be connected to the NoC must be specified.

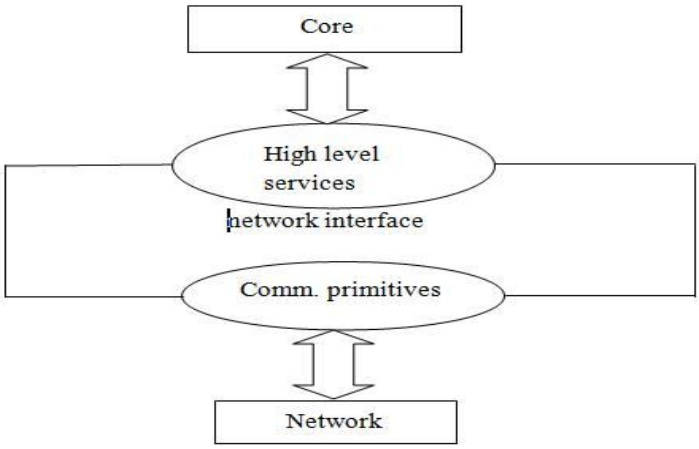


Figure 1 Logical Representation of Network Interface

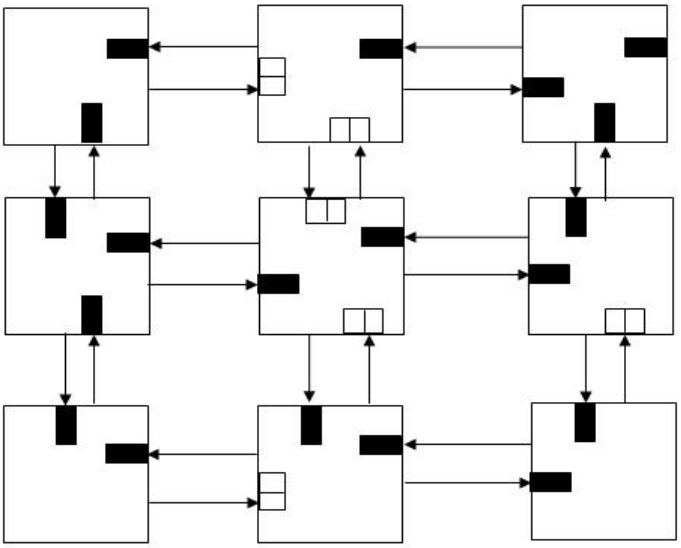


Figure 2 NOC with non-uniform VC configuration

III. LITERATURE SURVEY

It is suitable for both homogeneous cores on regular mesh architecture as well as heterogeneous cores on irregular mesh or custom architecture. The main contribution of this architecture is efficient interconnection matrix that models any task graph and network. Then, task mapping problem is exactly formulated to an MIQP (Mixed Integer Quadratic Programming).They propose two effective heuristics, a successive relaxation algorithm and a genetic algorithm.A3MAP can be the successive relaxation algorithm and genetic algorithm to reduce the amount of traffic in regular mesh, irregular mesh and custom network respectively. So far, most of the NoC based MPSoC targeting general-purposed computing favor a regular mesh network. The regular mesh network lets task-to-tile mapping easier, increases routing efficiency and reduces the complexity of resource management. The irregular mesh network can be also found in a regular mesh network when some links become faulty and degraded by process variation and temperature variation. After the fault and degradation of link are detected, task mapping and routing path allocation should deal with the abnormal links and compensate the loss of yield and performance of the MPSoCs and temperature variation are determined. They use a metric space that exactly captures the interconnection of network and that is simple yet efficient for a task mapping problem in various network. The A3MAP can map a task adaptively to any different sized tile both on a regular/irregular mesh and on a custom network. Given a task graph and a network as inputs, an interconnection matrix that can model any task graph and network along interconnection is generated. Then, task mapping problem is exactly formulated to an MIQP and is solved by two effective

algorithms (i.e.) successive relaxation algorithm and genetic algorithm.

The proposed algorithms for routing without using buffers in router input/output ports. The evaluations show that routing without buffers significantly reduces the energy consumption of the on-chip cache/processor-to-cache network, while providing similar performance to that of existing buffered routing algorithms at low network utilization (i.e., on most real applications). Thus the buffer less routing can be an attractive and energy-efficient design option for on chip cache/processor-to-cache networks where network utilization is low. Interconnection networks are commonly used to connect different computing components. Several NoC prototypes show that NoCs consume a substantial portion of system power. Indeed, buffering within each router improves the bandwidth efficiency in the network because buffering reduces the number of dropped or "misrouted" packets, i.e. packets that are sent to a less desirable destination port. On the other hand, buffering has several disadvantages. First, buffers consume significant energy/power dynamic energy when read/written and static energy even when they are not occupied. Second, having buffers increases the complexity of the network design because logic needs to be implemented to place packets into and out of buffers. Third, buffers can consume significant chip area. In this paper, we propose to eliminate buffers in the design of on chip cache-to-cache and cache-to-memory networks to improve both energy- and area-efficiency, as well as reduce network design complexity and router latency.

IV. EXISTING SYSTEM

Network throughput can be increased by dividing the buffer storage associated with each network channel into several small queues, virtual channels rather than a single deep queue. This decoupling allows active message to pass blocked messages using network bandwidth that would otherwise be left idle.

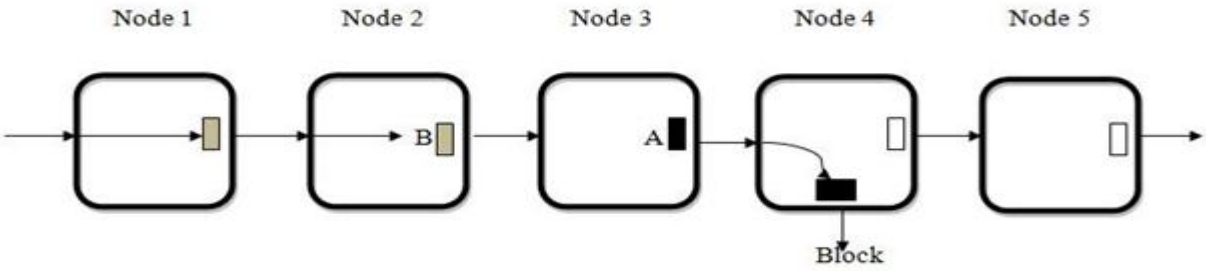
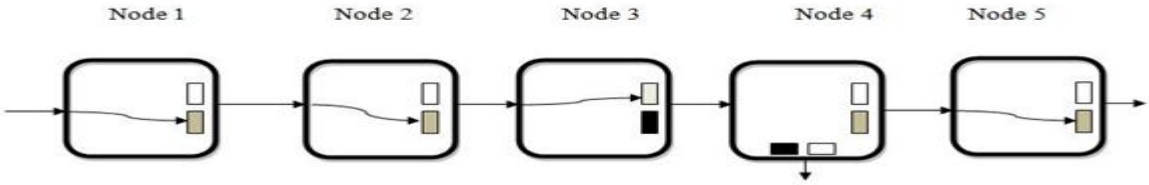


Figure 3 Virtual channel of single buffer



. Fig 4 Extraction of image using ROI descriptor

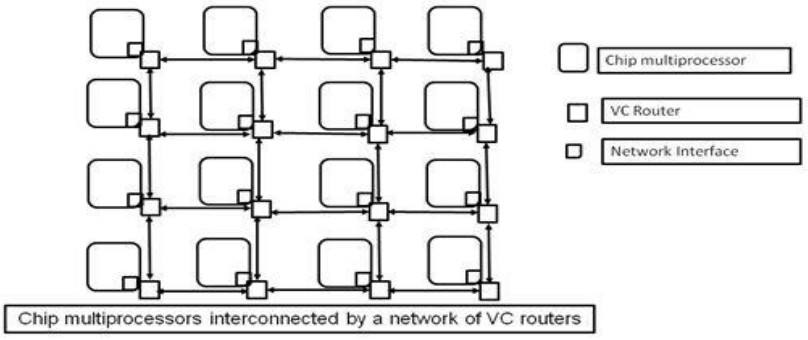


Fig 5 Block diagram of VC router

V. PROPOSED SYSTEM

Router architecture with shared queues based on the idea of Figure shown below. When an input port receives a packet, it calculates its output port for the next router (look ahead routing), at the same time it arbitrates for both its decided output port and shared queues. If it receives a grant from the output port allocators (OPAs), it will advance to its output port in the next cycle. Otherwise, if it receives a grant to a shared queue, it will be written to that shared queue at the next cycle. In case that it receives both grants, it will prioritize to advance to the output port.

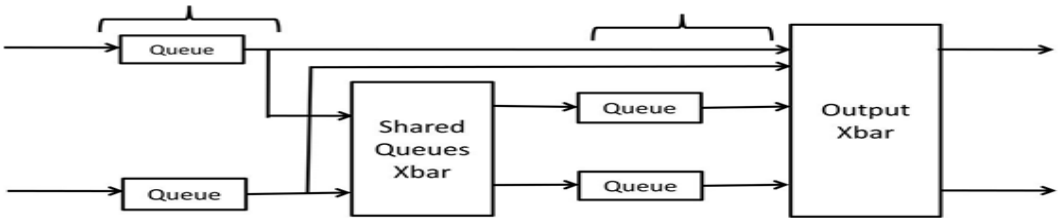


Figure 6 Proposed system block diagram

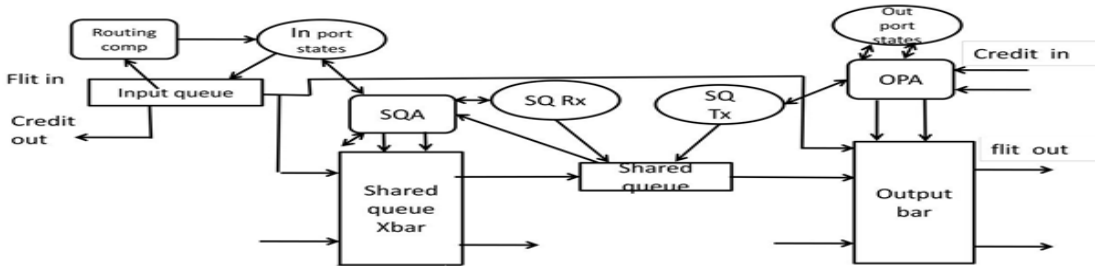


Figure 7 Prediction of fundus flavimaculatus for affected eye

. VI. RESULTS AND DISCUSSIONS

The following diagram shows the basic steps for simulating a design within a model sim project. First the modelsim should be start and then create the project then add files to the project or add the existing files to the project that is programs then compile the design files then run the program and determine the simulated result which is shown in the figure 5.1.according to the flow diagram the modelsim program is simulated and the output is obtained. The project flow of the modelsim is important to beginner it should follow the same flow for any project which is using this software.

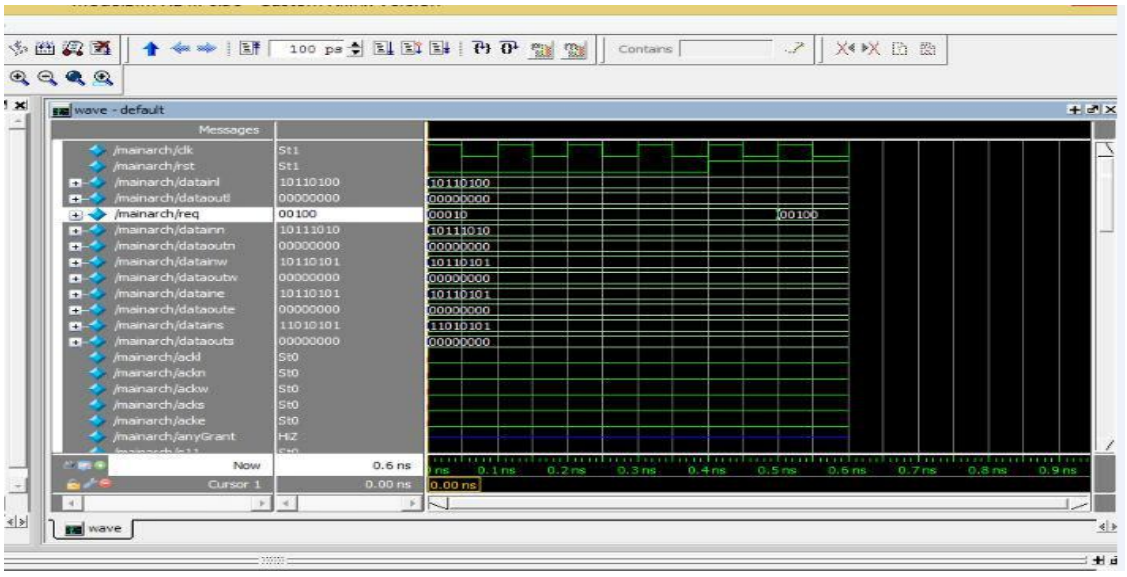


Figure 8 Simulation result of virtual channel (proposed)

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	12	28,800	5%
Number of 4 input LUTs	12	28,800	14%
Logic Distribution			
Number of occupied Slices	1,100	6,912	10%
Number of Slices containing only related Logic	1,050	1,150	90%
Number of Slices containing only unrelated Logic	0	1,054	2%
Total Number of 4 input LUTs	2,245	6,824	19%
Number used as logics	2,588		
Number unused flipflops	5	8	0%
Number of Bonded IOBs	15	220	8%
Fully used Flip Flops LUT pairs	8	0	93%
Number of unique control sets	1		
Number of slice register	3	28,800	2%
Total equivalent gate count for design	20,524		
Additional JTAG Gate count for IOBs	15,576		

Table 1 Device utilization summary of the existing model

VI. CONCLUSION

This project work presents a modelsim simulated result of virtual channel router architecture. The virtual channel allocations can provide performance improvement similar to wormhole router configuration for on chip network but much less area over headed. The performance of interconnection networks was improved by organizing the buffers associated with each network channel into virtual channels rather than a single FIFO queue. Associating several lanes with each physical channel decouples the allocation of physical channel to flits that leads to 8%lower power and 36%lesser area

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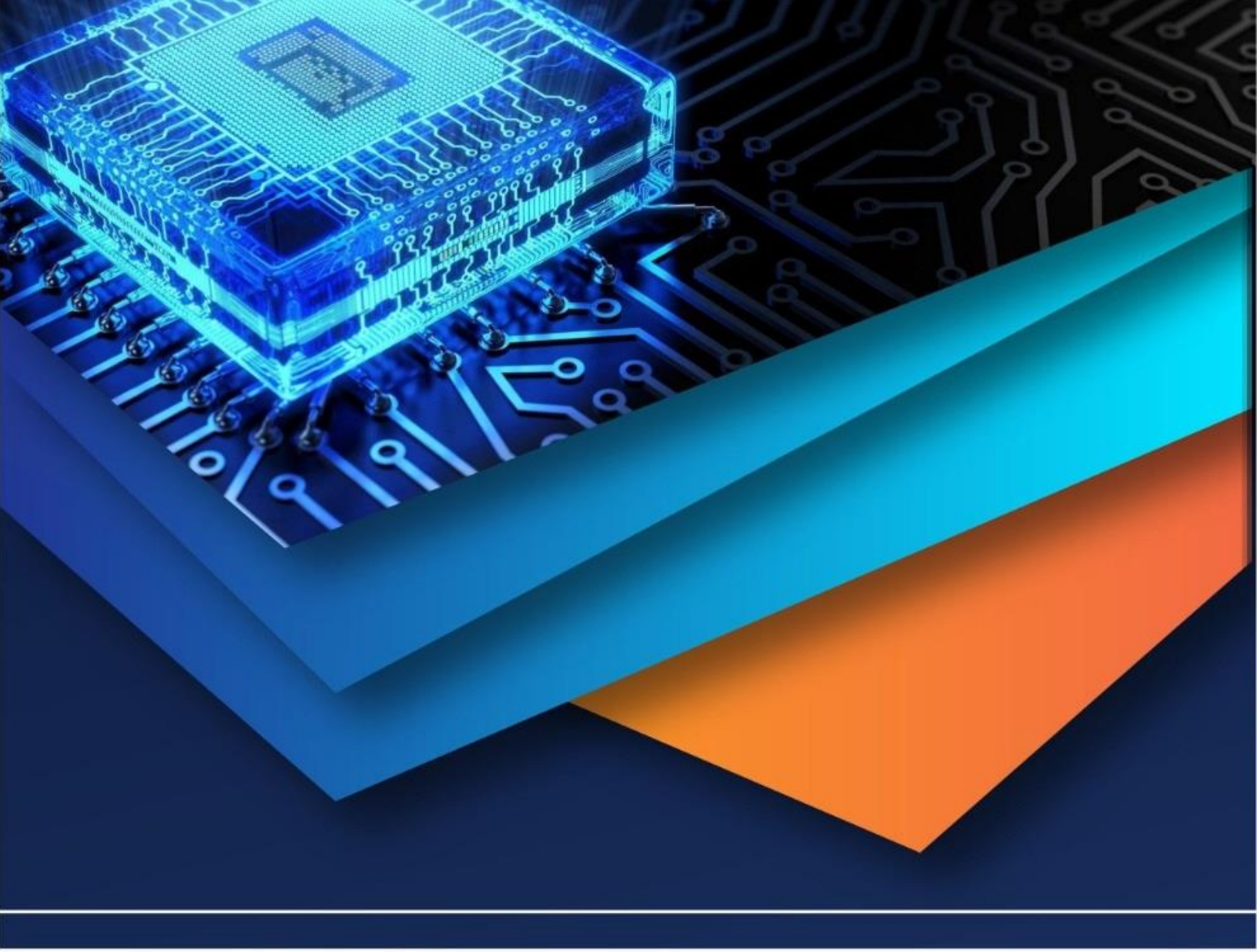

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