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A Comparative Performance Analysis of Various CMOS Design Techniques for XOR and XNOR Circuits

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Abstract*: *XOR and XNOR gates play an important role in digital systems. XOR & XNOR logic gates are basic building blocks of many arithmetic circuits. The XOR and XNOR circuit is implemented in pass transistor logic, static CMOS logic, transmission gate logic. The design of the XOR & XNOR circuits based on TSMC 32nm process models at the supply voltage 0.9V is simulated using HSPICE. Due to low power consumption and high speed these design circuits are suitable for arithmetic operations and VLSI applications. Hence comparison of delay & power is obtained in this paper for various design techniques of logic gates.

Keywords*: *HSPICE, Low power, pass transistor logic, transmission gate, Exclusive-OR, Exclusive-NOR

I. INTRODUCTION

To design integrated circuits with high operating frequency the major issues are power, delay and smaller silicon area with higher speed. The XOR and XNOR circuits influence the performance of the complex logic circuits. The key parameter for today's electronic industry is low power. In order to make a device more reliable and efficient, power consumption should be reduced. As the demand of portable consumer electronics increases, and the size of the chip decreases, challenges towards the power dissipated are induced [1-3].

In CMOS circuit, the power consumption for any given function must be reduced for two different reasons: the first reason is to reduce heat dissipation in order to allow a large density of functions to be incorporated on an IC chip. Any amount of power consumption is fruitful as long as it doesn't degrade overall circuit performance [4]. The second reason is to save energy in battery operated instruments. By choosing proper design style the power saving capability in circuits can increase at the design level. Without low-power design techniques such applications generally suffer from very short battery life, while packaging and cooling them would be very difficult. This is leading to an unavoidable increase in the cost of the product.

A. Static CMOS Logic

It is the most commonly used logic design technique. This circuit is made up of two networks namely pull up network (PUN) and pull down network (PDN). PUN and PDN comprises of PMOS transistors and NMOS transistors respectively. Input to these networks is dual of each other [5]. Output is based on the inputs applied to PUN and PDN making the output 1 or 0 respectively. This design technique is mostly used and produces results that are widely accepted but it requires more number of CMOS.

B. Pass Transistor Logic

The static Gate with low-impedance path exists. In this logic design, the reduction in output voltage swing is useful for power consumption as well as for slow switching. Less number of transistors are difficulty to design [7].

C. Transmission Gate Logic

Transmission gate CMOS (TG) uses complex logic functions by using complementary transistors. PMOS and NMOS are in parallel and are controlled by complementary signals. Both transistors are ON or OFF simultaneously [8].

The NMOS switch passes a good zero but a poor 1.

The PMOS switch passes a good one but a poor 0.

Combining them we get a good 0 and a good 1 passed in both directions.

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II. CIRCUIT DESIGN

A. Static CMOS XOR and XNOR Circuit

Complementary CMOS uses dual networks to implement a given function [9-11]. A first part consists solely of complementary pull-up (PMOS) network while a second part consists of pull-down (NMOS) networks. This technique is popular and produces results that are widely accepted but it requires more numbers of CMOS transistors. Static CMOS XOR and XNOR gate is shown in Fig.2.1(a) and Fig.2.1(b). The circuit operates with full output voltage swing.

$$Z = A \oplus B = (A + B).(A' + B')$$
$$Z' = (A \oplus B)' = \{(A + B).(A' + B')\}'$$
$$Z' = AB + A'B'$$
$$Z = (AB + A'B')' = A \oplus B$$

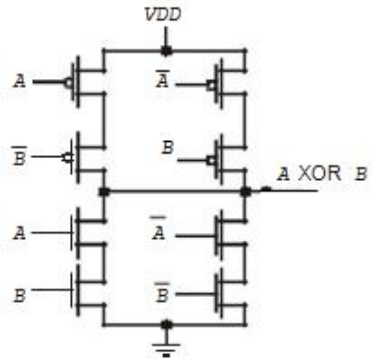

Fig.2.1 (a) Static CMOS XOR circuit.

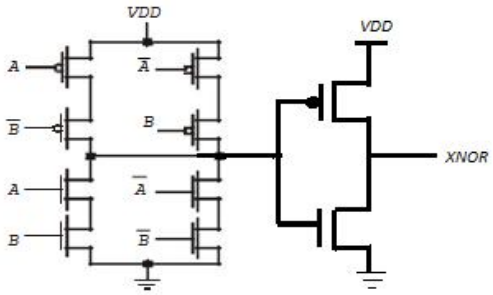

Fig.2.1 (b) Static CMOS XNOR Circuit

B. PTL based XOR and XNOR Circuits

When the input B is at logic 1, the PMOS pass transistor is OFF and NMOS pass transistor is ON. Therefore the XOR output of the circuit in Fig.2.2(a) is the complement of input A and XNOR output in Fig.2.2(b) gets the same logic value as input A. When the input B is at logic 0, the XNOR output of the circuit in Fig.2.2(b) is the complement of input A and XOR output in Fig.2.2(a) gets the same logic value as input A for the reason that PMOS pass transistor is ON and NMOS pass transistor is OFF.

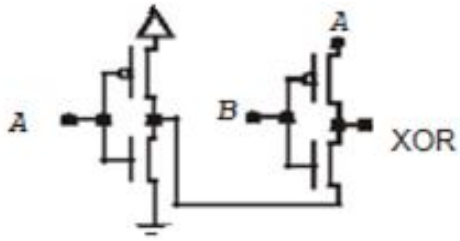

Fig.2.2 (a) Pass Transistor XOR Circuit

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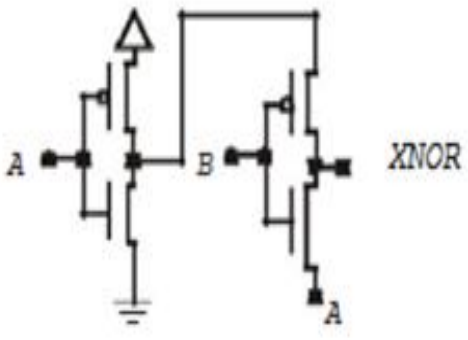

Fig.2.2 (b) Pass Transistor XNOR Circuit

C. Transmission Gate based XOR and XNOR Circuits

It solves the problem of low logic level swing by using PMOS as well as NMOS. The circuits for XOR-XNOR function is shown in Fig. 2.3(a) alleviate the problems of threshold voltage loss and non-zero standby power dissipation. By cascading a standard inverter after the XOR circuit, a high performance XNOR, as shown in Fig. 2.3(b) will have a restored output. The same property is present in the XOR structure. These circuits provide a full voltage swing (i.e., 0V for logic 0 and 1.8V for logic 1) [12-13].

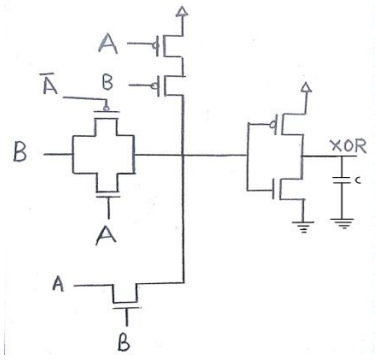

Fig.2.3 (a) Transmission Gate XOR Circuit

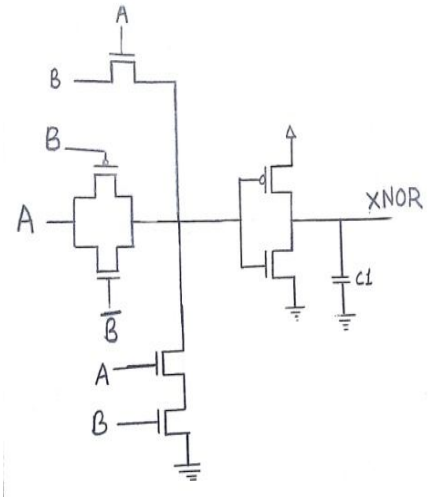

Fig.2.3 (b) Transmission Gate XNOR Circuit

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III. SIMULATION RESULTS

The transient and DC analysis of the circuits were performed on HSPICE at a supply voltage ranging 0.9V using TSMC 32nm CMOS process. The simulation results of various XOR and XNOR designs are shown in Fig.3.1-3.6.

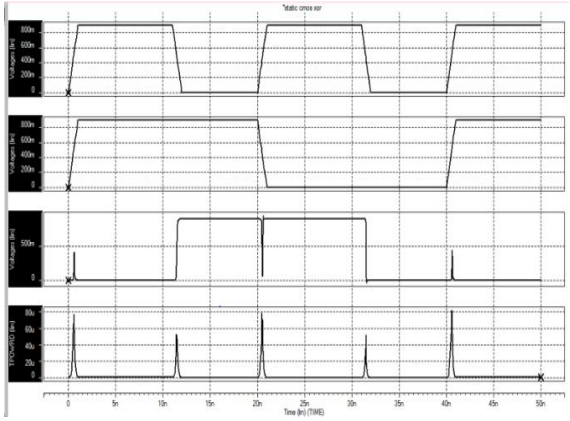

Fig.3.1 Static CMOS XOR Waveform

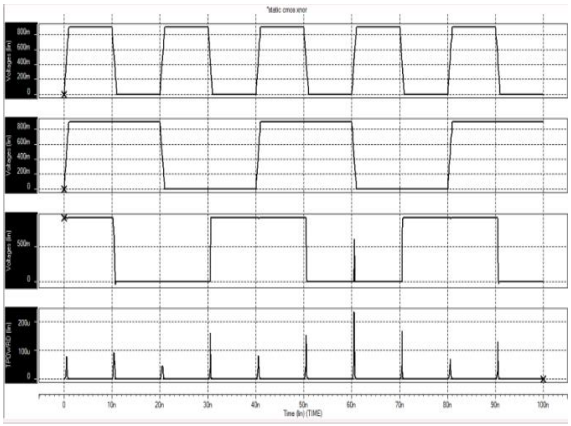

Fig.3.2 Static CMOS XNOR Waveform

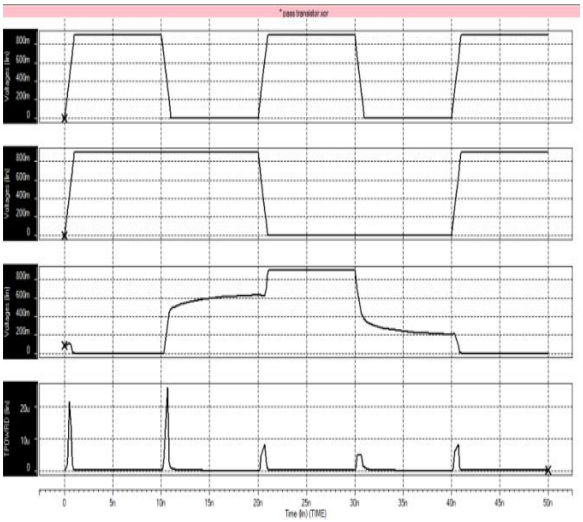

Fig.3.3 Pass Transistor XOR Waveform

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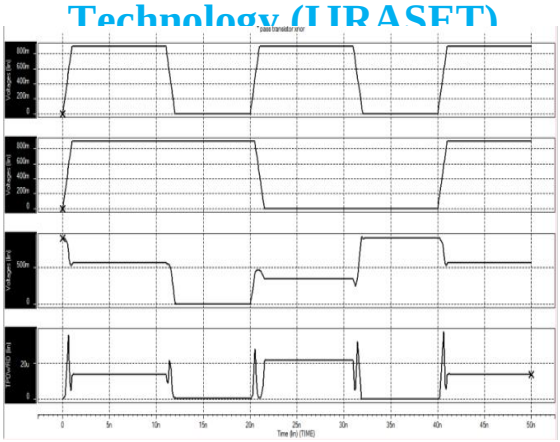

Fig.3.4 Pass Transistor XNOR Waveform

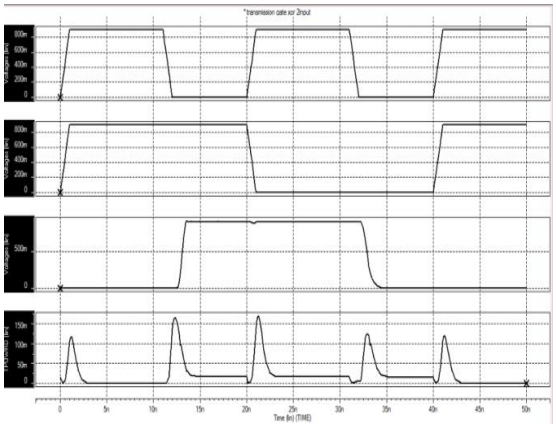

Fig.3.5 Transmission gate XOR Waveform

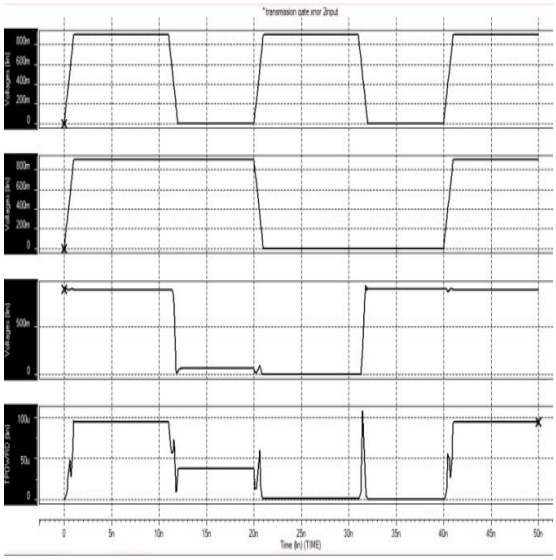

Fig.3.6 Transmission gate XNOR Waveform

IV. COMPARISON

The comparative performance for all design techniques described in this paper using XOR and XNOR circuit at VDD = 0.9V are respectively shown in Table 1 and Table 2.

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TABLE I
Comparative performance of transient analysis of XOR circuits with different design techniques at Vdd = 0.9V

Parameter XOR	Static CMOS Logic	Pass Transistor Logic	Transmission Gate Logic
Number of Transistor	12	4	2
tplh	9.0851E-09	3.0510E-10	5.2327E-11
tphl	1.3190E-11	1.6685E-10	2.0933E-11
Delay	4.5491E-09	2.3598E-10	3.6630E-11
Average Power	1.9658E-06	7.9505E-07	9.8448E-05
Maximum Power	7.8521E-05	2.6015E-05	1.6720E-04
PDP	8.9426E-15	1.8761E-16	1.3417E-15

TABLE II
Comparative performance of transient analysis of XNOR circuits with different design techniques at Vdd = 0.9V

Parameter XNOR	Static CMOS Logic	Pass Transistor Logic	Transmission Gate Logic
Number of Transistor	14	4	11
tplh	6.6263E-11	2.3065E-11	3.2094E-11
tphl	6.1547E-11	7.9278E-11	1.6440E-10
Delay	6.3905E-11	5.1171E-11	9.8248E-11
Average Power	2.6255E-06	9.8413E-06	3.4730E-05
Maximum Power	1.5933E-04	3.5464E-05	1.0833E-04
PDP	1.6778E-16	5.0358E-16	3.1421E-15

V. CONCLUSION

In this paper, we have studied various design techniques for XOR-XNOR circuits. The mentioned design techniques are compared based on area, delay, power consumption, and PDP. The performances of these techniques have been evaluated by HSPICE using a TSMC 32nm CMOS technology. These design techniques are suitable for arithmetic circuits and other VLSI applications with very low power consumption and a very high speed performance. Based on the simulation results, it has been culminated that in the PTL based XOR and XNOR design the output high (or low) voltage is deviated from the VDD (or ground) by a multiple of threshold voltage. The XOR-XNOR circuits using transmission gate improve the threshold voltage loss problem while XOR and XNOR circuits with feedback transistors have good output signal levels, consume less power and have high speed compared to the previous designs at low supply voltage.

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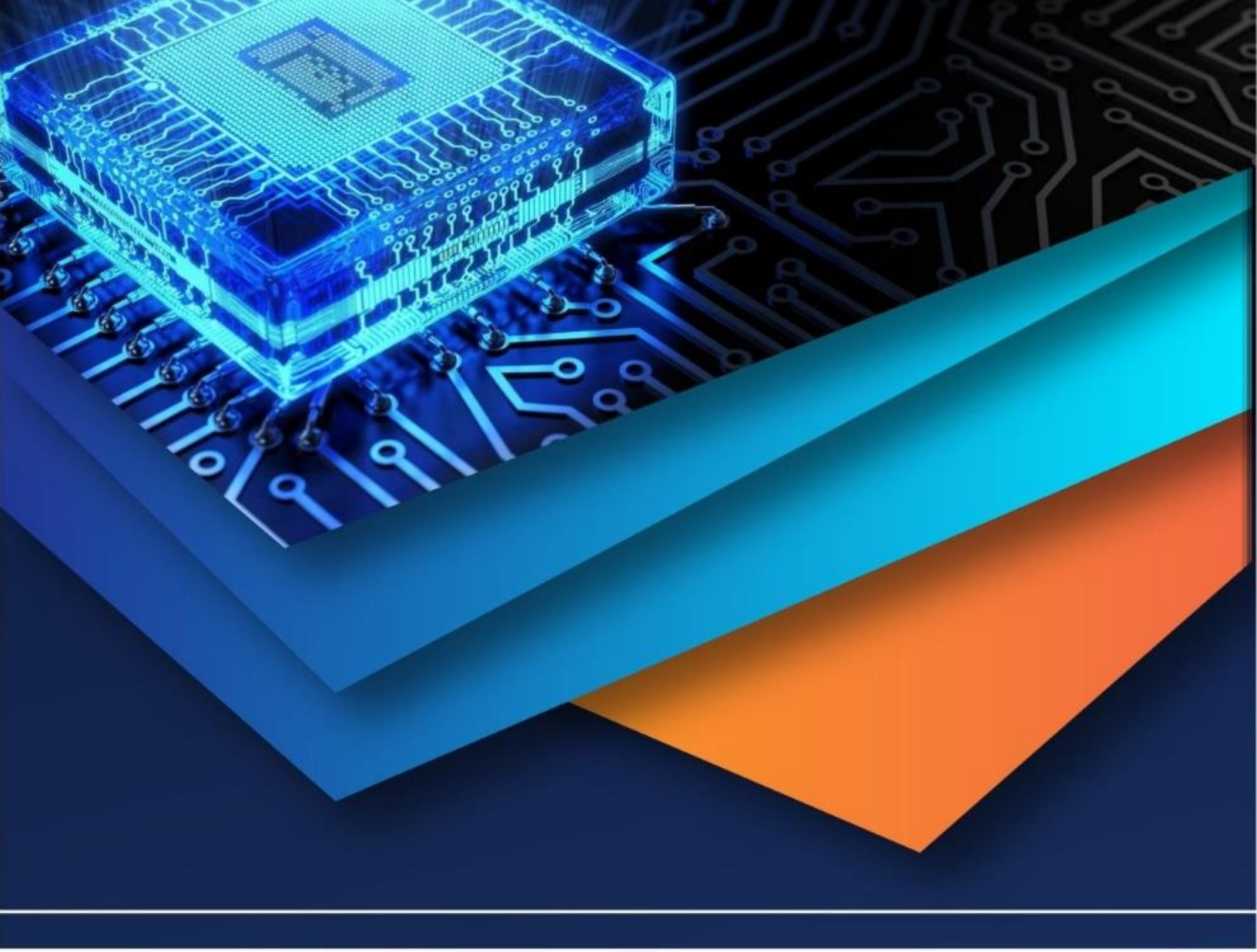

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