iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 5 **Issue:** VI **Month of publication:** June 2017

DOI:

www.ijraset.com

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Volume 5 Issue VI, June 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

Design of CMOS Frequency Multiplier in 180nm Technology

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Abstract: ***CMOS Frequency multipliers are key blocks in new developing applications at microwaves and mm-waves. Frequency multiplication is carried out in Radio Frequency or Microwave equipment to achieve high stability and low noise signals. Frequency multiplier circuits are utilized as a part of an extensive variety of applications in communication systems. In this paper, we have presented a method for designing a Digital Phase Locked Loop (DPLL) based Frequency Multiplier using Cadence Virtuoso 180nm CMOS Technology. The proposed circuit utilizes phase locked loop architecture to play out the frequency multiplication and is executed totally on-chip. Focal points of this topology incorporate excellent fundamental suppression, compact layout, and low power dissipation. The proposed design operates at the 3V power supply and provides less power dissipation of 1.46mW.***
Keywords— Op-amp, PLL, CMOS, PFD, VCO, LPF

I. INTRODUCTION

The frequency multiplier is an electronic circuit that produces an output signal whose frequency is an integral multiple (harmonic) of its input frequency. Frequency multipliers contain a nonlinear circuit that alters the input signal and produces harmonics of that signal. A band pass filter selects the desired fundamental frequency and removes the unwanted harmonics from the output. Frequency multipliers find a wide variety of applications in nonlinear optics to generate various harmonics of laser light, telecommunication circuits for instrument processing, frequency synthesizers and circuit analysis in analog processing. It can be more conservative to build up a lower frequency signal with lower control and after that utilization of the frequency multiplier to create an output signal having a frequency in millimeter or microwave range. Also, oscillators designed with the help of frequency multipliers have simplified design and improved phase noise.Power has turned out to be a standout amongst the most critical worries in plan merging for multi-gigahertz correspondence frameworks, for example, optical information joins, remote items, chip, and ASIC/SOC outlines. Power utilization has turned into a bottleneck in chip plan. With an end goal to decrease the power consumption of the circuit, the supply voltage can be diminished prompting lessening of dynamic and static power dissipation. Bringing down the supply voltage likewise lessens the execution of the circuit, which is usually unsatisfactory. Phase Lock Loop (PLL) is a closed-loop feedback system that is used to fix constant phase relationship between its reference clock phase and the phase of the output clock. PLL is an essential analog circuit having various communication applications such as clock generation, frequency synthesizer, clock recovery, radio, computer, etc. Phase Locked Loops are mainly utilized for clock synthesis, synchronization, skew and jitter reduction. PLLs are also used to produce all around coordinated on-chip checks in elite computerized frameworks. In order to reduce the overall power dissipation of the circuit, phase lock loop architecture is used for designing frequency multipliers [7].
Outline of this paper includes: Section 2 describes the design methodology opted for the frequency multiplier, Section 3 describes the simulation result and waveform of the design, section 4 includes the conclusion and performance parameters of the frequency multiplier, and finally section 5 includes the references.

II. DESIGN METHODOLOGY OF FREQUENCY MULTIPLIER

A. Schematic of Frequency Multiplier

A frequency multiplier is a gadget for duplicating by a whole number the input frequency of a signal. PLL can be modified so that it multiplies the input frequency by a constant factor i.e. it produces an output frequency having an integral multiple of the input frequency.

1) The basic architecture of PLL based frequency multiplier consists of three sections:

a) Phase Frequency Detector(PFD)

Volume 5 Issue VI, June 2017
ISSN: 2321-9653
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b) Low Pass Filter(LPF)

c) Voltage Controlled Oscillator(VCO)

The PFD is used to detect phase differences between the input signal and a feedback signal and then generates a corresponding error signal [1].” Up” or “down” error signals are produced by PFD by the phase difference between two signals and are fed to the LPF. If up error signal is generated by PFD then charging of LPF capacitance takes place otherwise it discharges the capacitance for corresponding down signal which in turn decreases control voltage. This control voltage is provided as input to VCO. LPF is used to store charge and prevents AC signals from reaching VCO i.e. passes only DC signals to VCO. The significance of VCO is that it either slow down or speed up the feedback signal by the error signal generated by PFD. VCO speeds up if “PFD produces up” signal, else it slows down if “PFD produces down” signal.

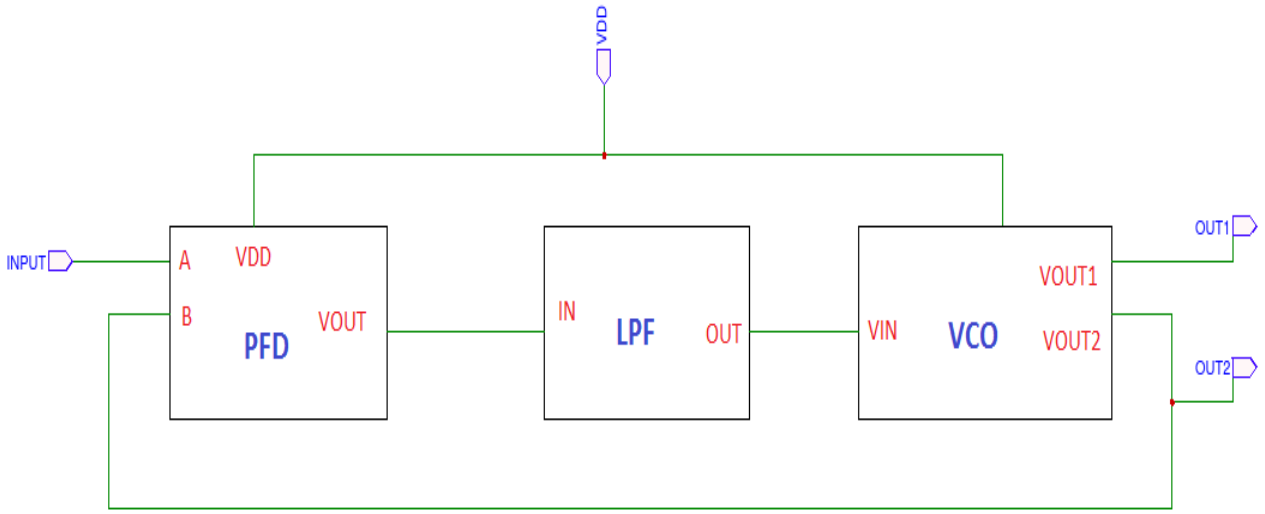

Fig. 1 Schematic of Frequency Multiplier Circuit

B. Schematic of Phase Frequency Detector

PLL is used to compare the phase of the output signal with the phase of the input signal. This comparison is made with the help of phase comparator or phase detector circuit. A Phase Frequency Detector (PFD) circuit produces an output having a linear relationship with the phase difference of the input signals. XOR gate is a basic example of phase detector circuit.

XOR gate circuit produces error pulses on both falling and rising edges of the signal. The width of output signal varies with the phase difference between the input signals. The differential amplifier and phase detector circuits are quite similar in operation as they both produce an output signal which is linearly proportional to the difference of input signals provided. Characteristics of PFD are Phase sensitivity, maximum operating frequency, and dead zone region.

The sensitivity of PFD describes the smallest phase difference; a PFD can detect and generate a corresponding correct output signal. This prompts a conclusion that higher is the sensitivity, the better will be PFDs performance [2].

The meaning of maximum operating frequency is characterized as one over the briefest period with right PFD yield signals when the sources of info have 90º phase difference and similar frequency. The maximum operating frequency and reset pulse width of PFD are inversely proportional to each other.

When the phase error lies within the dead zone, there is no change in the control voltage. If the input phase difference of PFD falls below a threshold value, the output voltage is no longer a linear function of the phase difference.

Also, if the phase difference is below a certain level, no current is injected by the charge pump. The dead zone is exceptionally undesirable since it permits the VCO to aggregate arbitrary phase error with respect to the input signal while getting no corrective feedback.

Volume 5 Issue VI, June 2017
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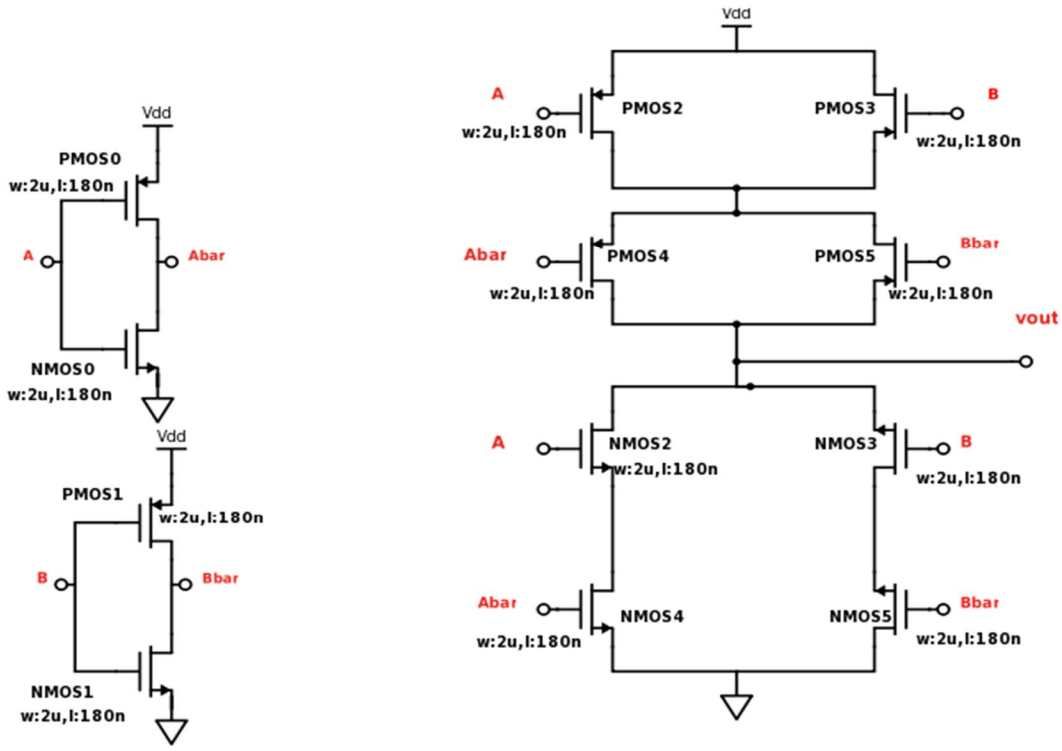

Fig. 2 Schematic of Phase Detector Circuit

C. Schematic of Low Pass Filter

Low pass filter is called as the brain of PLL. PLL loop filter (low pass filter) has two specific functions.

The essential function is to determine stability or loop dynamics. This is the means by which the loop reacts to unsettling influences, for example, changes in the reference frequency, changes of the input feedback divider, or at startup. Basic contemplations are the range over which the loop can accomplish lock (pull-in range, capture range or lock range), how quick the loop accomplishes (settling time) and damping behaviour.

The second regular thought is restricting the measure of reference frequency energy (ripple) showing up at the phase detector output that is then connected to the VCO control input. This frequency tweaks or modulates the VCO and produces FM sidebands ordinarily called "reference spurs."

The low pass normal for this square can be utilized to lessen this energy, yet now and again a band rejects "notch" may likewise be helpful.

The PLL filter is expected to evacuate any unwanted high-frequency components which may go out of the phase detector and show up on the VCO tune line. They would then show up on the yield of the VCO, as spurious signals [6].

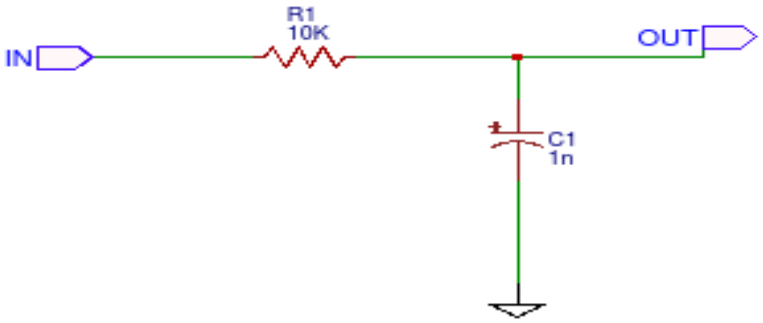

Fig. 3 Schematic of Low Pass Filter

Volume 5 Issue VI, June 2017
ISSN: 2321-9653
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D. Schematic of Voltage Controlled Oscilltor

A voltage-Controlled Oscillator or VCO is an electronic oscillator whose output oscillation frequency is a linear function the input voltage. The instantaneous oscillation frequency is determined using applied input voltage. Most ordinarily a voltage signal is utilized as a control input to change the output frequency. Voltage controlled oscillators have various applications in frequency (FM), pulse (PM) modulators and phase locked loops (PLL). VCO is also used as variable frequency signal generator. VCO gives a concurrent square wave and triangular wave outputs as a function of the input voltage. The frequency of oscillation is controlled by the resistor R and capacitor C alongside the voltage connected to the control terminal.

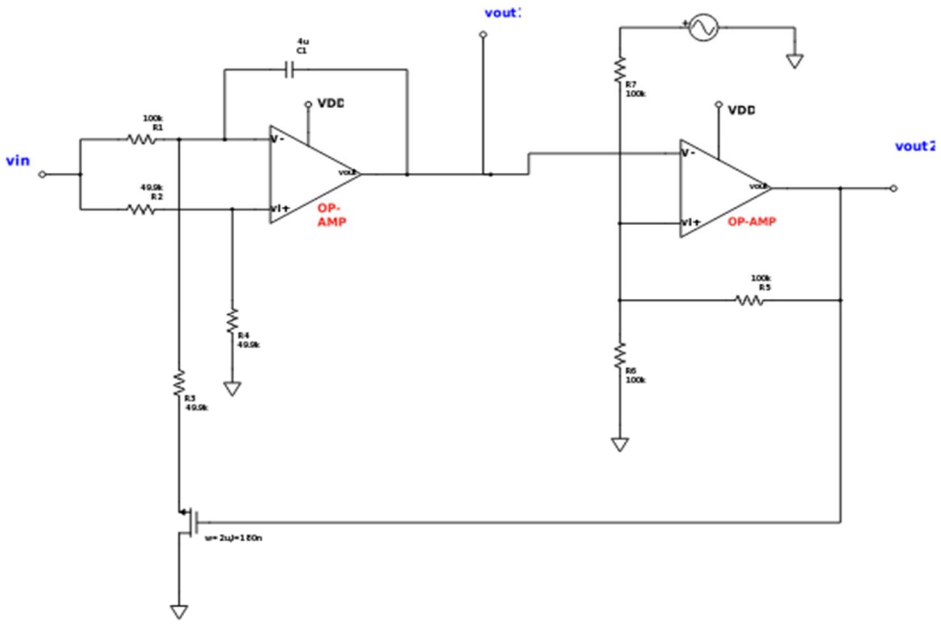

Fig. 4 Schematic of Voltage Controlled Oscillator

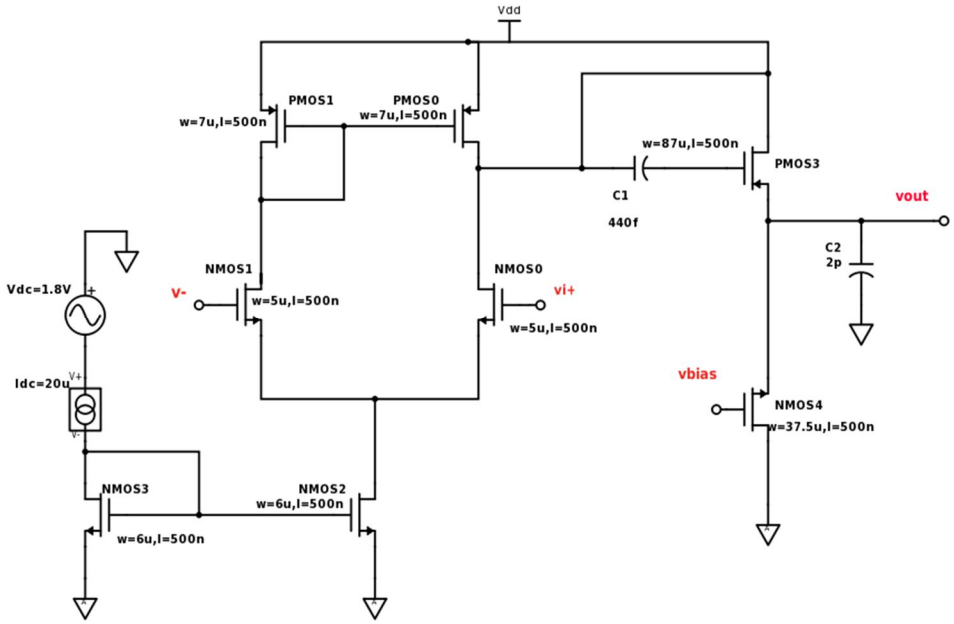

Fig. 5 Schematic of Two-Stage Operational Amplifier

Volume 5 Issue VI, June 2017
ISSN: 2321-9653
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Figure 5 shows the implementation of VCO with the help of two operational amplifiers. Square wave output is obtained whose frequency is determined by a control voltage. The first op-amp behaves as an integrator circuit. The control voltage is connected to the input terminal, and because of the voltage divider arrangement, half the control voltage is connected to the positive terminal of the first main op-amp. Likewise, at the negative terminal, the voltage is kept up at a similar level with a specific end goal to keep up the voltage drop across the R1 is half of the control voltage. At the point when the MOSFET is turned ON, the current from the resistor R1 moves through the MOSFET. The voltage which is presently changed over into current signal is used to charge the capacitor. Consequently, to source this current, the main op-amp must give a relentlessly rising output voltage [3].

At the point when the MOSFET is turned OFF, the current from the resistor R1 is used to discharge the capacitor. The main op-amp must provide a steadily falling output voltage. Along these lines, the output of the first operation amp is a triangular waveform. The second op-amp acts as Schmitt trigger, and it acknowledges the triangular wave as a contribution from the principal op-amp [4].

At the point when the info voltage is over the limit level, then it yields VDD, and if the information falls beneath the edge level, the yield winds up noticeably zero. Consequently, the square wave is created at the output.

III.SIMULATION RESULTS AND WAVEFORMS

A. Transient Analysis

The PLL-based Frequency Multiplier is fed with square wave pulse input having pulse width 5us, period 10us, and voltage1 as 0V and voltage2 as 2.5V. The output signal of a frequency higher than that of the input signal is produced having voltage1 as 3V and voltage2 as 0V. Power Dissipation, rise time, fall time, settling time and Delay have been evaluated from this output signal using calculator tool.

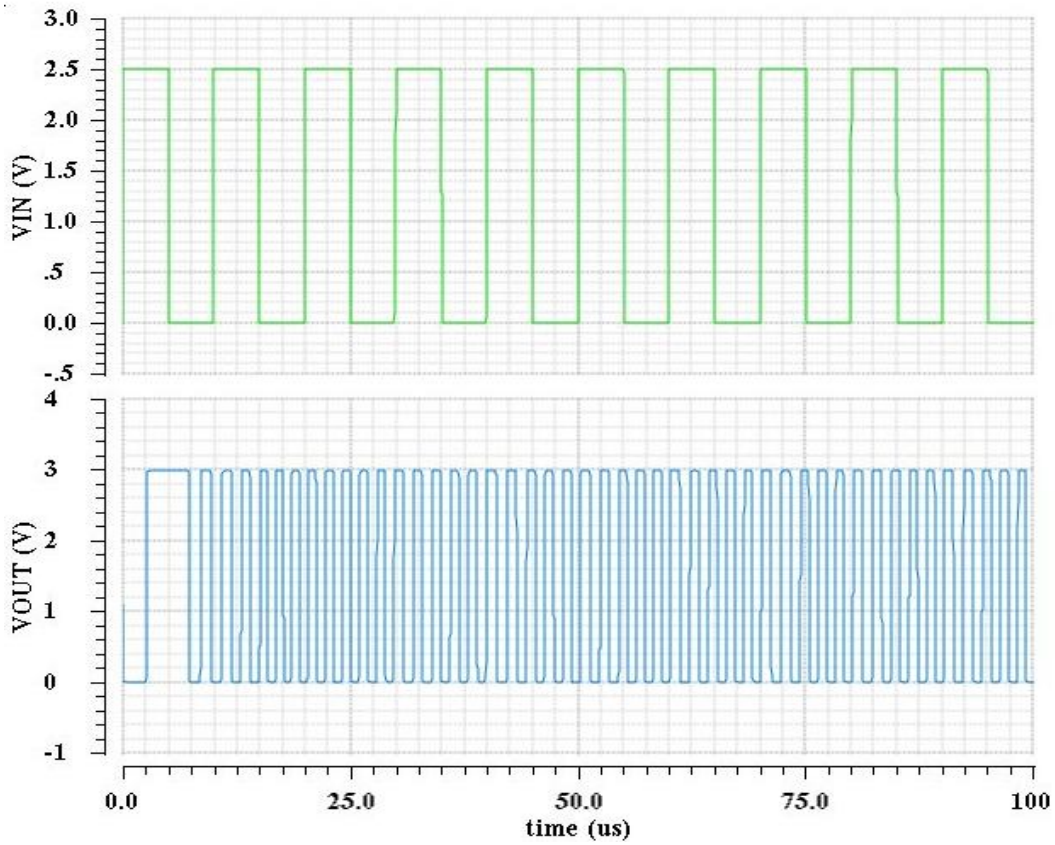

Fig. 6 Transient Analysis of Phase lock loop based Frequency Multiplier.

B. DC Analysis

At the input of PLL based Frequency Multiplier, a square wave pulse is provided having period 10us, pulse width 5us. DC analysis is carried out to calculate the power dissipation in the circuit for 0 to 2sec.

Volume 5 Issue VI, June 2017
ISSN: 2321-9653
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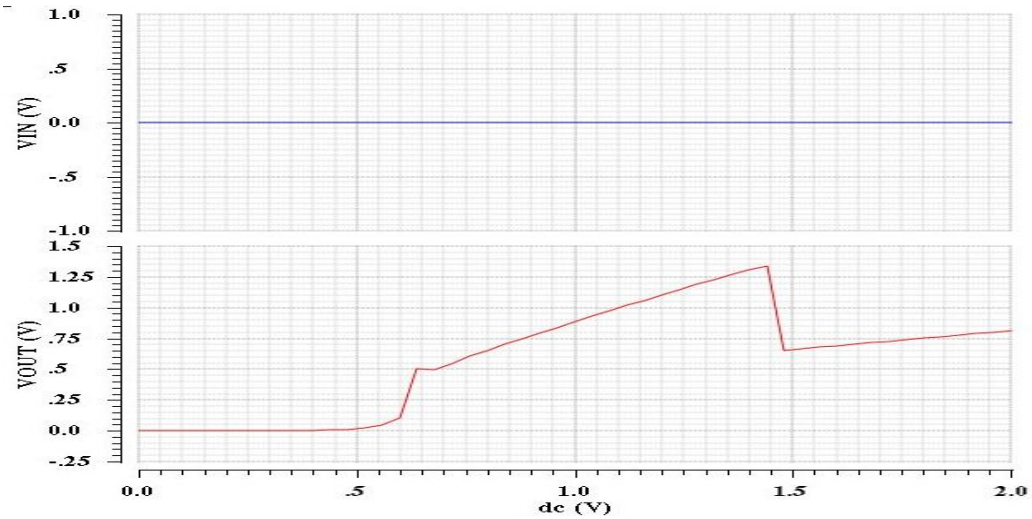

Fig. 7 DC Analysis of Phase lock loop based Frequency Multiplier.

C. AC Analysis

Sinusoidal wave input having magnitude 5m, frequency 100k, offset 0V, AC magnitude 2V is provided to the input of PLL based Frequency Multiplier. AC analysis is carried out for frequency range 1 to 100G. Bandwidth is calculated from the output signal using calculator tool.

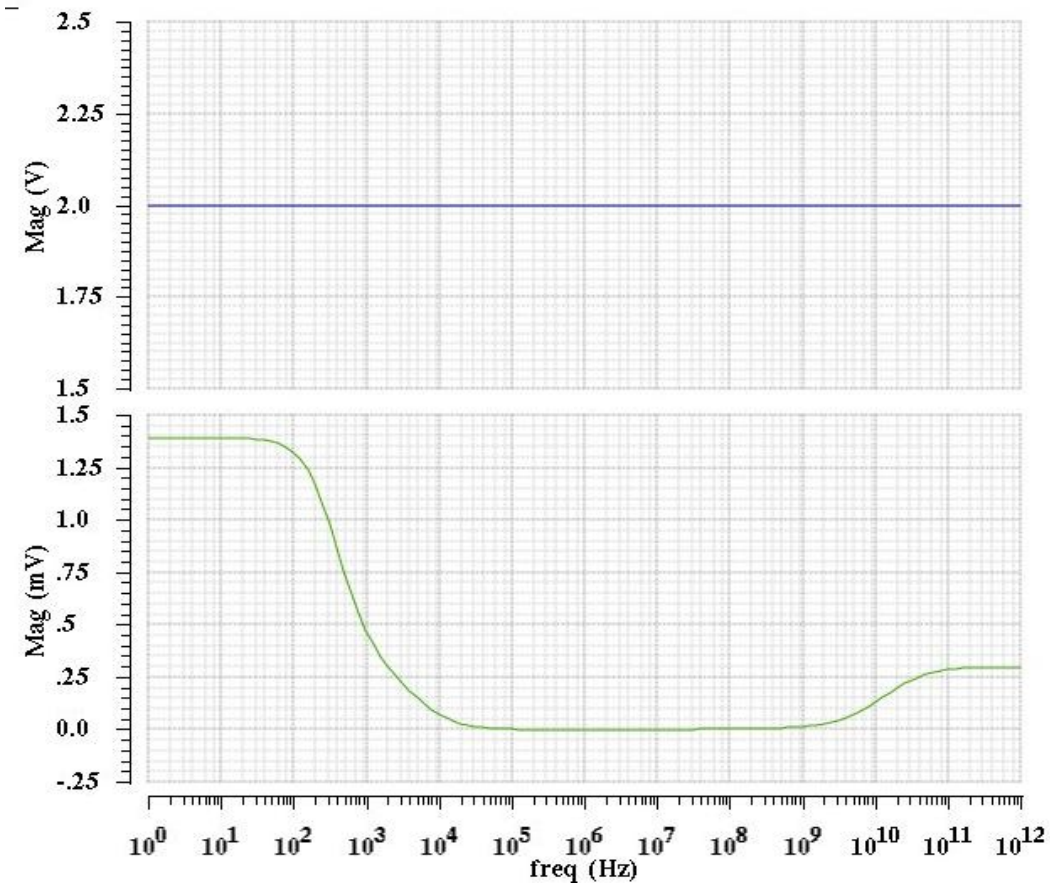

Fig. 8 AC Analysis of Phase lock loop based Frequency Multiplier.

Volume 5 Issue VI, June 2017
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E. Layout Design

The layout of DPLL based Frequency Multiplier is developed and verified for DRC and LVS checks.

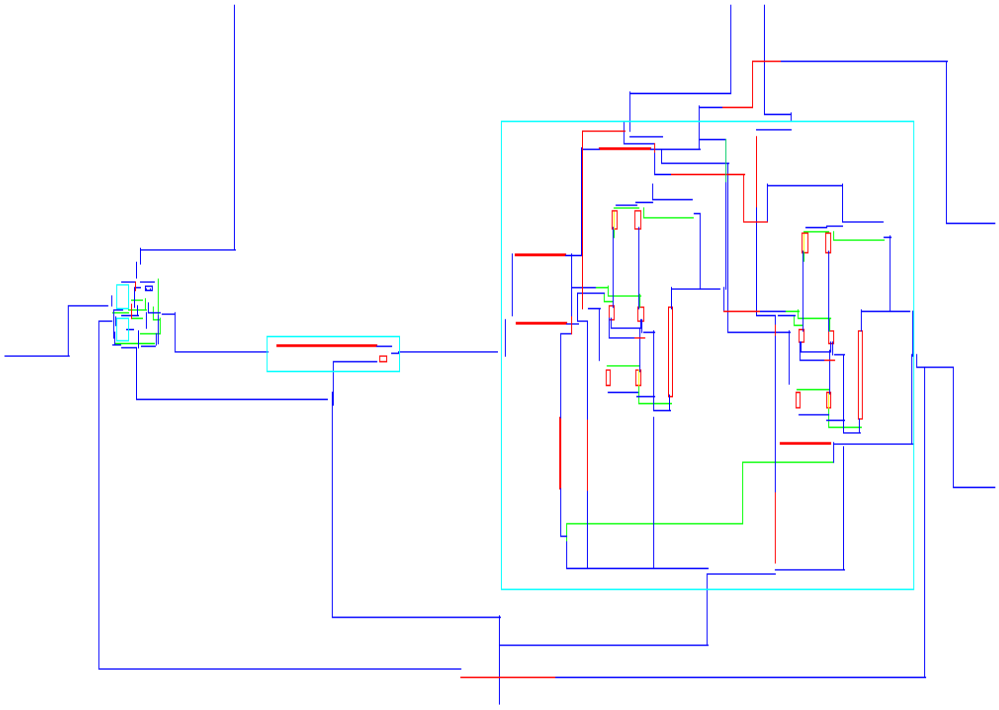

Fig. 9 Layout of Phase lock loop based Frequency Multiplier.

TABLE I
SIMULATION RESULTS OF FREQUENCY MULTIPLIER

PERFORMANCE PARAMETERS	VALUES
POWER SUPPLY	3V
INPUT FREQUENCY	100KHz
OUTPUT FREQUENCY	481.09KHz
BANDWIDTH	23.03GHz
POWER DISSIPATION	1.335mW
DELAY	122.52ns
RISE TIME OF OUTPUT	28.44ns
FALL TIME OF OUTPUT	20.66ns
SETTLING TIME OF OUTPUT	99.25us
AREA	600um*300um

Volume 5 Issue VI, June 2017
ISSN: 2321-9653
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TABLE2

COMPARISON AMONG PERFORMANCE PARAMETERS OF FREQUENCY MULTIPLIER

PARAMETERS	THIS WORK	[9]	[8]	[12]
TECHNOLOGY	180nm	180nm	180nm	180nm
POWER SUPPLY	3V	3.3V	-	1.8V
POWER DISSIPATION	1.33mW	-	26.9mW	25.85mW
AREA	600um*300um	-	-	290mm*160mm

IV. CONCLUSIONS

A high-speed DPLL-based Frequency Multiplier has been designed using 180nm CMOS process, utilizing a 3V power supply. It operates in the frequency range of 100 KHz - 2.7 MHz This circuit design is consuming less power i.e. having low power dissipation nearly 1.46mW. This circuit provides fewer harmonics and less noise for the output signal. A variable frequency multiplier has been designed using phase lock loop architecture to obtain low noise, high-frequency signals from a small frequency signal. The delay produced by the output signal w.r.t input signal is 122.5ns i.e., slight. Also, it is a compact design i.e. consuming less area.

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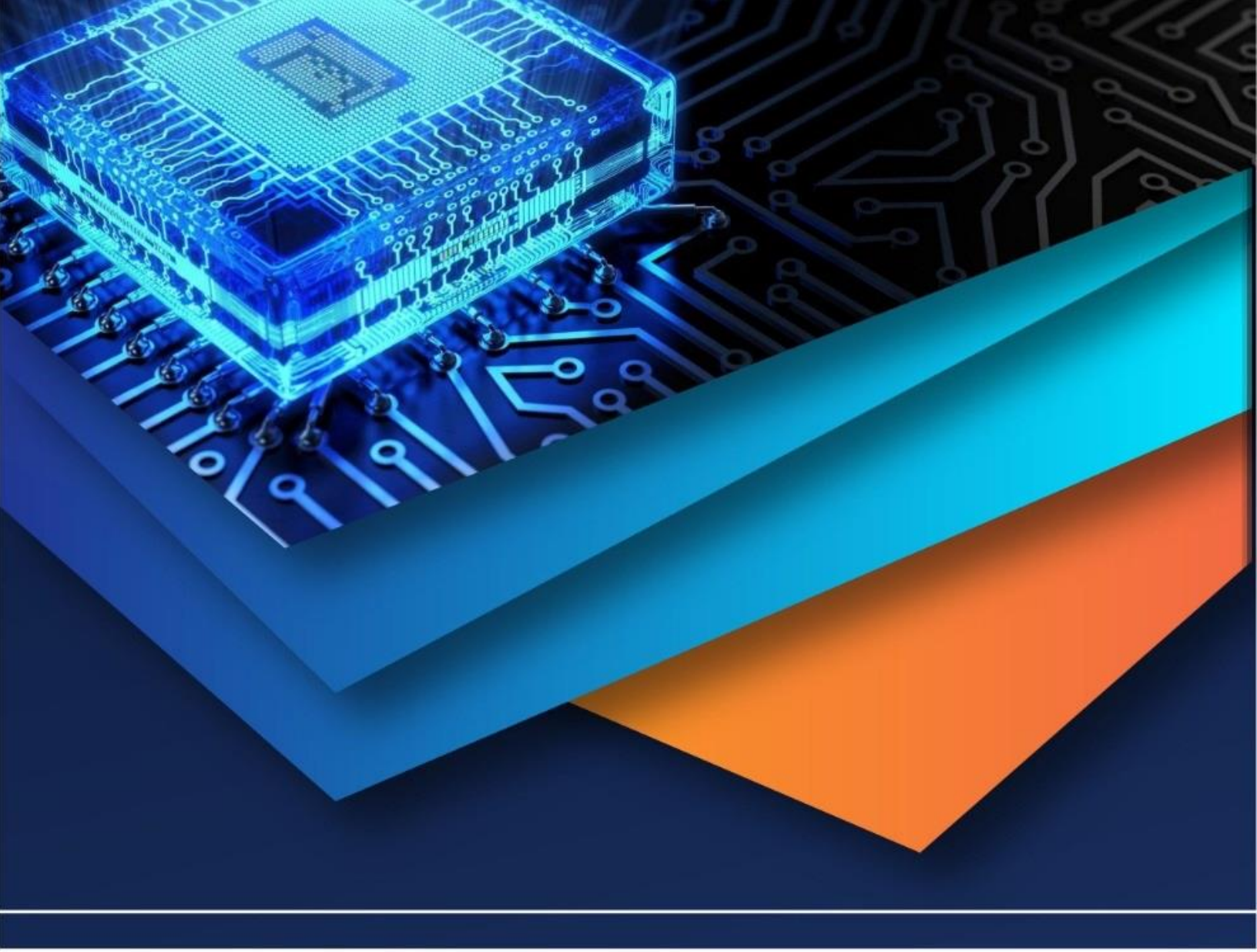

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