iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 5 **Issue:** VI **Month of publication:** June 2017

DOI:

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Volume 5 Issue VI, June 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

Differentiate Different Methodology for Design of Vedic Multiplier

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Abstract: ***Multiplier is one of the most important part in any processor speed which improves the speed of the operation for example in special application processors like Digital Signal Processor (DSPs). Basically, the operational speed of any digital signal processor is strictly dependent upon the speed of the multipliers used. This paper presents the comparative study of design methodology of Urdhva Tiryakbhyam multiplier on various performance factors like power, delay, space, speed. This paper gives information of "Urdhva Tiryakbhyam" algorithm of Vedic Mathematics which is utilized for multiplication to improve the speed, power and area of multipliers. Proposed design is simulated using ISim and synthesized using Xilinx ISE 14.5. When compared with Mux based Vedic multipliers, proposed design shows a significant improvement in speed.***
Keywords: Vedic Multiplier, Delay, speed, Mux based adder, Brent Kung adder, Urdhva Tiryagbhyam Sutra, Verilog HDL

I. INTRODUCTION

Multipliers are frequently used in DSP, image processing architectures and microprocessors. It plays an important fundamental function in arithmetic operations. A high speed processor performance greatly depends on the multiplier, in most digital signal processing systems as well as in all-purpose processors which is one of the essential hardware components also it's consumed area is more. Vedic multiplier gives the fast speed of operations than the conventional multiplier and requires less system memory. As compared to other multiplier design this multiplier requires very small area. Here in this work we use different methodology for designing Vedic multiplier, such as full adder, MUX based adder, and Brent Kung adder. Brent Kung adder is the parallel prefix form of carry look ahead adder. The design result of the multiplier shows that the 16- bit Vedic multiplier is faster other than two design methodology and16- bit Vedic multiplier with MUX based adder gives medium response that is faster than full adder methodology but slower than Brent Kung adder methodology. Hence full adder gives poor performance as compared to other. The main purpose of this work is to design compared the performance of 16 X 16 bit Vedic multiplier by combining the best technique.

II. VEDIC MATHEMATICS

The ancient Indian Vedic mathematics is now currently used in our global silicon chip technology for easier and faster calculations. The proposed Vedic multiplier is based on the Vedic multiplication formulae (Sutras). By using three sutras of Vedic mathematics the complex number multiplication can be done, which are Urdhva Tiryakbhyam sutra, Ekadhikena Purvena, and Nikhilam Navatascaraman Dasatah or simply Nikhilam. The Nikhilam sutra of Vedic mathematics can only be applied to large number multiplication. While the Urdhva Tiryakbhyam method of Vedic mathematics can be efficiently applied to all cases of multiplication. This is a universal method for obtaining fast multiplication which can be applied everywhere. It is very simple and easy to implement. For the multiplication of two numbers in the decimal number system these Sutras have been traditionally used. In this present work, we apply the same ideas to the binary number system for making the proposed algorithm compatible with the digital hardware.

A. Vedic multiplier using, Urdhva Triyagbhyam" Sutra

Urdhva Tiryakbhyam Sutra is a general multiplication formula which is applicable to all cases of multiplication. It literally means "Vertically and crosswise". This Sutra has been conventionally used for multiplication of two numbers in the decimal number system. The same idea has been applied for binary multiplication in this work. By breaking into smaller sizes, this can solve the multiplication of larger number (N X N bits). The 2 x 2 Vedic multiplier are basic building module through which higher multiplier are designed by splitting into smaller sizes.
This algorithm can be implemented into three steps which are as follows:

Volume 5 Issue VI, June 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

1) *Step-1:* The first step is vertical multiplication of LSB of both multiplicands.
2) *Step-2:* Second step is crosswise multiplication and additions of the partial products.
3) *Step-3:* Third step is vertical multiplication of MSB of the multiplicand and addition with the carry propagated from step 2. For better understanding consider 2-bit two binary number are a1a0 and b1b0. The below figure 1 shows the 2 bit multiplier.

The expression of two bit Vedic multiplier is:

s0 = a0 and b0
s1 = (a1 and b0) XOR (a0 and b1)
c1 = (a1 and b0) and (a0 and b1)
s2 = c1 XOR (a1 and b1)
c2 = c1 and (a1 and b1)
sum = {c2,s2,s1,s0}

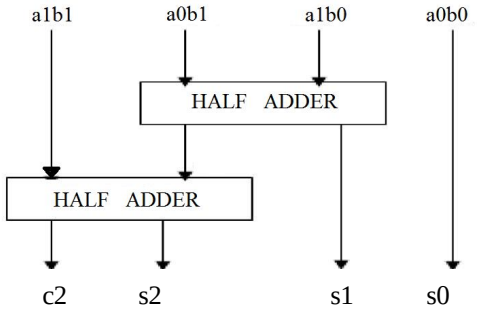

Figure 1: Line Diagram for 2 X 2 Bit binary multiplication using Urdhva Tiryagbhyam Sutra

B. Algorithm for 4 x 4 bit Vedic multiplier Using Urdhva Tiryakbhyam (Vertically and crosswise) for two Binary number –

Let us consider 'X3X2X1X0' (Multiplicand) and 'Y3Y2Y1Y0' (Multiplier) are two 4 bit binary number which are multiply by Urdhva Tiryakbhyam methods. The algorithm for 4 x 4 bit Vedic multiplier using dhva Tiryakbhyam are described below. Now consider H, G, F, E, D, C, B, A are the propagated carry through 4 x 4 bit multiplication and consider the product P7P6P5P4P3P2P1P0 are the obtained product during the multiplication process.

CP = Cross Product (Vertically and Crosswise)

X3 X2 X1 X0 Multiplicand
Y3 Y2 Y1 Y0 Multiplier
H G F E D C B A

P7 P6 P5 P4 P3 P2 P1 P0 Product

PARALLEL COMPUTATION METHODOLOGY

1. CP X0 = X0 * Y0 = A
   Y0
2. CP X1 X0 = X1 * Y0+X0 * Y1 = B
   Y1 Y0
3. CP X2 X1 X0 = X2 * Y0 +X0 * Y2 +X1 * Y1 = C
   Y2 Y1 Y0
4. CP X3 X2 X1 X0 = X3 * Y0 +X0 * Y3+X2 * Y1 +X1 * Y2 = D
   Y3 Y2 Y1 Y0
5. CP X3 X2 X1 = X3 * Y1+X1 * Y3+X2 * Y2 = E
   Y3 Y2 Y1

Volume 5 Issue VI, June 2017
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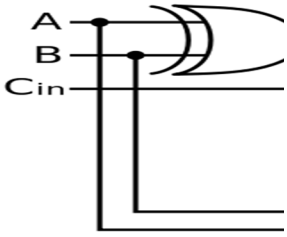
6. CP X3 X2 = X3 * Y2+X2 * Y3 = F
   Y3 Y2
7 CP X3 = X3 * Y3 = G
   Y3

III. DIFFERENT ADDER DESIGN USED TO DESIGN MULTIPLIER

There are several adder that used for deign multiplier. Some of them are as follows

A. *Full adder*

Full adder is used to add three one bit binary number. It takes three one bits as an input (two inputs and one previous carry) and generate two bit output (one for sum and one for carry). For increasing the number of bit cascading of the full adder take place. It consist of as given in figure 2.



$$S = \bar{A}\bar{B}C_{IN} + \bar{A}B\bar{C}_{IN} + A\bar{B}\bar{C}_{IN} + ABC_{IN}$$

Factoring out $\bar{A}$ and A:

$$S = \bar{A}(\bar{B}C_{IN} + B\bar{C}_{IN}) + A(\overline{B\bar{C}_{IN}} + BC_{IN})$$

which is

$$S = \bar{A}(B \oplus C_{IN}) + A(\overline{B \oplus C_{IN}})$$

Figure 2: Architecture of full adder

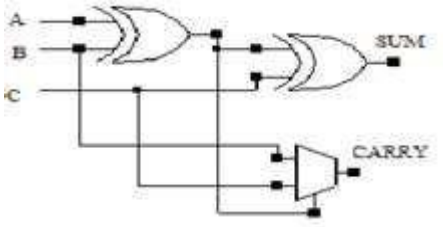
B. *MUX based adder*

For efficient implementation adders become a critical hardware unit of multiplier. The speed of multiplier ultimately increased when the delay of the adder is reduced. In terms of delay and power dissipation, it is observed that full adder with multiplexer and XOR gate gives best performance, especially. It consists of two XOR gates and one 2xl MUX as shown in Fig. 3.

By using logical effort method we can calculate delay mathematically instead of using simulation tools. It gives a simple method to select best logical topology. Let us assumed ‘d’ is the delay for a single stage network in term of is logical effort ‘g’, electrical effort ‘h’ and parasitic delay ‘p’, than the delay can be calculated by the equation (1) as given below

$$d = g*h+p; \quad (1)$$

where 'g 'represents logic gate's ability to produce output current (Compared to inverter, how much worse it is in producing output current), 'h' gives ratio of output capacitance to input capacitance and p gives delay of gate due to internal capacitance.



Sum	$S = A \oplus B \oplus C;$
Carry	$C_{out} = \overline{(A \oplus B)}.B + (A \oplus B).C$

Volume 5 Issue VI, June 2017
ISSN: 2321-9653
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Figure 3: Architecture of MUX based adder

C. Brent Kung adder

Brent Kung adder is the type of parallel prefix adder. Parallel prefix adder are high performance carry tree adder in which pre-computing of propagation and generation signal take place. Due to the complexity (log2n) delay through the carry path, the parallel-prefix tree adders are more favorable in terms of speed as compared to other adders. It consumed less area and has maximum depth. The number of cell of Brent Kung adder can be calculated by (2n-1) –log2n and the delay of the structure is (2log2 n-2). The three steps are generally used for design a Brent Kung adder:

1) *Step-1:* It involves the creation of generate and propagate signals for the input operand bits.
2) *Step-2:* This involves the generation of carry signals.
3) *Step-3*: In this step the sum bits of the adder following stages of the operand bits and the preceding stage carry bit using a XOR gate

Step-1: Pre-processing Stage
Pi=Ai XOR Bi
Gi=Ai .Bi
Step-2: Carry generation Stage
If nodes are connected than
CPi = CPi.CPj
CGi= CGi+CGj.CPi
Otherwise
CPi =Pi and CGi = Gi (Here j node is connected to i node)
Step-3: Post-processing Stage
Si = Pi XOR CGi -1

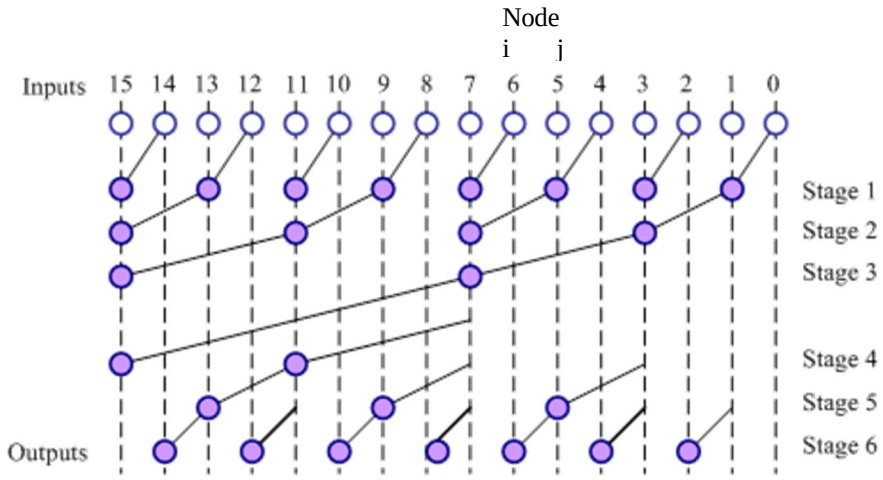

Figure 4 Schematic of 16 bit Brent Kung adder

IV. DESIGN OF 16 X 16 VEDIC MULTIPLIER USING FULL ADDER

The 2 x 2-bit Vedic multiplier is the basic building section for the system. Two Half adders are required in designing 2 x2 Vedic Multiplier, figure 5 shows the RTL view of 16x16 bits Vedic multiplier using full adder.

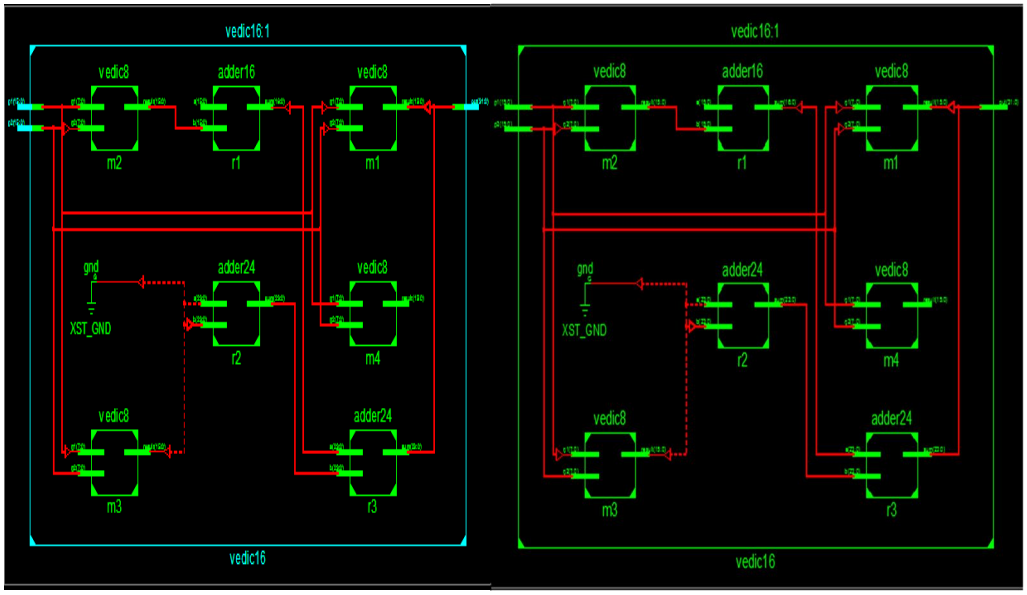

Figure 5: RTL view of 16x16 Figure 6 RTL view of 16x16 bit Vedic Multiplier using

Volume 5 Issue VI, June 2017
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Vedic multiplier using full adder mux based adder

V. DESIGN OF 16 X 16 VEDIC MULTIPLIER USING MUX BASED ADDER

Figure 6 gives the RTL view of 16x16 bits Vedic multiplier. The 4 x 4-bit multiplier is designed by using four 2 x 2-bit Vedic multiplier . The 8 x 8 bit Vedic multiplier is designed by using four 4 x 4 bit Vedic multiplier building blocks. The approach applied for designing a 16 x 16-bit Vedic multiplier by using four 8 x 8 bit multiplier blocks and two 24-bit and one 16-bit MUX based adder blocks

VI. DESIGN OF 16 X 16 VEDIC MULTIPLIER USING BRENT KUNG ADDER

The approach applied for designing a 16 x 16-bit Vedic multiplier by using four 8 x 8 bit multiplier blocks and three 16-bit Brent Kung adders, RTL view are shows in figure 7.

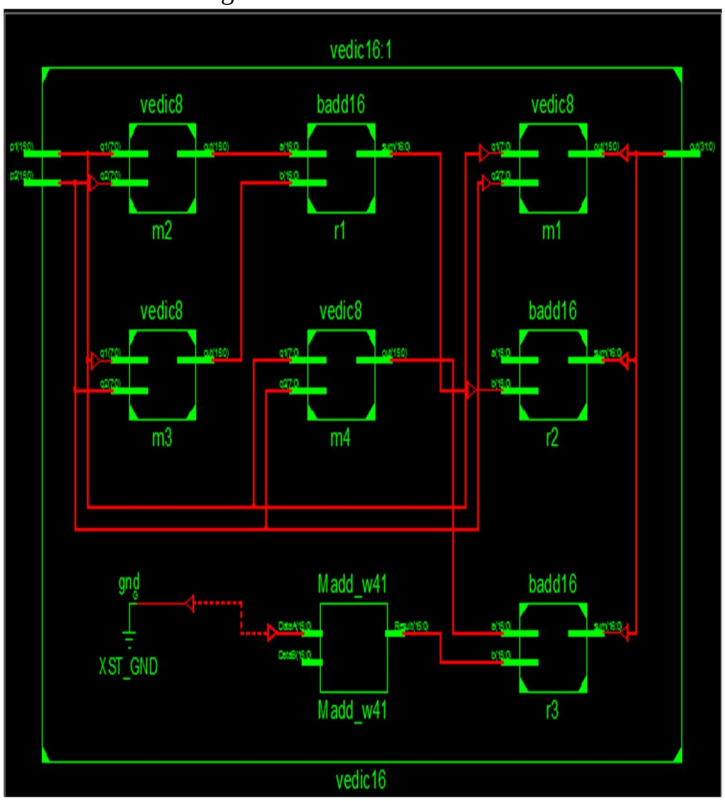

Figure 7 RTL view of 16x16 bit Vedic Multiplier using Brent Kung adder

VII. RESULT

A. *Simulation*

The functionality of Vedic multiplier is verified and confirms the operation of the design from the simulated waveforms. The combinational delay is reduced drastically with a little bit of trade off in terms of area. ISim simulator is used for simulation purpose. Figure 8, 9 & 10 shows the Simulation result for 16 bit Vedic multiplier in which 'P1' and 'P2'are same set of inputs and 'out' is their product and table 1 gives the delay and number of slice LUTs comparison between these two design architecture.

B. *Simulation of 16 X 16 bit Vedic Multiplier with three methodology*

The Simulation Result of 16X 16 bit Vedic Multiplier using full adder are shown in figure 8, 16X 16 bit Vedic Multiplier using Brent Kung adder are shown in figure 9 and Simulation result for 16 X 16-bit Vedic multiplier using Brent kung is shown in figure 10 in which P1= 1111000000000000 and P2= 1000111111111111 is taken and result out =10000111000000000000000000000000 is obtained. Figure 8 gives the delay compression between two Vedic multiplier architecture designs.

Volume 5 Issue VI, June 2017
ISSN: 2321-9653
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Figure 8: Simulation Result of 16X 16 bit , Multiplier using full adder

Figure 9: Simulation Result of 16X 16 bit Vedic multiplier using MUX based adder

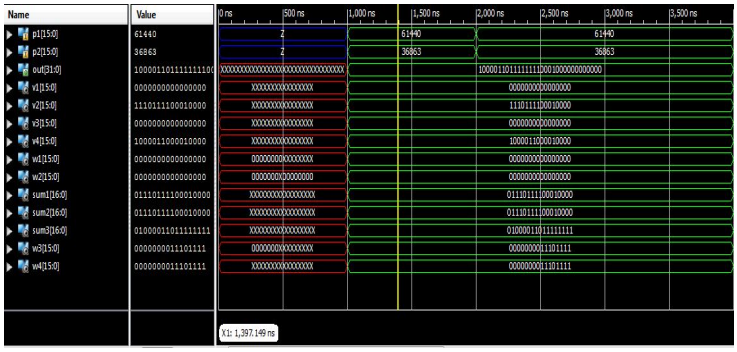

Figure 10: Simulation Result of 16X 16 bit Vedic Multiplier using Brent Kung adder

Table 1:

Ty	No. of Bits	No.of bonded IOs	Delay (ns)	Level of logic	Number of Slice LUTs
Vedic multiplier using Brent Kung adder	16	64	12.818	22	568
Vedic multiplier using MUX based adder	16	64	16.142	23	513
Vedic multiplier using full adder	16	64	20.347	23	623

VIII. CONCLUSION AND FUTURE WORK

This paper work presents a high performance design for multiplication by combining the feature of Vedic mathematics and different adders. When we compared our design methodologies ‘’Vedic multiplier using full adder, Vedic multipliers using Mux based adder and Vedic multiplier using Brent Kung adder’, the design with Brent Kung adder gives much less delay i.e. high performance . The design with full adder gives large delay as compare to other two design. So MUX based adder design little improvement in performance from full adder design. The multiplier architecture using Brent Kung adder and its fast performance makes this particularly attractive for VLSI implementations. For future work, its performance within MAC unit and ALU can be tested and compared with designs. This 16 bit Multiplier can be further extended to 32 bit or 64 bit multiplier.

IX. ACKNOWLEDGMENT

I would like to dedicate this paper to my husband Mr. Abhimanyu Tyagi.

To Mr. Suyash Tyagi thank you for your assistance and advice, my in laws Mrs. Chitralekha Tyagi and Mr. Anuj Kumar Tyagi. And my Parents Mrs. Pavitra Tyagi & Mr. Yograj Tyagi, I would have never done this without you.

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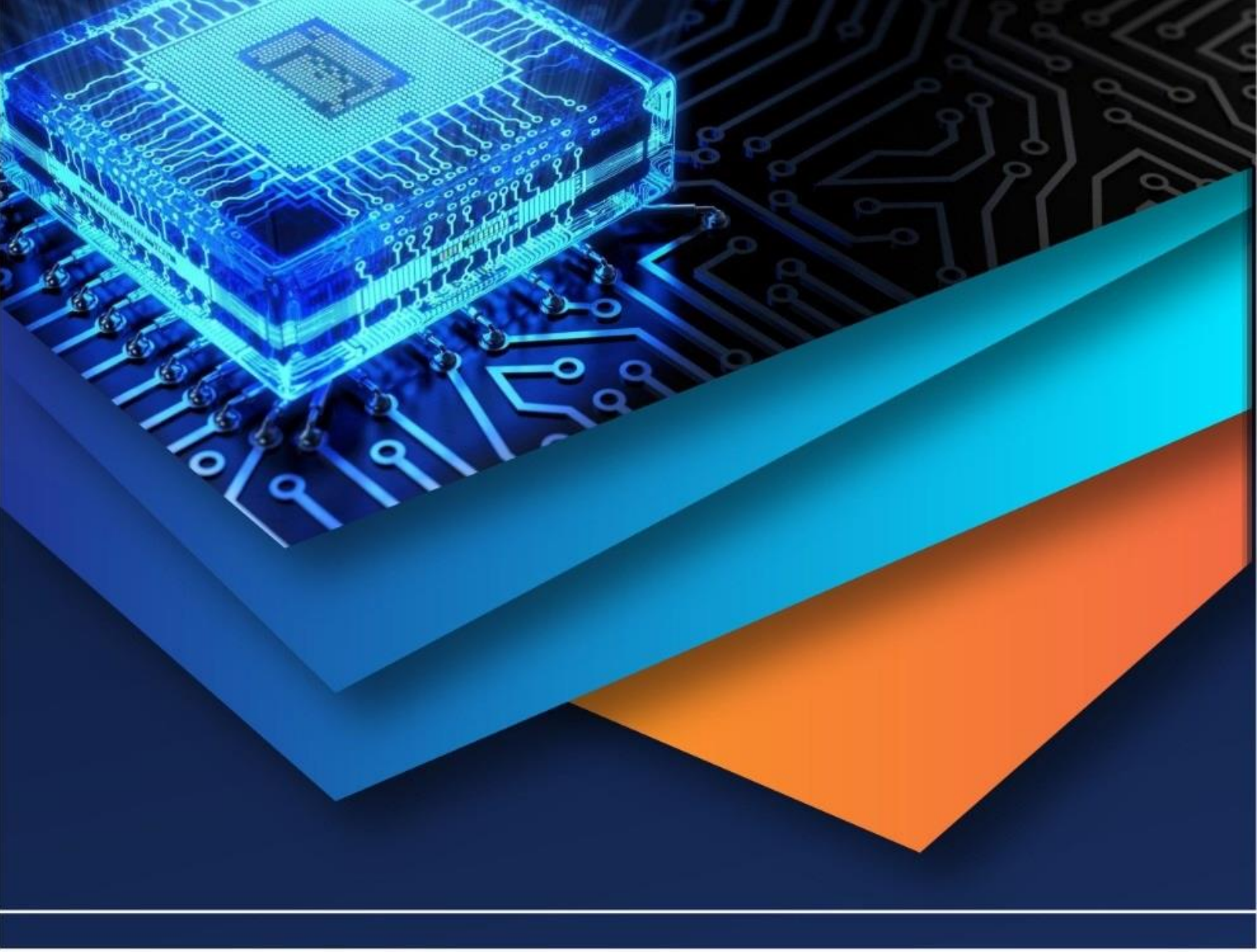

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