iJRASET
International Journal For Research in
Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 5 **Issue:** VI **Month of publication:** June 2017

DOI:

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

Volume 5 Issue VI, June 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

A Low Power 4 Bit Successive Approximation Analog-To-Digital Converter Using 180nm Technology

Jasbir Kaur[1], Praveen Kumar[2]
[1]Assistant Professor, ECE Department, PEC University of Technology, Chandigarh, India
[2]PG Scholar, Electronics (VLSI Design), PEC University of Technology, Chandigarh, India

Abstract: ***In this paper, 4 bit successive approximation analog-to- digital converter (SAR ADC) has been designed. The design is using Cadence tool with 180nm CMOS technology in which supply voltage is 3.3V. The successive approximation has three components which are comparator, control logic and digital- to- analog converter.The SAR ADC is used widely in data acquisition techniques at the sampling rates higher than 10KHz like computer, microcontroller, microprocessor, TV etc. Simulation result shows that proposed successive approximation analog-to-digital converter have a power efficiency or consumption of 3.323mwatt.***
Keywords-- Comparator, Control logic, Digital-to-analog converter.

I. INTRODUCTION

ADC is an integral part of many electronic devices. It is used to convert the analog signal to digital signal. There are various type of ADC like counter type ADC, SAR ADC, pipeline ADC, sigma-delta ADC and flash type ADC. Pipeline ADC are used when higher resolution is required then that of flash ADC is required at the cost of lower sampling rate. Sigma-Delta ADC and counter type are slower in speed. Flash ADC also required larger area. SAR ADC provide good accuracy, good resolution, low cost and good speed. So the best ADC is SAR ADC. This paper is organized as follows. A brief introduction about SAR ADC is given in Section I. In section II, the conventional ADC architecture has been discussed. In section III, the proposed SCR ADC is explained. In Section IV, simulation and experiment result of conventional SAR ADC and proposed SAR ADC is shown. In section IV, conclusion and comparison of conventional SCR ADC and proposed SCR ADC is done.

II. CONVENTIONAL ADC

One method of addressing the digital ramp ADC's shortcomings is the so called successive-approximation ADC. The only change in this design is a very special counter circuit known as a successive-approximation register. Instead of counting up in binary sequence, this register counts by trying all values of bits starting with the most-significant bit and finishing at the least-significant bit. Throughout the count process, the register monitors the comparator's output to see if the binary count is less than or greater than the analog signal input, adjusting the bit values accordingly. The way the register counts is identical to the "trial-and-fit" method of decimal-to-binary conversion, whereby different values of bits are tried from MSB to LSB to get a binary number that equals the original decimal number. The advantage to this counting strategy is much faster results: the DAC output converges on the analog signal input in much larger steps than with the 0-to-full count sequence of a regular counter.

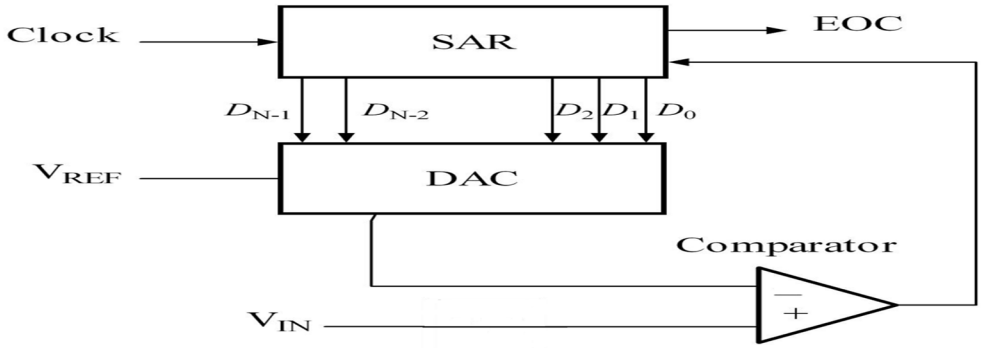


Figure 1: Block Diagram of successive approximation ADC

©IJRASET: All Rights are Reserved

Volume 5 Issue VI, June 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

III. PROPOSED ADC

As discussed in section II the block diagram of conventional ADC is shown in figure1. The design procedure in the proposed ADC has been done by designing each block independently and the output waveform has been verified for each block. The blocks are control logic, Digital-to-Analog converter, comparator. Further in this section the each block is explained in detail its working and interfacing.

A. control logic

Figure 2 show the control logic circuit by using sequencer and code register. The sequencer is a shift register which is initially reset and for every clock pulse it shift '1' through the register. The output of a sequencer set a flip-flop in the coded register and the output of comparator is given as input to each coded register flip-flop. First of all it will set the MSB bit to '1' and remaining bit to '0' if the output of comparator is '1' MSB bit remain at '1' and the next bit is set to '1'. If the output of comparator is '0' then MSB bit is set to '0' and the next bit is set to '1'. This process continues until all bit are done.

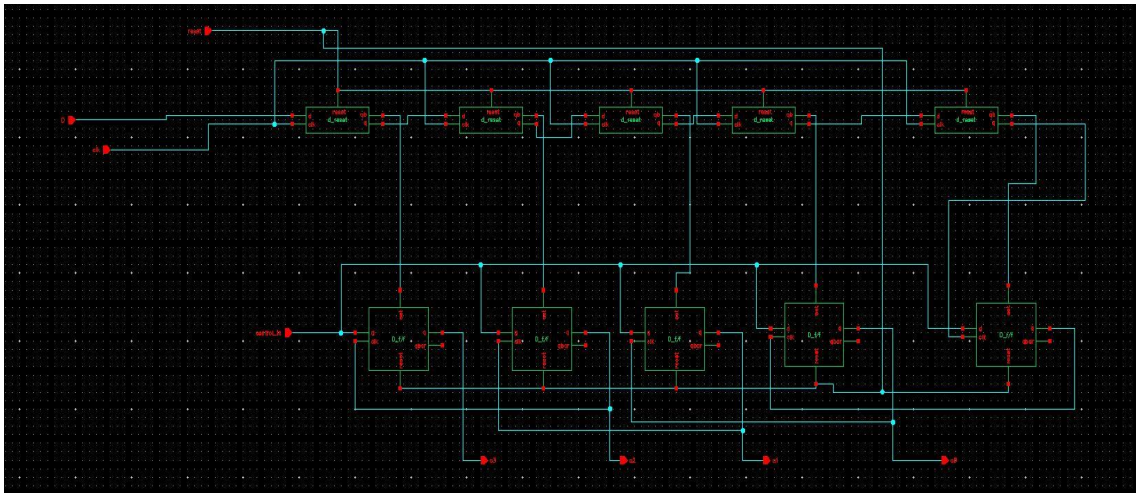


Figure 2: Circuit Diagram of control logic

B. Digital-to-Analog converter

Figure 3 shows the Digital-to-Analog converter circuit it consist of R-2R ladder and a comparator. It is used to convert the digital signal to analog singnal. The bit which near to comparator is the MSB bit and the bit which is far away from comparator is the LSB bit. The expression used to convert the digital signal to analog signal is

$$vout = (vref/2^n)\left(\sum_{i-0}^{n-1} 2^i\, bi\right)\left(1+\frac{rf}{r1}\right)$$

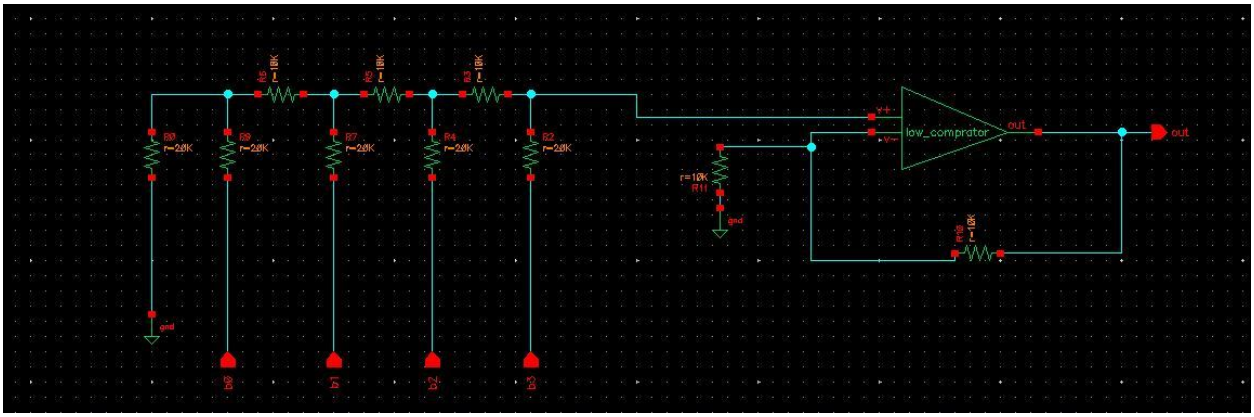


Figure 3: Circuit Diagram of Digital-to-analog converter

©IJRASET: All Rights are Reserved

Volume 5 Issue VI, June 2017
ISSN: 2321-9653

C. Comparator

Comparator used in ADCs plays very critical role. The parameters such as input offset voltage, propagation delay, power consumption and input range of comparator decides the parameters of Successive approximation ADC.

Comparator consumes considerable power in ADC circuits. As the resolution increases, the number of comparator increases and consequently, the power consumed and area also increases exponentially. At

high frequencies, the noise generated in the comparator is considerable. Block diagram of comparator used in designed ADC is shown in Figure 4.

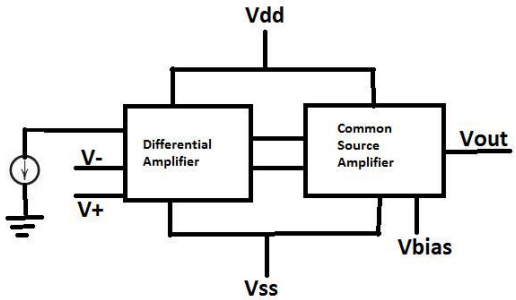


Figure 4. Block diagram of Comparator

Comparator used in flash ADC is designed using CMOS technology so that it consumes minimum power. It consists of two stages

1) Differential amplifier

2) Common source amplifie

3) Differential Amplifier

The active loaded MOS differential amplifier schematic is shown in Figure 5. It consists of two matched transistors, NM0 and NM1, whose sources are joined together and biased by a constant-current source *I*. The constant current source is usually implemented by a MOSFET circuit of current mirror. Generally, each drain of differential amplifier is connected to the positive supply through a drain resistance, but active (current-source) loads are employed here. Whatever type of load is used, it is essential that the MOSFETs not enter the triode region of operation.

Transistor NM0 and NM1 are biased using constant current source which has been implemented using a current mirror circuit i.e. source of NM0 and NM1 are connected to each other and current source is applied to them. Current mirror has been implemented using NM2 and NM3. PM0 and PM1 are used as an active load in differential amp.

$$Differentialgain = \frac{vout}{v1-v2} \text{and } A_d = \frac{1}{2} g_m r_0$$

Where A_d represents the differential gain of the differential amplifier, g_m denotes the transcendence of MOS transistor and r_0 denotes the output resistance of MOS transistor.

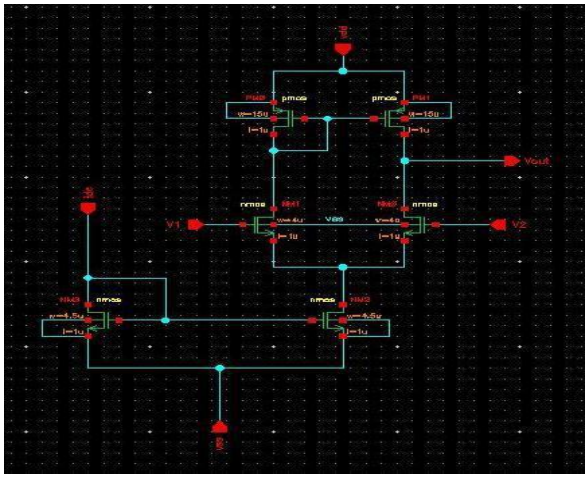


Figure 5: Circuit Diagram of Differential amplifier

©IJRASET: All Rights Reserved

Volume 5 Issue VI, June 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

D. Current Mirror

The circuit of a simple MOS constant-current source is given by Figure 6.

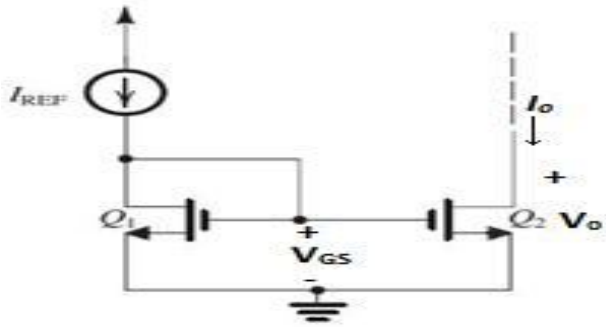


Figure 6: Current mirror circuit

The heart of the circuit is transistor *Q*1, the drain of which is shorted to its gate, thereby forcing it to operate in the saturation mode with

$$I_{D1}=\frac{1}{2}k'_n\frac{(W)1}{(L)1}(V_{GS}-Vtn)^2$$

The drain current of *Q*1 is supplied by current source, which in most cases would be outside the IC chip. Since the gate currents are zero where the current of current source is considered to be the reference current of the current source and is denoted I_{REF}.

$$I_{D1} = I_{REF} = \frac{Vdd-Vgs}{R}$$

Now consider transistor *Q*2: It has the same as *Q*1; thus, if we assume that it is operating in saturation, its drain current which is the output current of the current source *IO*, will be

$$I_0=I_{D2}=\frac{1}{2}k'_n\frac{(W)2}{(L)2}(V_{GS}-Vtn)^2$$

The special connection of Q1 and Q2 provides an output current *Io* that is related to the reference current I_{REF} by the aspect ratios of the transistors. In other words, the relationship between *Io* and I_{REF} is solely determined by the geometries of the transistors.

$$\frac{Io}{Iref} = \frac{(W\ /\ L)2}{(W\ /\ L)1}$$

1) Common Source Amplifier: The Schematic of the Common Source Amplifier is shown in the Figure 7.

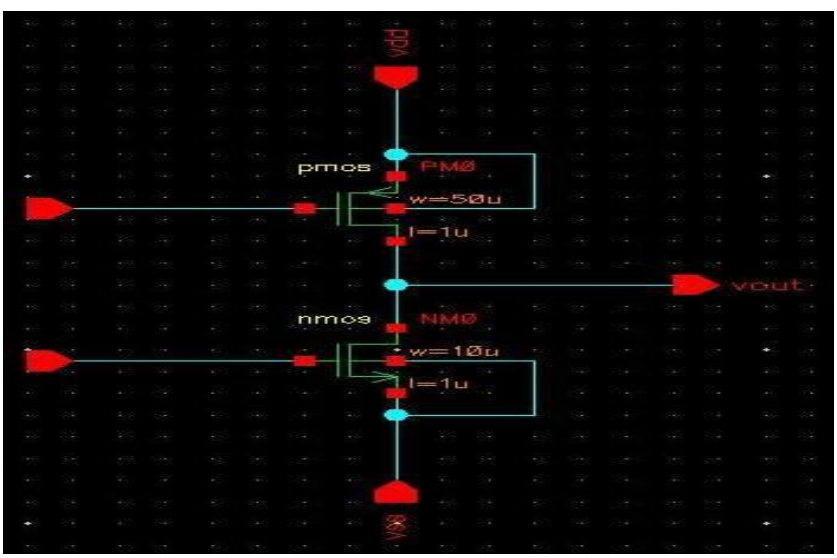


Figure 7: Schematic of Common Source Amplifier

©IJRASET: All Rights Reserved

Volume 5 Issue VI, June 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

As shown in the schematic, the input to CS amplifier is given between source and gate terminal of NMOS and output is taken between source and drain of NMOS. PMOS acts as active load and input given to it keeps the amplifier in saturation region. The input of CS amplifier is the output of differential amplifier and gain of the CS amplifier is such that if the difference between V1 and V2 applied to the differential amplifier is positive then output saturates to the $+V_{DD}$ otherwise $-V_{DD}$

Figure 8 illustrate the complete module of the successive approximation ADC. Each unit has been designed separately and verified by obtaining the output waveforms individually before interfacing and to be used in SAR ADC as a whole unit.

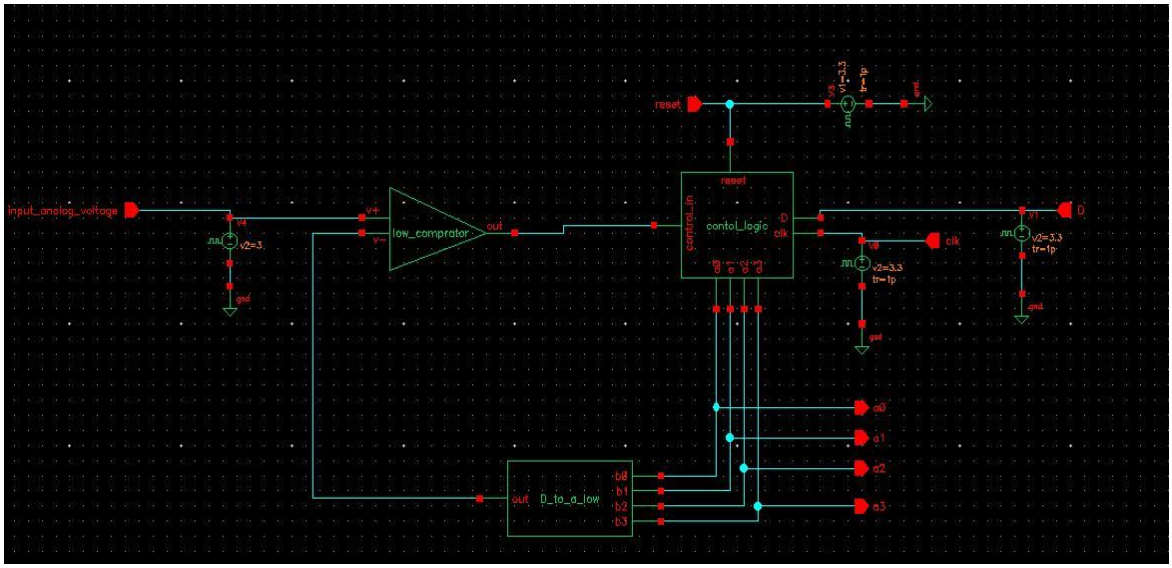


Figure 8: Block diagram of proposed ADC

IV. SIMULATION AND EXPERIMENTAL RESULTS

Simulation of the conventional 4 bit SAR ADC and proposed SAR ADC comparator has been done with Cadence Analog tool using 180 nm technology. For simulation the input voltage is 3.3 V and VDD is also at 3.3V and the output are a3, a2, a1, a0 where a3 is the MSB bit and a0 is the LSB bit the output waveform obtained by tool is shown in Figure 9 and Figure 10 for conventional and proposed SAR ADC respectively. The power consumed is labeled on the output waveform for both ADC.

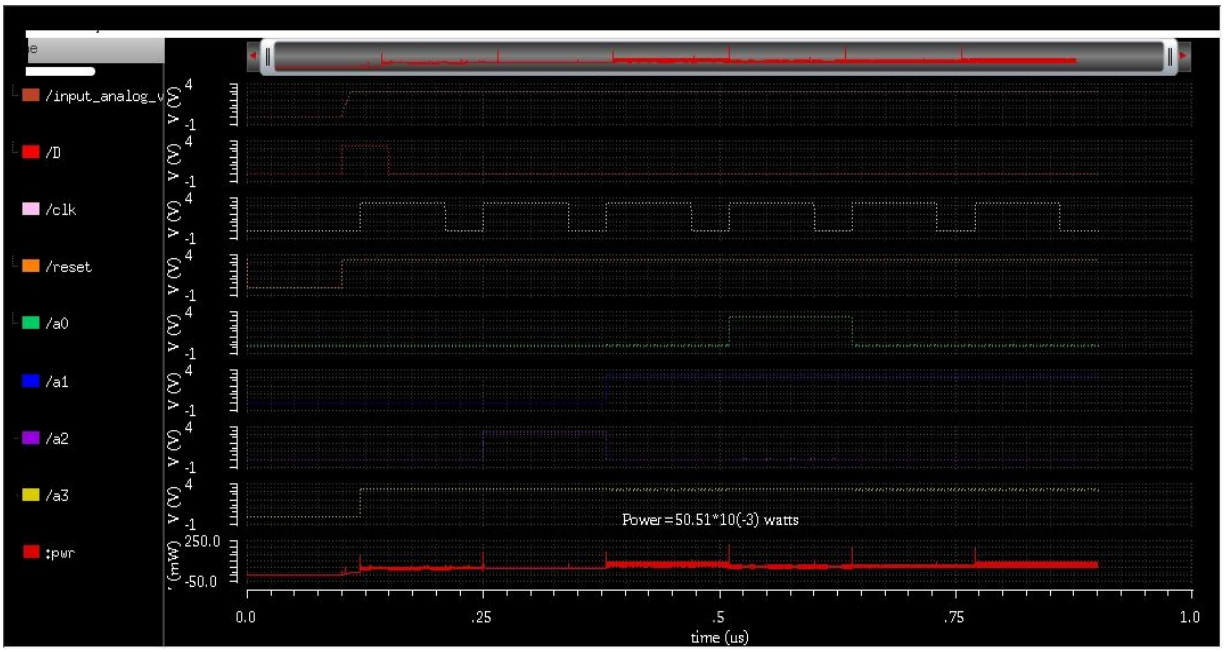


Figure 9: Simulation result of conventional SAR ADC

©IJRASET: All Rights are Reserved

Volume 5 Issue VI, June 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

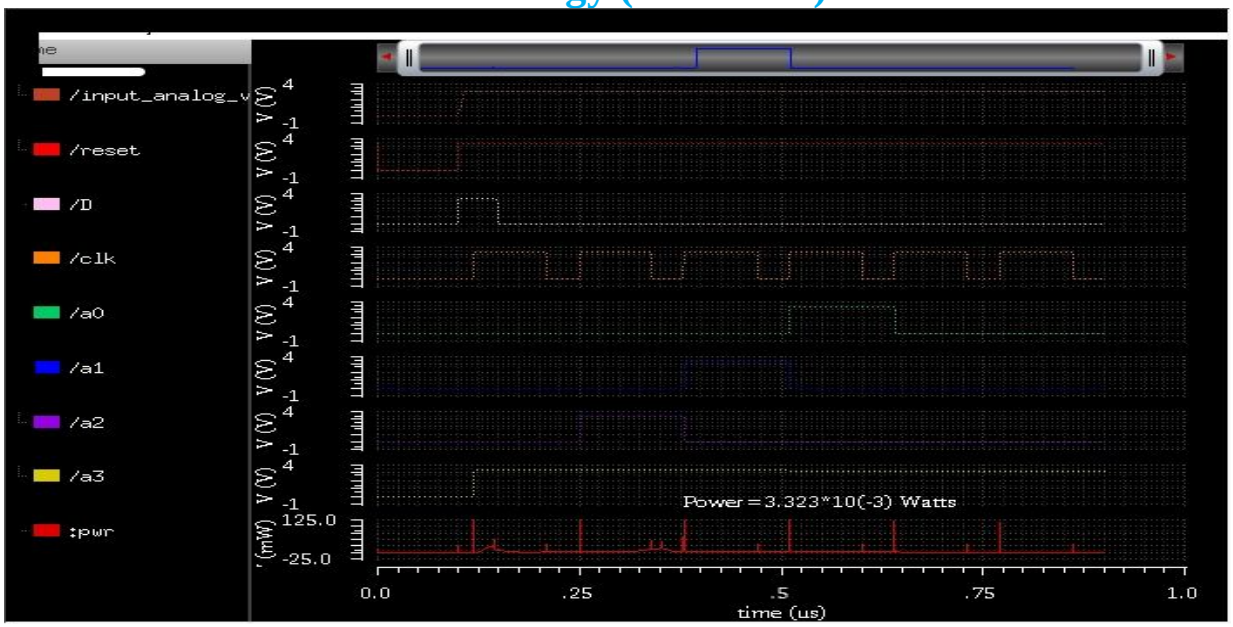


Figure 10: Simulation result of proposed SAR ADC

V. CONCLUSION

The proposed SAR ADC consumes less power. The comparison of power consumed between conventional SAR ADC and proposed SAR ADC is shown in table I. The conventional ADC consume 50.51mW power while the proposed ADC consume 3.323mW. Thus, this proposed SAR ADC ispower efficient and can be used in low power application.

Table I

Comparison of power consumed between conventional SAR ADC and proposed SAR ADC

Arch. / Spec.	Conventional SAR ADC	Proposed SAR ADC	SAR ADC [9]
Technology	GPDK 180nm	GPDK 180nm	45nm
Power Supply	3.3V	3.3V	1 V
Resolution	4 bit	4 bit	4 bit
Input Analog Range	0~6V	0~6V	0~1V
Power Consumed	50.51mW	3.323mW	4mW

REFERENCES

[1] ALGN Aditya, G.RakeshChowdary , J. Meenakshi, M.S.Vamsi Krishna “Implementation of Low power Successive Approximation ADC for MAV’S”, IEEE International Conference on Signal Processing, Image Processing and Pattern Recognition 2013.

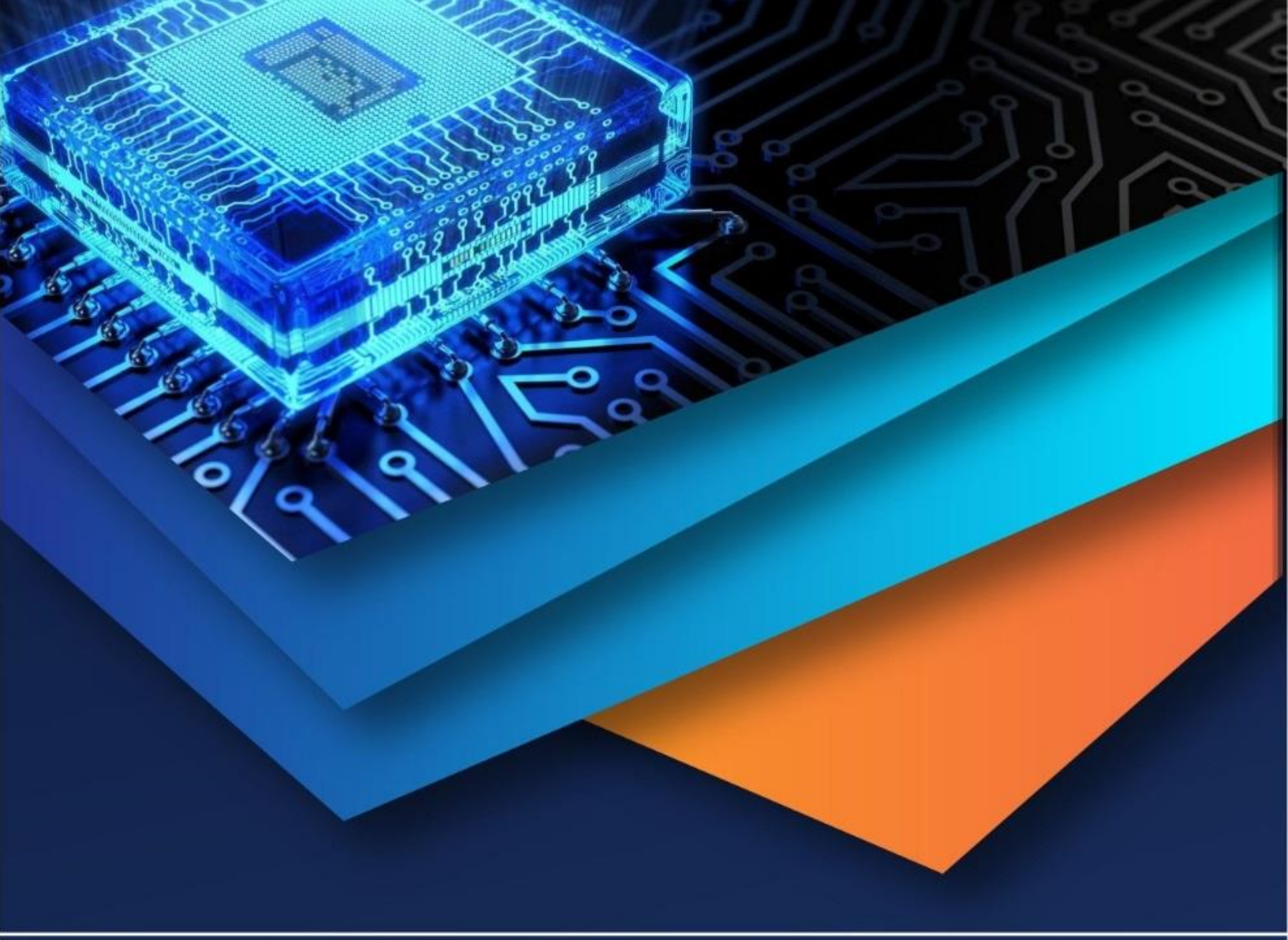
[2] Brian P. Ginsburg and Anantha P. Chandrakasan, "500-MS/s 5-bit ADC in 65-nm CMOS With Split Capacitor Array DAC", IEEE J. Solid-State Circuits, vol. 42, no. 4, pp.739-747 ,Apr. 2007.

©IJRASET: All Rights are Reserved

Volume 5 Issue VI, June 2017
ISSN: 2321-9653

[3] SiamakMortezapour, Edward K. F. Lee "A 1V 8-Bit Successive Approximation Register in standard CMOS process", IEEE Journal of SolidState Circuits, Vol.35, No.4, April 2009.
[4] Young-Kyun Cho, Young-DeukJeon, Jae –won Nam,Jong-Kee Kwon "A 9-bit 80 MS/s Successive Approximation Register Analog to Digital converter with a capacitor reduction Technique" ,IEEE Transactions on Circuits and Systems—Ii: Express Briefs, Vol. 57, No. 7, July 2010.
[5] Pieter J. A. Harpe, Cui Zhou, Yu Bi, Nick P. van derMeijs, XiaoyanWang,Kathleen Philips, Guido Dolmans, and Harmke de Groot "A 26 uW 8 bit 10 MS/s Asynchronous SAR ADC for Low Energy Radios", IEEE Journal of Solid-State Circuits, Vol. 46, No. 7, July 2011.
[6] Guan-Ying Huang, Soon-Jyh Chang, Chun-Cheng Liu, Ying-Zu Lin "A 1-μW 10-bit 200-kS/s SAR ADC With a Bypass Window for Biomedical Applications" ,IEEE Journal of Solid-State Circuits, Vol. 47, No. 11, November 2012.
[7] Weibo Hu, Yen-Ting Liu, Tam Nguyen, DonaldY. C. Lie, Brian P. Ginsburg "An 8-Bit Single-Ended UltraLow-Power SAR ADC With a Novel DAC Switching Method and a Counter-Based Digital Control Circuitry" ,IEEE Transactions on Circuits And Systems—I: Regular Papers, Vol. 60, No. 7, July 2013.
[8] Hur A. Hassan, Izhal Abdul Halin, Ishak Bin Aris , MohdKhair Bin Hassan "Design of 8-bit SAR-ADC CMOS" ,IEEE 2009.
[9] Nilofar M. A. Shaikh, Seema H. Rajput, Shrikant R. Atkarne "Design of SAR Logic for Low Power High Speed SAR ADC", IJAREEIE, Vol. 5, Issue 1, January 2016.

©IJRASET: All Rights are Reserved



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Call : 08813907089 (24*7 Support on Whatsapp)