iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 5 **Issue:** VI **Month of publication:** June 2017

DOI:

www.ijraset.com

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Volume 5 Issue VI, June 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

Review on CMOS Technology &Various Sources of Power Dissipation in CMOS Devices

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Abstract*: The historical background of Electronics Industry tells about the integration of more and more components in a chip to enhance the processing speed and efficiency of any device can be improved. But at the same time, the integrating more number of components leads to increase in power dissipation. CMOS design technology has become the fundamental technology in electronics industry these days. Various electronics equipments are now based on CMOS technology. At the same time, there is a disadvantage of power dissipation or more energy consumption. To reduce power dissipation, the best approach is to study the sources of power dissipation so that the problem is identified and the way to remove it can be achieved.
Index Terms—CMOS, NMOS, Velocity saturation , Hot Electron

I. INTRODUCTION

Power Dissipation is one of the most important parameter that need to be taken care while designing. There is great need of low power dissipation devices as day by day, with more and more integration, the energy dissipation in high. There are hundreds of Electronics gazzates which have overpowered the market and one of the most important requirement is good battery backup. For example, there are Laptops, notebooks, mobiles and so on.

Due to energy consumption in any device will lead to deploy heat sinks which will make device bulkier and costly at the same time the device may not be portable any more. Power dissipation occurs due to computational process involve, hence portable battery requirements is increasing day by day. Nowadays, low power requirement are coming from environmental concern . Modern offices, labs are now furnished with automotive equipments which dissipates lots of power. Thus, low power dissipation has become very thoughtful issue.

A. Historical Background

It started with vacuum tubes before 1947, and in 2017 more and more integrated circuits are evolved and still evolving . The Evolution Process of various technologies can be best described with the help of a flow chart shown in figure 1. The evolution process plays an important role in visualizing further improvements in existing technologies.

Nowadays, a new technology named 'Bi-FET' technology is invented and many other technologies are about be invented , which is entirely a result of visualizing the existing technology's benefits and improving it by associating it with some other technology so that better results can be achieved .

Now since the vacuum tubes were bulkier and high power dissipation components so , these were replaced by transistors and hence IC's came into existence and the era of cramming more and more components on single IC started with Moore's Law. The problem of heat dissipation also increasing exponentially. So the effort is in eliminating those parameters which are influencing device to dissipate more power.

II. CMOS TECHNOLOGY OVERVIEW

CMOS Technology is one of the most important technology in VLSI design. For technology point of view, in CMOS technology we can realize bot N-Channel & P-Channel MOSFETS in three different ways which are:

Start with n-type substrate and form a well with a layer of p-type substrate also known as p-well technology.

Start with p-type substrate and form a n-well layer known as n-well technology.

Twin well or Twin Tub technology in which a very low doped substrate is used and both the layers of ptype and ntype substrates are formed.

Further Twin well technology is divided into two subparts i.e, True twin well and secondary twin well

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ISSN: 2321-9653

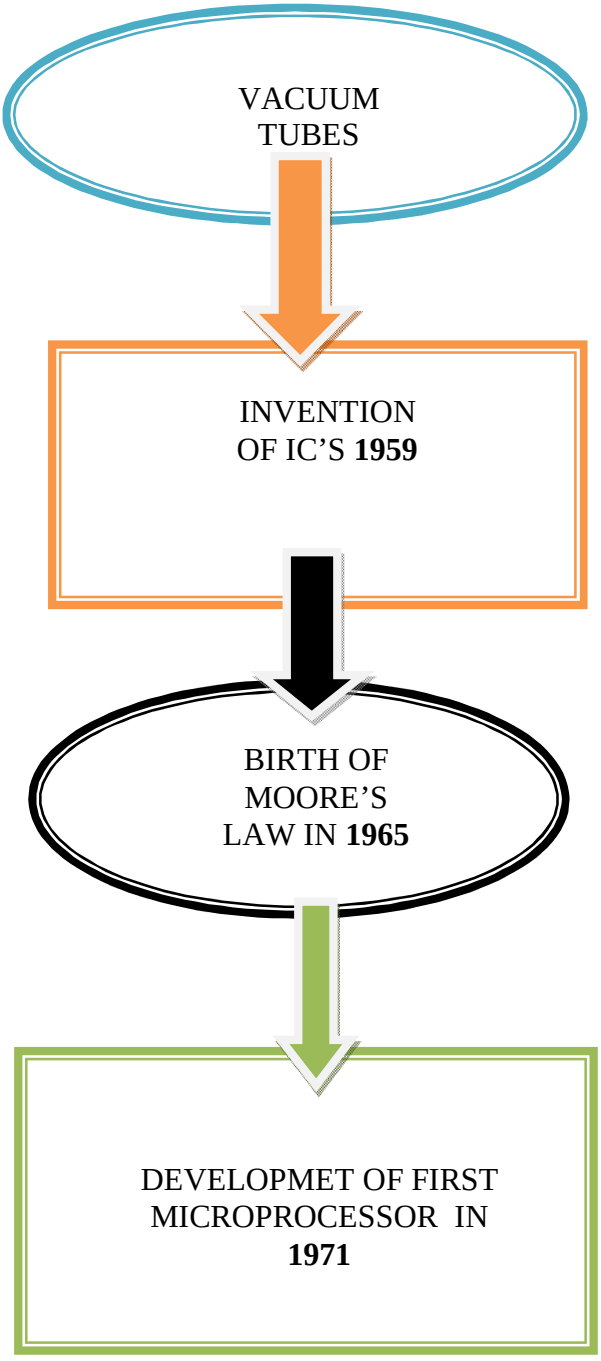

Figure no. 1: Flow Chart of Evolution of Various Technologies

In true twin well, a nearly intrinsic substrate is used and bot p-well & n-well are doped together. The other possibility is to have a secondary p-well or n-well. This is case is basically, an extension of either p-well or n-well technology.
Suppose if p-well secondary CMOS technology is considered the, it has to start with n substrate and then a layer of p type substrate will be used to make a p-well but at the same time a deep implantation hs to be done in n type substrate to avoid *punch through.* It will be clearer with the help of figure 2.

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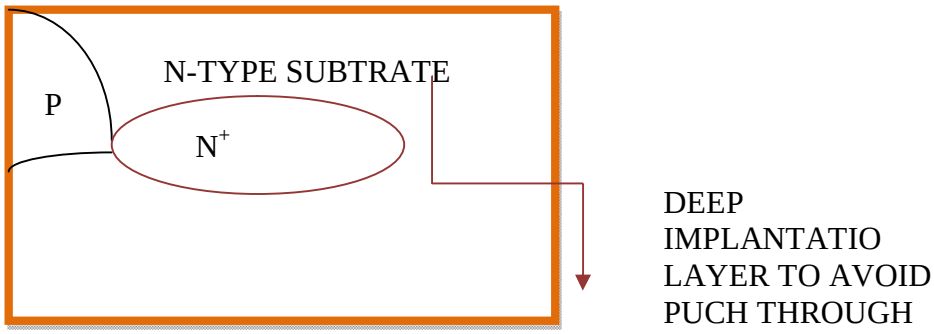

Figure 2 : Formation of p-well

For MOSFET's we use 100 substrate which is universally accepted where 100 shows the oxide charge and interstate space . In N-well Twin well technology, following steps has to be followed;
100 p substrate is used , n-well can be created by doping some of the parts of p type substrate with n type
substrate layer.
For doing that , ptype substrate has to be protected with oxide nitride layer or mask i.e, Si_3N_4 and for rest of the region , there will be phosphorus implantation.
After that , a layer of oxide is formed on the region which is not protected by nitride as shown in figure 4.
Now the next step is to remove the nitride oxide layer as well the oxide layer so that the n well can be formed inside the semiconductor.

A. Step 1: P-Substrate Is Exposed To Oxide Nitride Layer & Phosphorus Implantation

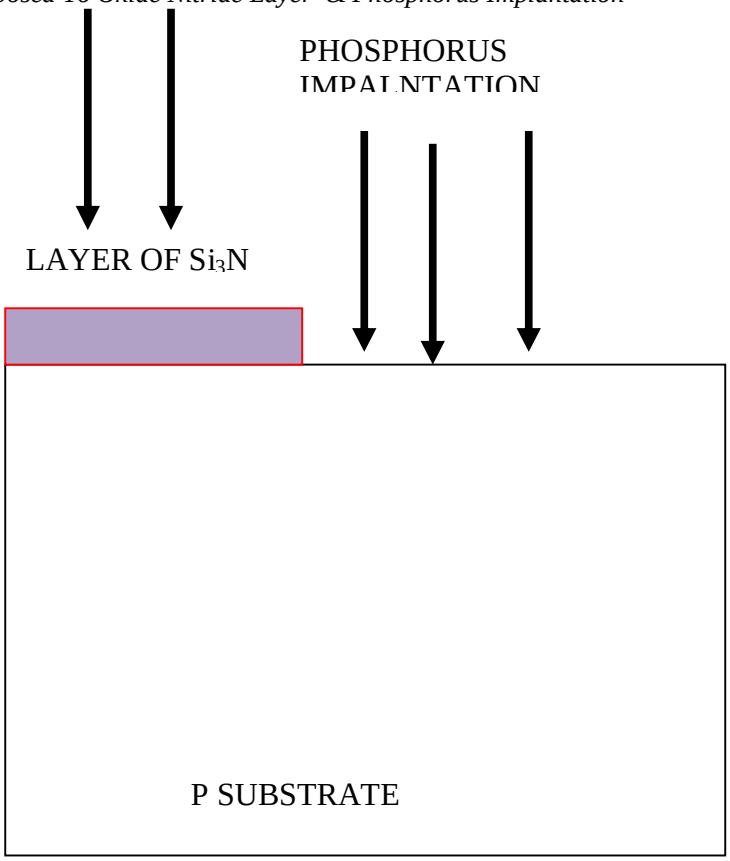

Figure 2 : Formation of oxide nitride layer

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B. Step 2 : Rest Of P Substarte Is Exposed To Oxide Layer

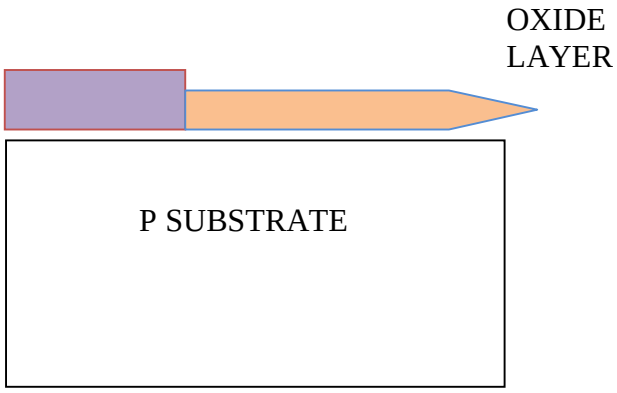

Figure 4 : Formation of oxide layer

C. Step 3 : Removing The Nitride Oxide And Oxide Layer To Form N Well Inside The Semiconductor

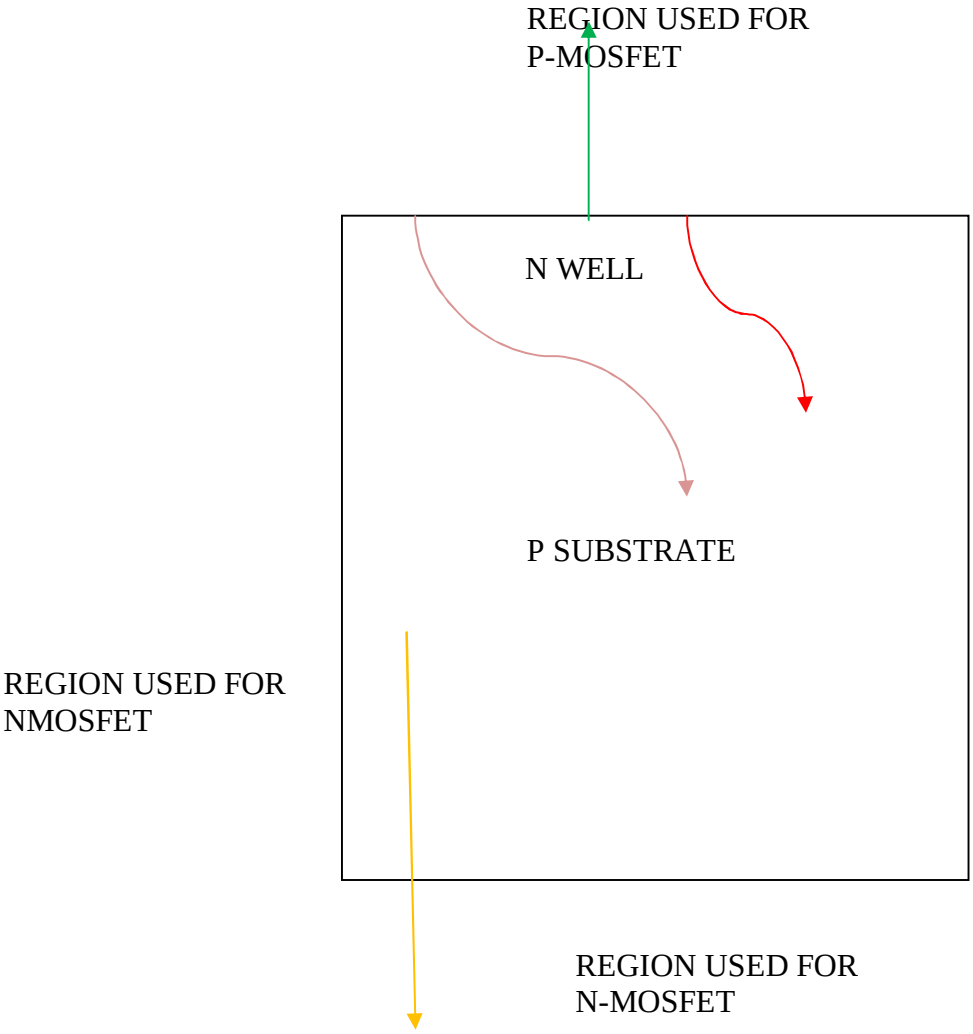

Figure 5 : Formation of N substrate inside semiconductor

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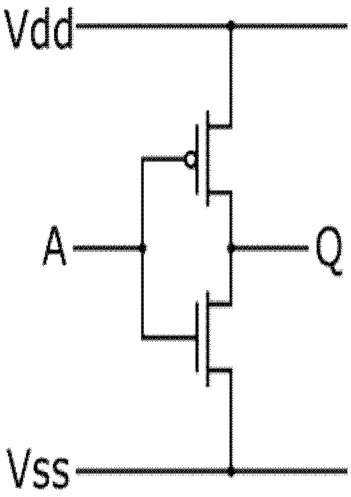

Figure 6 : CMOS Inverter

D. The MIS Structure

MIS stands for metal – insulator and semiconductor .If sources of power dissipation are to be identified then , MOSFET has to be studied deeply. The MOSFET can be divided into metal – insulator and semiconductor layer as shown in figure 7

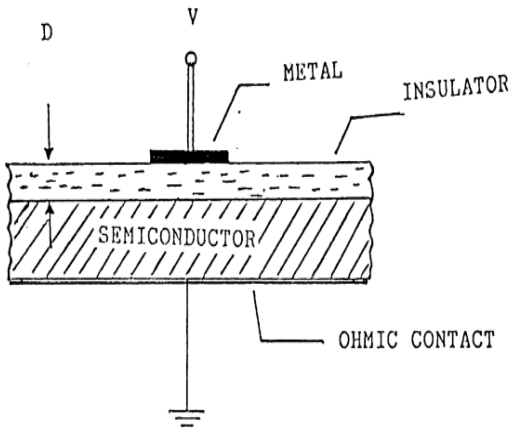

Figure 7: The MIS Structure

From figure 7 , it is clear that

1) Semiconductor layer can be n-type or p-type
2) Insulator is due to silicon dioxide layer
3) Metal is due to metal contact.

E. Ideal MIS Structure

1) The MIS Structure was proposed as voltage-variable capacitor in 1959 by MOLL and by Pfann and Garrett.
2) An ideal MIS is defined as follow:

It consist of following parameters

Bias voltage(V),metal work function (Qm),semiconductor work function (Qs).

KEY POINT The work function is defined as the minimum energy required to escape into vacuum from initial energy of fermi

level.In ideal case of MIS :The difference between Qm and Qs is zero
V=0(zero bias),so the net charge exist in this case is due to the charge present in semi conductor and due to charge present in insulator with equal and opposite magnitude. At different biasing conditions we obtain different results in terms of current and voltage.It will be more clear with Fermi level digram for N-TYPE Semiconductor

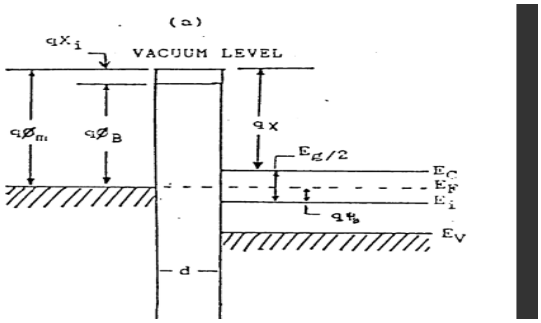

Figure 8 :Fermi level diagram for n-type semiconductor

E_V is is valance energy band, E_F is the Fermi level , E_C is the conduction band. Here fermi level is close to conduction band while in case of p type semiconductor the fermi level will be close to valance band as shown next.

F. P-Type Fermi Level Diagram

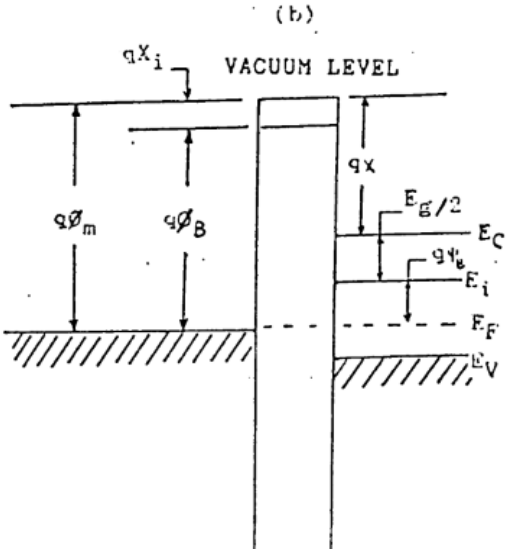

Figure 9: Fermi level diagram for Ptype Semiconductor

In case of non ideal condition ,that is when V is not equal to zero then two cases arises

1) When semiconductor is p-type
2) When semiconductor is n-type

G. Case 1: For Ptype Semiconductor (Negative Voltage Is Applied)

1) When we apply negative voltage to metal plate the top of the valance band bends upward and is close to fermi level as shown in fig
2) This bending result in carrier accumulation i.e , holes near the semiconductor surface known as ‘accumulation case’.

This phenomena is shown in figure 10.

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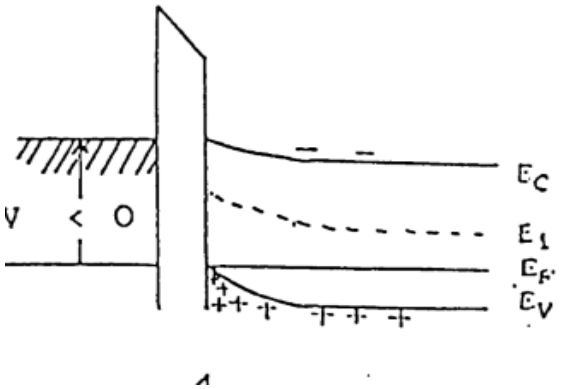

Figure 10 : Accumulation Mode

H. (When Small Positive Voltage Is Applied)

In this case the valance band will bend downwards and results in depletion as shown in figure 11.Hence the majority carriers are depleted.

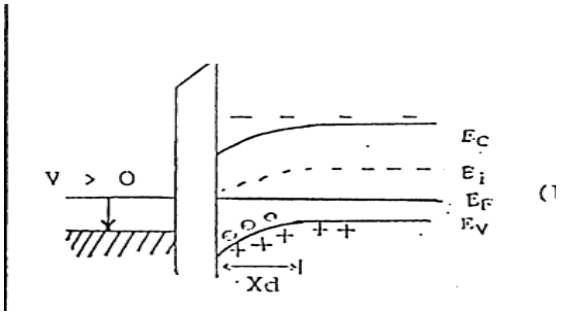

Figure 11 : Depletion Mode

I. (When More Positive Voltage Is Applied)

In this case the intrinsic level will cross over fermi level as shown in figure 12, In this case the minority carrier will increase near surface region and inversion will take place.

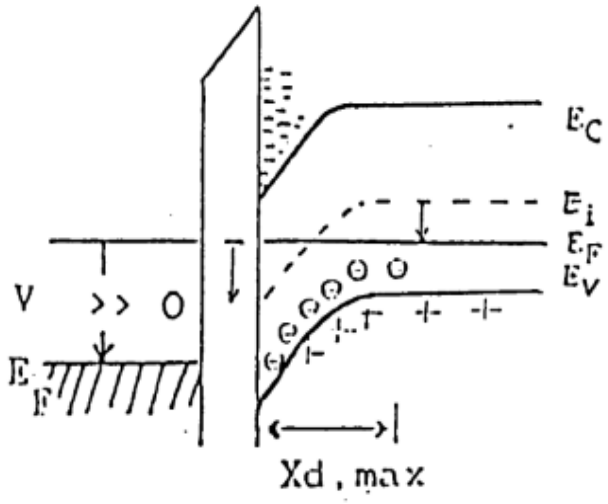

Figure 12 : Inversion Mode.Similarly ,

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J. Case 2: For N-Type Semiconductor (Negative Volatge Is Applied)

With this accumulation mode will happen shown in figure 13

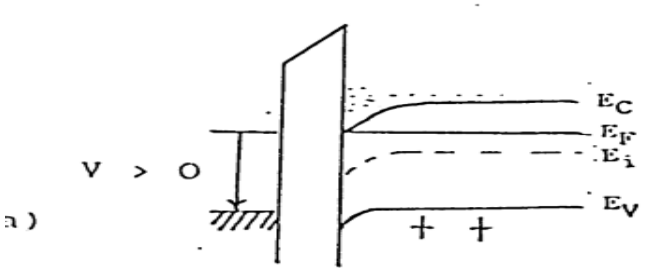

Figure 13 :Accumulation Mode

K. (When Neagtive Voltage Is Increased)

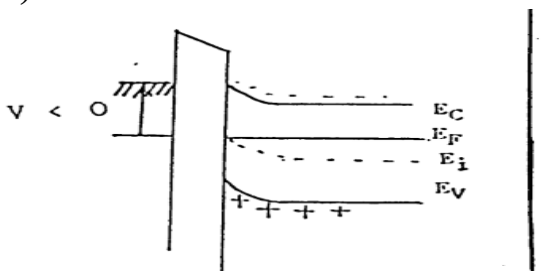

Figure 14 : Depletion Mode

L. (*When Gatevoltage Is Increased)*

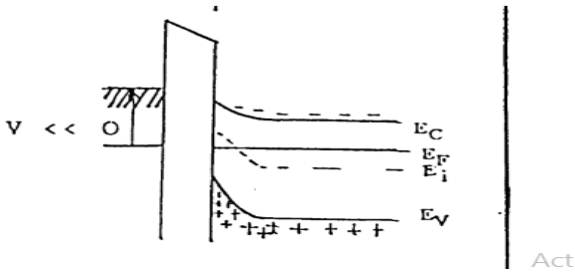

Figure 15 :Inversion Mode

M. Space Charge Region

Surface effects on P-N junction is due to the fact that ionic charges outside the semiconductor surface will induce an image charge in the semiconductor and leads to surface space charge region.

So the above mention depletion ,accumulation and inversion region are known as space charge region.

In case of equilibrium , no d.c current will flow across the space charge region as in this any current will go to insulator with infinite resistance(ideal MIS case)

And the fermi level will also be constant in this case with respect to the equation

$$np=ni^2$$

N. types of Channel effect

There are two type of channel effects

1) long channel effect

2) short channel effect

O. Long Cahnnel Effect

Long Channel MOSFET is defined with width and length are long enough so that the edge effect from the four sides can be neglected.Length of the channel (l)>(drain width + Source width)

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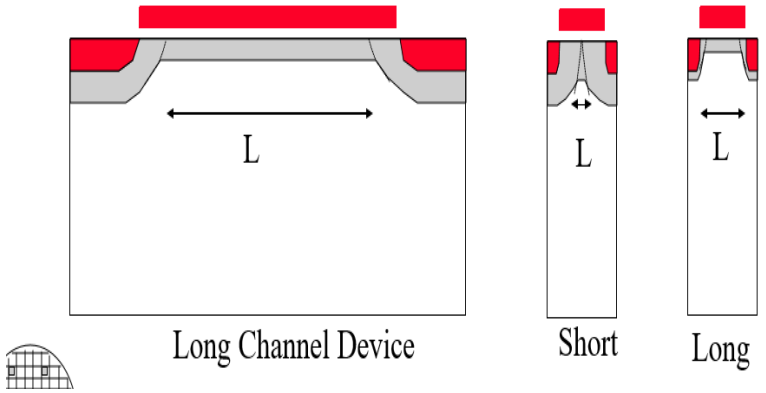

Figure 16: Long Channel Effect

P. Short Channel Effect

MOSFETS with smaller dimensions are known as submicron MOSFET or short channel mosfets . Here the length of the channel is equal to depletion width between source and drain. Before comparing these two kinds of mosfets we need to know following parameters:

1) Threshold voltage
2) Sub-threshold current
3) Pinch off voltage.
4) Threshold voltage is defined as the minimum voltage across the gate and source which allows current flow through the transistor.
5) Sub-threshold current is defined as the current flowing through the transistor before the threshold voltage is applied.
6) Pinch-off voltage is defined as the voltage after which there is no effect of increase in drain to source voltage on the current flowing through the transistor. Short channel MOS are having good processing speed ,requires low operating potential and increase transistor density on the chip. Performance degrades with short channel effect. Serious issues like DIBL , Surface scattering , velocity saturation , hot electron effect , impact ionization.

a) *DIBL*: Increase in drain voltage reduces the barrier face by electrons or holes in the source allowing them to go from source to drain where gate voltage remain unchanged. Gate looses the control of flow of current through the MOS and become as good as redundant. Instead of gate , drain is controlling the barrier which is totally unwanted.

b) Surface Scattering

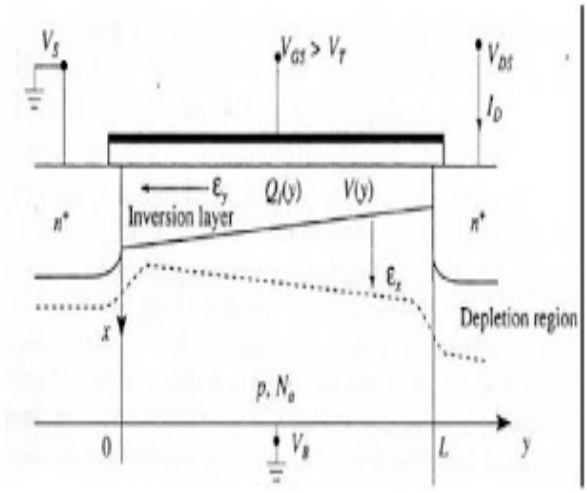

Figure 17 : Surface Scattering

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From figure it is clear that E_x is vertical electric field due to the Vg(gate voltage) and E_y is the horizontal field due to Vds(drain to source voltage).In long channel the E_y is neglected but in short channel it is not neglected.So E_x and E_y will make a resultant zig-zag path , reducing their mobility .As carrier is going in zig-zag maner it will take larger time.Hence it is not desirable.

c) Hot Electron Effect

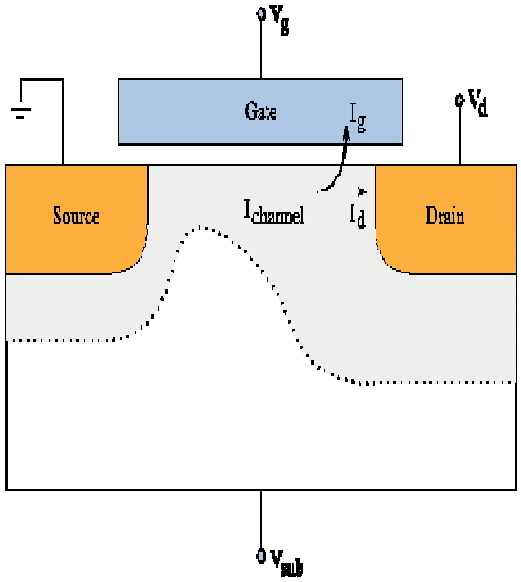

Figure 18:Hot Electron Effect

At high velocity , the carriers drifts near the drain gets extra energy and are known as 'hot electron'. These HOT electrons tunnels through the gate oxide layer and thus reducing the total flow of current from source to drain and reduces the input impedance.

d) Impact Inonization

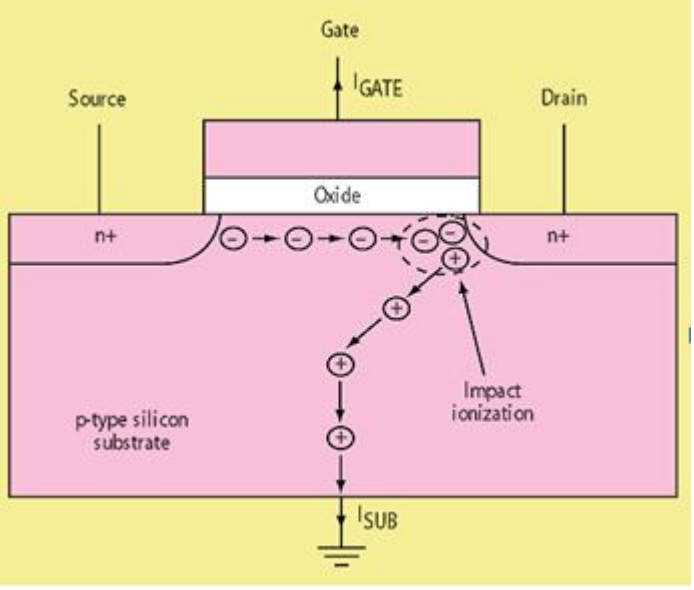

Figure 19 : Impact Ionization

Electron travelling to the drain creates electron hole pair by impact ionization. Secondary electrons are collected at the drain causing current to increase in saturation. Secondary holes are collected at substrate to create a problem of LATCH-UP.

e) Velocity Saturation

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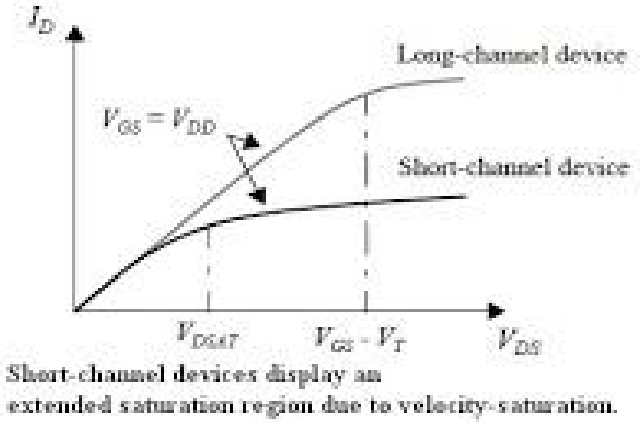

Figure20: Velocity Saturation

Up to certain level the velocity is proportional to electric field.In short channel after a certain effect velocity saturates and has no effect of electric field.When velocity saturates there will be power dissipation.
From previous discussion on short channel effects like hot electron effect , impact ionization , velocity saturation , surface scattering these all leads to power dissipation.

III. EMERGING STRATEGIES FOR LOW POWER

A. Reverse Body Biasing

In this technique basically, voltage to the body(substrate)terminal of MOSFET is provided
so that there is an increase in the threshold voltage which will further decrease the sub-threshold current and ultimately helps in reducing power dissipation.

B. Dual Threshold Cmos

This approach is implemented by using different threshold voltage to decrease the power consumption.It mainly decreases the sub threshold current.But at the same time there is certain increase in the number of MOSFETS which will further altogether increase the delay in the circuit.

C. Multi – Threshold Cmos

Multi- threshold CMOS makes use of both high and low threshold MOS in the same circuit . The main concern is to selectively change the threshold voltages in order to improve the power consumption with improved the circuit speed.
Simple method of making MOS with multiple threshold voltages is to apply different bias voltages(Vb) to the body or the substrate terminal of the transistor. Other method include changing the thickness of gate oxide or the dopant concentration in MOS channel.This approach overcomes the speed limitation which is present in DT-CMOS.

D. Sleep Transistor.

In this technique, the sleep transistors having high threshold value is inserted between the vdd and the pull up network and another transistor is inserted between ground and pull down transistors.These transistors switch ON when circuit is ON and switch OFF when circuit is idle. By cutting OFF the power supply , this can reduce leakage power.But when it is in cut off state , it does not hold states , it destructs the states.

E. Sleepy Stack Approach

This technique divides the single transistor in two half-size transistors. In this approach every half-transistor is added in series so that there is small leakage current.It also adds sleepy transistors to disconnect the power supply and the ground from the network so that there is no power consumption in off mode.

F. Floating Gate Technology

Floating gate MOSFET is technology in which the gate is isolated as it is surrounded by insulator(silicon di-oxide).Electrons on the floating gate are prevented from escaping by the surrounding insulator. Voltage input to secondary control gate couple capacitively to the floating gate , thereby modulating the transistor ‘s channel current .

G. Bulk Driven Technology

As CMOS technology is the basic semiconductor model CMOS IC are almost exclusively fabricated on bulk silicon substrate, for two well known reasons:

1) The arability of electronic grade material produced either by the use of of floating gate technique,

2) Because good quality oxide can be readily grown on silicon, a thing is not possible on germanium or on compound semiconductor.Bulk MOSFET’S are made in silicon wafers having a thickness of approximately 800 micrometer, but only the first micrometer at the top of the wafer is used for transistor fabrication. Interactions between the devices and the substrate give rise to a range of unwanted parasitic effects. One of these is a parasitic capacitance between diffused source and drain and the substrate . This capacitance increases the substrate doping, and become large in submicron devices where doping concentration in the substrate is higher in previous MOS technologies. Latchup, which consists of unwanted triggering of PNPN thyristor structure inherently present in all bulk CMOS structure, becomes a several problem in devices with small dimensions. This creates problem hence we switch to silicon on insulator technology

IV. CONCLUSION

This paper concludes that , due to more integration power dissipation is increasing , hence by inventing more and more technologies , this emerging problem should be eliminated .

This paper has discussed various emerging low power strategies along with the power dissipation sources in brief . There are still so many sources which leads to static and dynamic power dissipation that has to be taken care in future.

V. ACKNOWLEDGMENT

Writing this paper gave us immense sense of knowledge and evoked a zeal of learning and exploring more and more . We would like to thank GOD , Our Parents and every one who helped us.

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Volume 5 Issue VI, June 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

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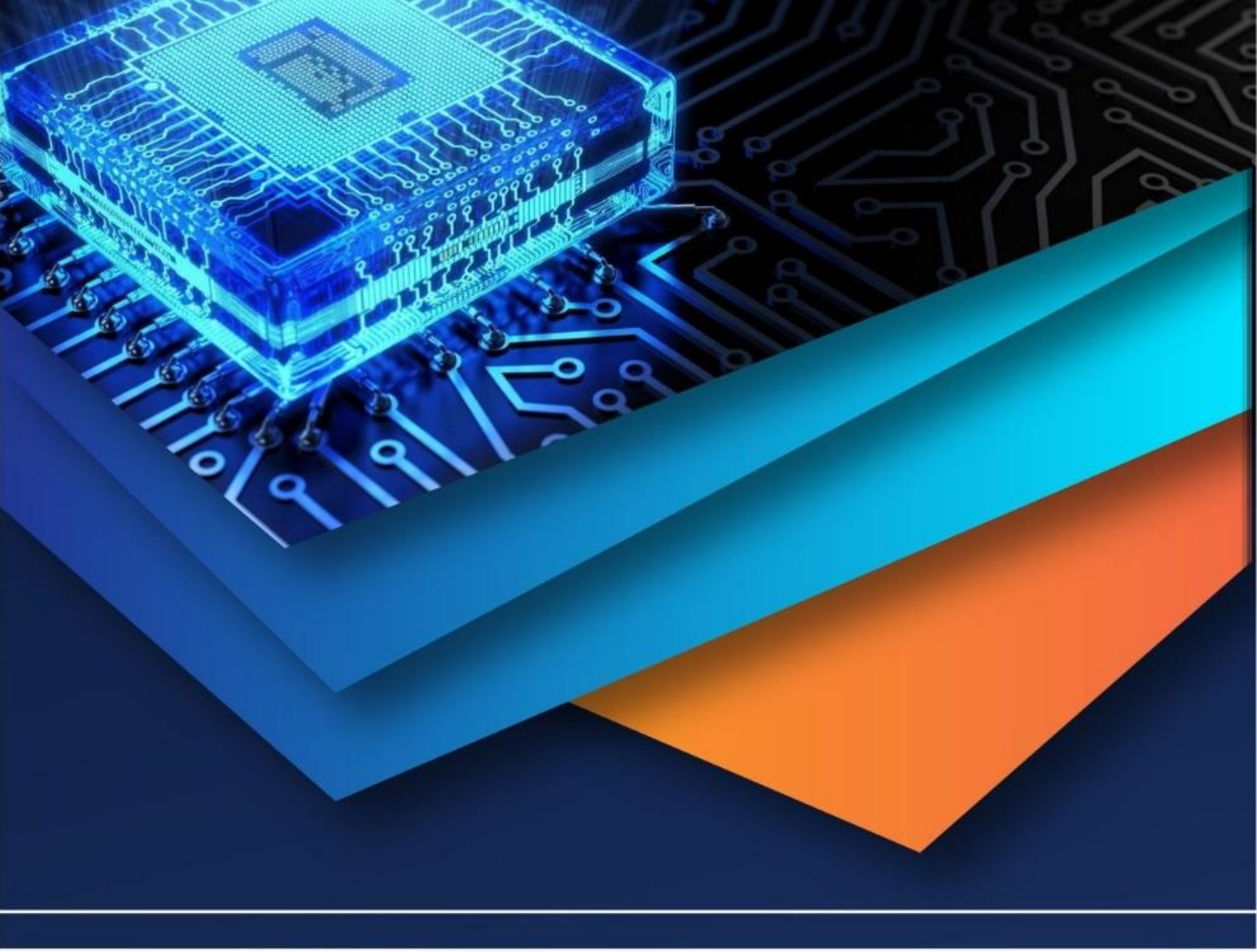

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