iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 5 **Issue:** VII **Month of publication:** July 2017

DOI:

www.ijraset.com

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International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor:6.887
Volume 5 Issue VIII, July 2017- Available at www.ijraset.com

Design of High Speed 16-Bit Vedic and Booth Multiplier

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Abstract: ***In VLSI design the performance of any system is determined by the performance of the elements of the system. Multiplier is the slow element in the system. The multiplier speed is depends on multiplication technique and type of adder. This paper proposes the type of architecture of 16*16 Vedic and Booth multiplier. The code is implemented in XILINX ISE 14.5 software. The combinational path delay of 16*16 bit Vedic and booth multiplier obtained after synthesis is compared with existing multiplier and found that the proposed Vedic multiplier circuits seems to have better performance in terms of speed.***
KeyWords: ***VLSI, Vedic multiplier, Booth multiplier, XILINX, etc.***

I. INTRODUCTION

Multiplication is one of the fundamental functions in arithmetic operations. In a Digital Signal Processors multipliers are the key components. Since multiplication dominates the execution time of many DSP algorithms, so there is need of high speed multiplier. The demand of high speed processing is increasing in computer and DSP application. Efficient arithmetic operations are important to achieve the desired performance in many real-time signals.

Hence continuous efforts are taken to improve the performance of multiplier by reducing the speed. There are several methods have been used for multipliers such as Braun-Array, Baugh-Wooley method of two's complement and Booth's algorithm is the most successful method for multiplication.

In this paper a simple 16*16 bits multiplier is proposed which is based on Urdhva tiryabhyam sutra of Vedic mathematics and on Booths algorithms. The two numbers of 16 bit each are multiplied by using Vedic maths. The main concept behind this is that to reduce the propagation delay of the architecture which is the drawback of Booth's algorithm. As the number of bit increases in the Booth's algorithm delay increases noticeably and for Vedic mathematics as number of bit increases delay increases slightly. In the end we have compared the tow algorithms on the basis of certain parameters and prove that Vedic mathematics is the best way to multiplication of higher number of bits like 16*16 bit.

II. BOOTH ALGORITHM

The Booth's multiplier based on Booth's algorithm. This method is given by "Andrew Donald Booth". The given flowchart describes the method.

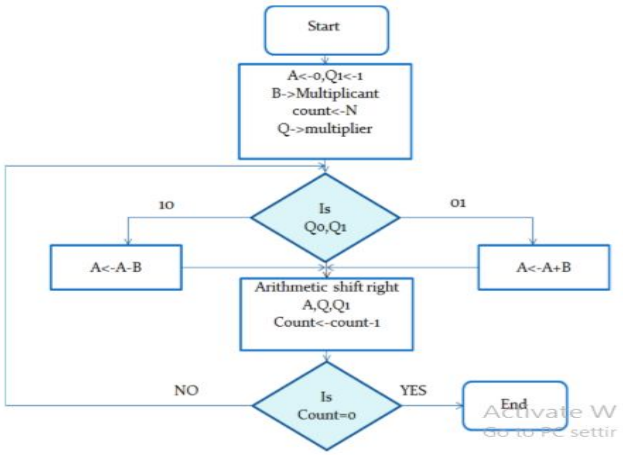


Fig. 1. Flow chart for Booth algorithm

The Booth's multipliers scan the three bits at time to reduce the number of partial product. These three bits are the two bits from the present pair and third bit from high order bit of an adjacent lower order pair.

A. From above Flow Chart we have Algorithm as follows

1) The multiplier and multiplication are placed in Q and B registers respectively.
2) A one bit Q(-1) register is placed at the least significant bit of Q(0) of register Q.
3) The final results appears in A.
4) A and Q(-1) registers are initialized to 0. Earlier days this Booth's multiplier is very suitable for multiplication. This will give the accurate result of multiplication.
5) Multiplication of no. Is one in n cycle
6) In each cycle Q(0)and Q(-1) are examined. i if Q(0) and Q(-1)are (1-1 or 0-0) then all the bits of A, Q AND Q(-1) registers shifted right by 1 bit. ii if Q(0) and Q(-1) are 01 then multiplication is added with A. After addition A Q and Q(-1) registers are shifted right by 1 bit. iii if Q(0) and Q(-1) are 10 then multiplication is substracted from A. After substraction A Q and Q(-1) registers are shifted to right by 1-bit
7) The final result appears in A.

In this multiplier has some drawback. The drawbacks can be overcome by designing suitable multiplier for 16*16 bit multiplication. We will design the new multiplier as Vedic multiplier by using the concept of Vedic mathematics.

III. VEDIC MULTIPLIER

Vedic multiplier is based on Vedic mathematics. Vedic mathematics is the ancient method of mathematics. It was rediscovered from Vedas in between 1911 to 1918 by Sri Bharti Krishna Ttirthaji (1884-1960). Who was mathematician and Sanskrit scholar. The Vedic mathematics is based on the 16 sutras of Urdhva Tiryagbhyam. It simply means that "vertically and crosswise multiplication". It involves minimum no. of calculations, it reduces the space, save the computational time and it is applicable in all cases of multiplication. This method is most efficient when the number of bit increases in multiplication.

The structure of this method is shown in the fig-2 from this we get clear idea about "vertical and crosswise multiplication". For multiplication of 4 bit numbers the process is divided into 7 steps. The first no. is X3X2X1X0 which is multiplier and second no. is Y3Y2Y1Y0 which is multiplicand as shown in step 1 of the figure.

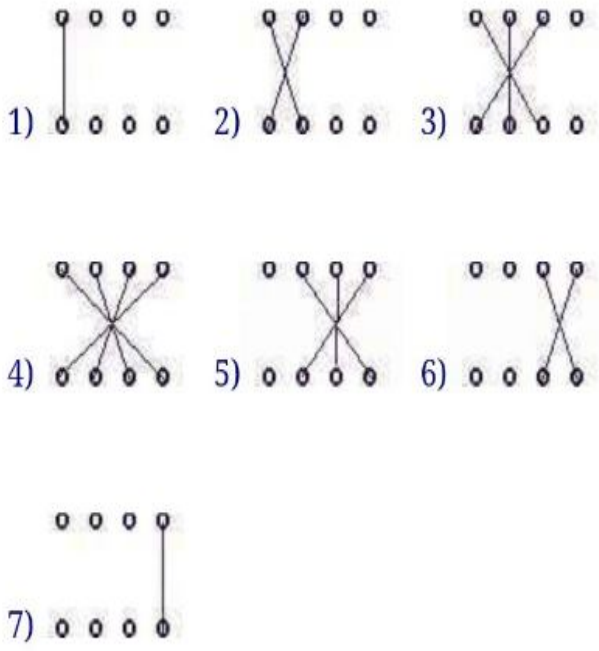


Fig-2:-Vedic method for multiplication of 4-bit binary number

The LSB(least significant bit) of multiplier is multiplied with LSB of the multiplicand and the result of this multiplication is stored as the LSB of the final result. Then as shown in the step2 of the above figure the LSB of the multiplier is multiplied with second higher bit of multiplier is multiplied with LSB of multiplicand and second higher bit of multiplier is multiplied with LSB of multiplicand and then these two partial product are added, after adding these two numbers the LSB of addition is taken as the second higher bit of the final result and remaining bits of the addition are taken as carry bit and this carry can be of multi-bit. Then follow the steps which are given in above figure and after that we get result of 4-bit multiplication.

In this paper we have done 16-bit multiplication and for that we require different modules of the 2-bit, 4-bit, 8-bit Vedic multiplier. the 16*16 bit Vedic multiplier, this multiplier is implemented from the 8*8 multiplier. in this diagram X0 to X15 are the bits of first digit and Y0 to Y15 are the bits of second digit. For 16*16 multiplier we require four 8*8 multiplier and three adders after doing the procedure as shown in fig-3, we will get the result of 16*16 multiplier and the result obtained is of 32 bits. The adder used in this proposed work is CSA adder which minimizes partial product.

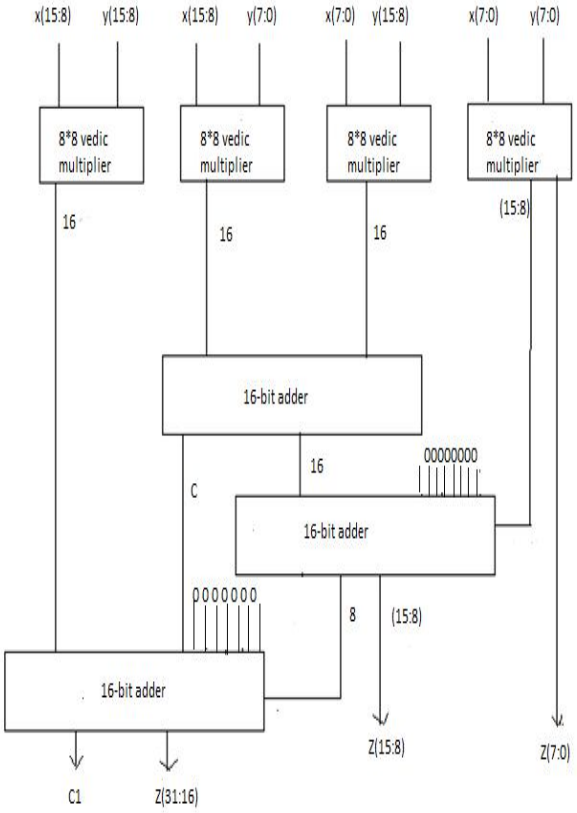


Fig-3:-16*1 Vedic multiplier by using CSA adder

IV. IMPLEMENTATION ON XILINX SOFTWARE

Now we are moving towards main programming parts. Using the Vedic multiplier and Booth multiplier we have to develop a program. In this paper the 16*16 bit multiplier is designed in VHDL (very high speed integrated circuits hardware description language). Synthesis and simulation was done in XILINX ISE 14.5. project navigator and simulator integrated in the XILINX package. XILINX is software which is purely based on the VHDL language. VHDL is Very Large Scale Integrated Circuit Hardware Description Language. We have performed our programming using the Vertex6XC6VCX75T FF84-2. Integrated Software Environment is a software tool produced by Xilinx for synthesis and analysis of HDL design, enabling the developer to synthesize their design, perform time analysis, examine RTL diagrams, simulate a design reaction to different stimuli, and configure the target device with the programmer. It includes ISE simulator which we can use for functionality verification of program. The programming is divided into 4 parts. For developing the multiplier 16*16 bit, we have to first develop the multiplier of 2*2, 4*4 and 8*8

V. EXPERIMENTAL RESULT

The result of the 16*16 Vedic and Booth multiplier is given in the figures below in which 16-bit number is in binary form. Also the RTL schematic of Vedic and Booth multiplier is given.

Fig-4:-simulation result of Booth multiplier

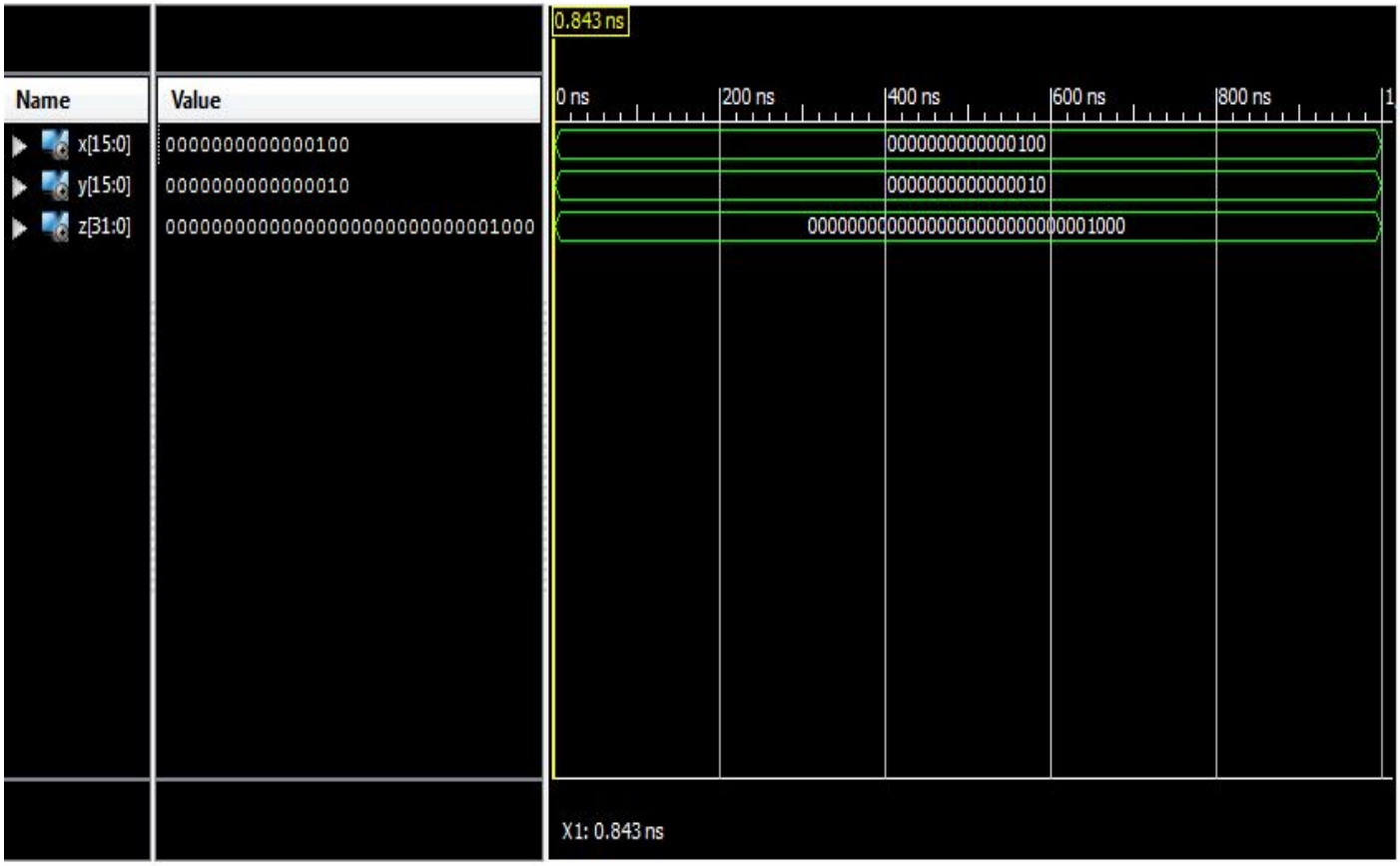
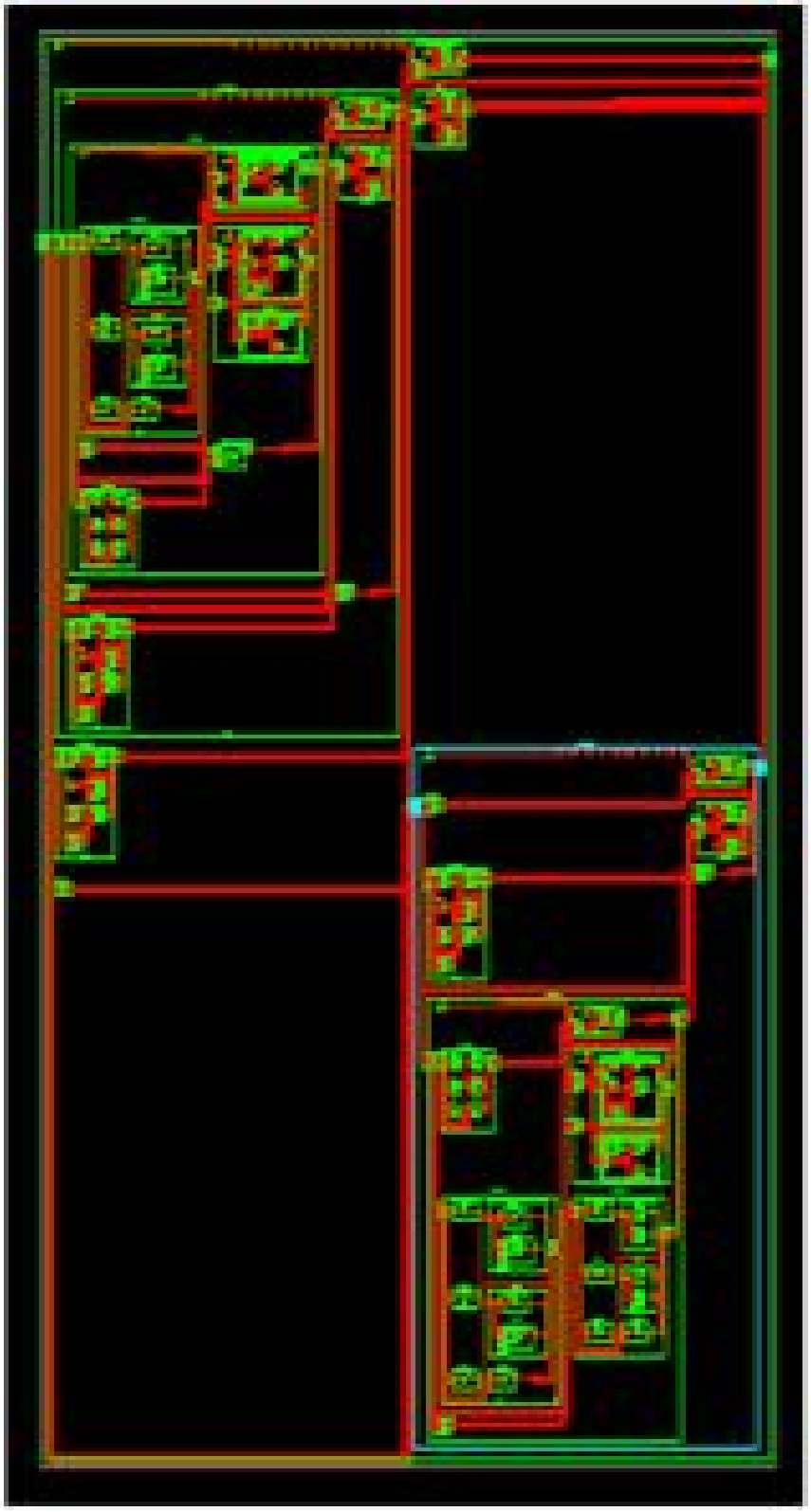


Fig-5:-simulation result of Vedic multiplier

Fig. 6. RTL schematic view of Vedic multiplier



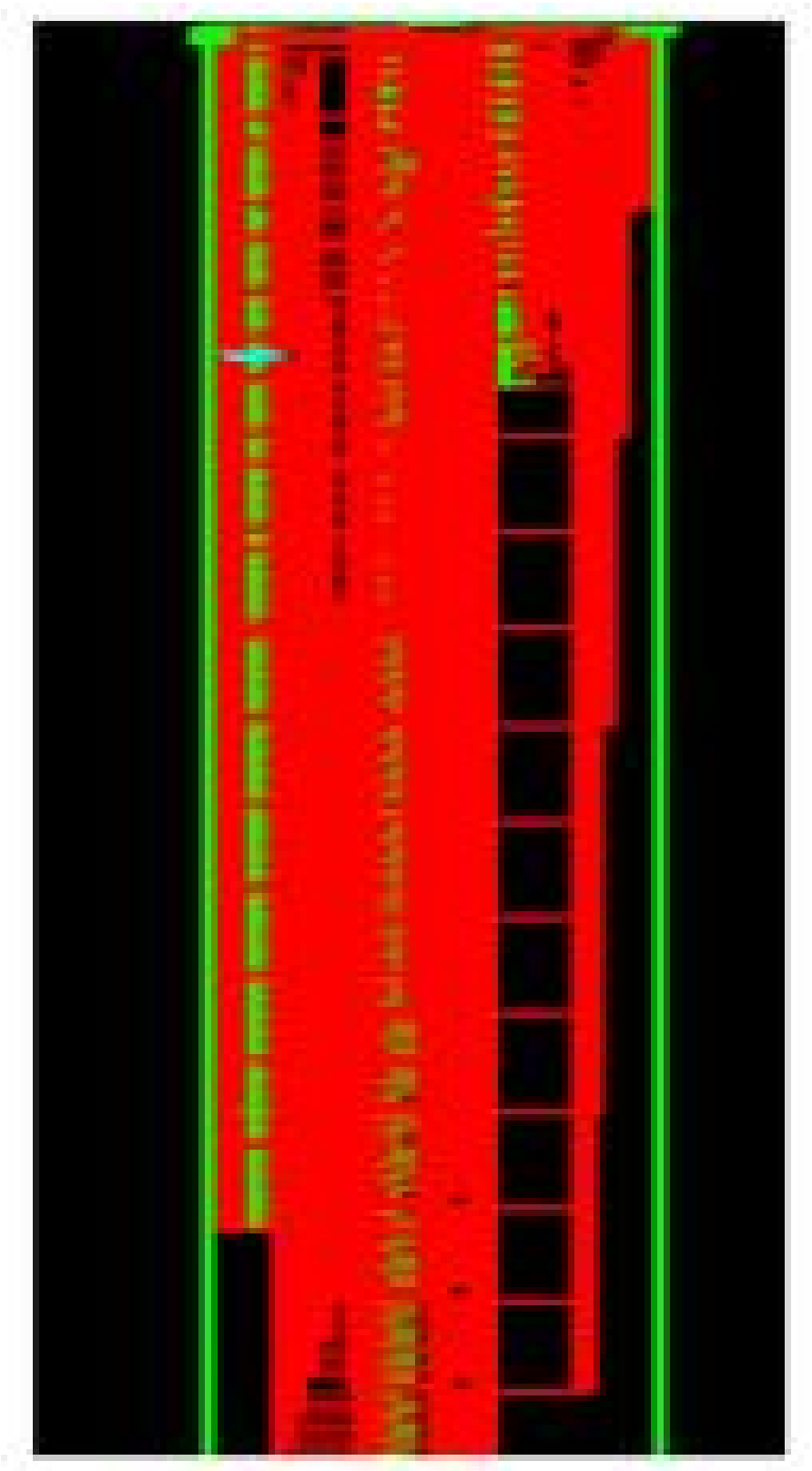


Fig-7:-RTL schematic view of Booth multiplie

REF. PAPER	NAME OF MULTIPLIER	DELAY (NS)	NO.OF SLICES	NO. OF 4 INPUT LUTS	NO.OF BOUNDED IOBs	DEVICE/ FAMILY
Proposed design	Booth multiplier	22.12	752 out of 46560	-	64 out of 240	Vertex6 XC6VCX75T FF84-2
Proposed design	Vedic multiplier	15.27	603 out of 46560	-	64 out of 240	Vertex6 XC6VCX75T FF84-2

Table I-Result of device utilization of proposed method between Booth and Vedic multiplier

REF. PAPER	NAME OF MULTIPLIER	DELAY (NS)	DEVICE/ FAMILY
[3]	Vedic multiplier (HALF ADDER)	27.14	Vertex6 XC6VCX75T FF84-2
Proposed design	Vedic multiplier (CSA ADDER)	15.27	Vertex6 XC6VCX75T FF84-2

Table II-comparison of 16*16 existing with proposed Vedic multiplier

From this table we conclude that delay required for Vedic multiplier using CSA adder is 15.27 ns is less than existing method.

VI. ACKNOWLEDGEMENT

we would like to thanks Mr. P. R. Indurkar, Associate Professor, Electronics and Telecommunication Department, B.D.C.O.E. for his valuable suggestion .we would thanks to our college for providing facilities which helps us in our research work. We also express thanks to our parents, friends and colleagues.

VII. CONCLUSION

The proposed Vedic and Booth multiplier is simulated using XILINX ISE 14.5. The comparison between proposed and existing multiplier is shown in table-2. From the table-1 the Vedic multiplier is superior in speed and delay than the Booth multiplier.

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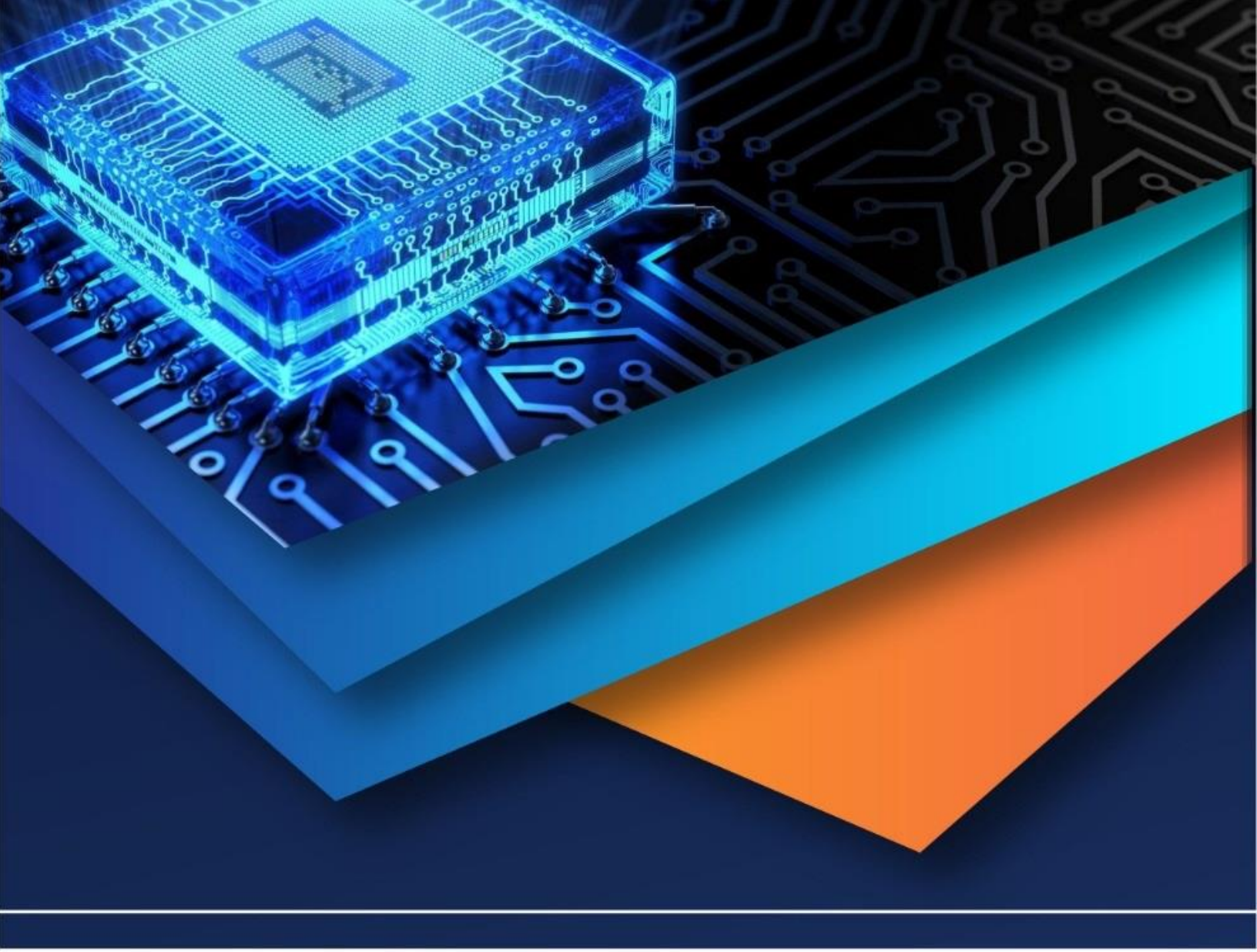

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