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High-Rapidity and Power-Efficient Carry Skip Adder Performance with AOI and OAI Skip Logic

Amrutavarshini S H[1], Mr. S Pramod Kumar[2]
[1]*PG student/ VLSI and ES, ECE, Kalpataru Institute of Technology Tiptur, Tumkur, India,*
[2]*Asst. Prof, ECE Department, Kalpataru Institute of Technology Tiptur,Tumkur, India*

***Abstract:** In this paper compare to conventional one the new structure of adder contains high speed and uses less energy. The concatenation and the speed and the incrementation scheme can be applied to increase the speed and efficiency of the conventional carry skip adder structure. In CSKA structure the Multiplexer can be used as a skip logic. But in this structure it suggested to replace Multiplexer by the AOI (And Or Invert) OAI (Or And Invert) skip logic. The structure may contain both stages; one is Fixed size stage and another one is Variable size stage. Ultimately Hybrid Variable latency at extension of the suggested structure, which lesses the utilization0f the power without making an impact at the speed which is representing a speed.This extension utilizes amended parallel type structure , basically for segmenting the feeble time thus capaciting at the further reduction of voltage suggested structure are assesedby making a camparision of some parameter that is speed and power with other type of adders utilizing a forty nm static CMOS in technology for a extensive range of supply voltage.*
***Key Words:** Carry skip adder(CSKA), Ripple carry adder(RCA), AOI, OAI, Concatenation*

I. INTRODUCTION

In most of the circuits adders are the commonly used unit. Adders are the basic building block in addition, subtraction, multiplication and Memory addressing units. Improving the Adder speed and performance and also reduce the power used is the Main azenda of the designer.

Adders can be differentiated by their speed, power and performance. Some commonly used adders are Ripple carry adder (RCA),Carry select adder (CSLA), Carry skip adder (CSKA), and Parallel prefix adder (PPAs). First considered the RCA; it is the combination of the cascading connection of the Fulladder (FA) in series. Fulladder structure contains some basic gates; it adds two binary digits at any stage of ripple carry adder. Critical path delay is the disadvantage of the Ripple carry adder. In proposed hybrid carry skip adder the parallel prefix adder is the main component used. Different types of PPAs are their; but in this article ,the circuits uses the brunt kung adder. Proposed hybrid CSKA structure can be implemented to reduce the delay and increase the speed and performance.

Proposed hybrid variable CSKA structure can be obtained by the replacing some of the middle stages in CI-CSKA structure with aPPA. Modification is achieved by making use of parallel prefix adder.

II. CARRY SKIP ADDER

It is one type of adder implementation; it can be used to improve the delay of the Ripple carry adder (RCA) also with small effort compared to other adders. The carry skip adder comes under the category of a by-pass adder and it uses a ripple carry adder for an adder implementation. This adder is an efficient one because of its area and power consumption. CSKA may be implemented using FSS and VSS where the highest speed may be obtained for the VSS structure.

III. CONVENTIONAL CARRY SKIP ADDER

Conventional carry skip adder contains some of the functional elements like cascading connection of fulladder chains, block of ripple carry adder (RCA), and 2:1 multiplexer. In this structure multiplexer act as a skip logic. RCA blocks are connected each other through this multiplexer. The input of the multiplexer are the carry input of the stage and the carry output of its RCA blocks and the product of propagation signals is bused as a selector signals of the multiplexer. The carry skip adder consider that Ai, Bi are the inputs to the fulladder. The propagate signal Pi is given by

Pi = Ai + Bi where (i = 1,2,3,……N).

Consider the N bit CSKA it consists of Q stages is given by Q = N/M if carry propagate (cp) equals to the one in a particular stage then cout of that is nothing but cin of the stage.

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In each stage inputs to the 2:1 mux are the carry input of that stage and carry out of particular RCA block. If the carry propagate (cp) is zero the delay is similar to RCA. The structure of conventional carry skip adder is shown in below figure.

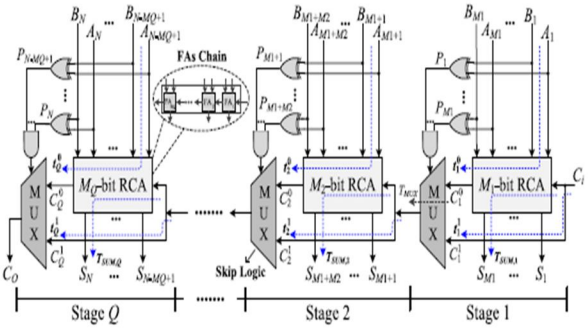

Fig 1: conventional structure of CSKA

IV. PROPOSED CI-CSKA STRUCTURE

The proposed CI-CSKA is the same as conventional one but one major difference of this structure is difference in skip logic; In the conventional one the multiplexer is used as the skip logic but in the proposed CI-CSKA the AOI (And Or Invert), OAI (Or And Invert) can be used as skip logic. AOI & OAI skip logic having some basic gates and it also reduces the area and increase speed compare to conventional one. In this structure incrementation logic block can be used . The incrementation block contains the chain of Halfadders(HAs); the incrementation logic block use the RCAs generated intermediate results; band the carry output of the stage. The internal structure of the incrementation block shown in below figure.

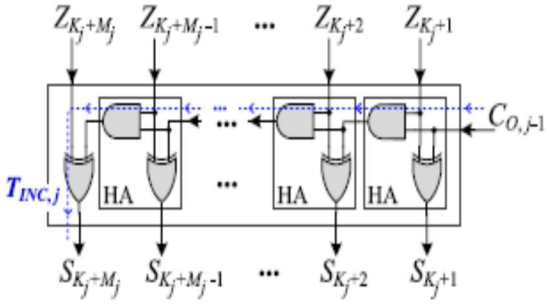

Figure 2: internal structure of the jth incrementation block

The figure contains the jth term it is the intermediate result of jth term. It contains a chain of Halfadders. The proposed CI-CSKA structure is shown in below figure,

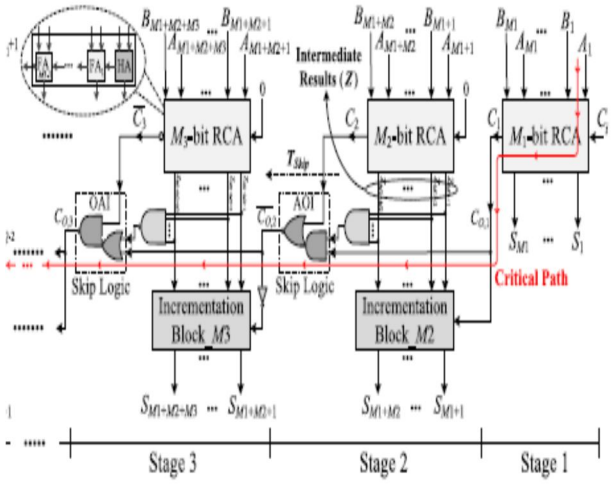

Figure 3: proposed CI-CSKA structure

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V. PROPOSED HYBRID VARIABLE CSKA STRUCTURE

Compare to other adder the proposed hybrid variable CSKA is higher speed. Its having some internal structure. Parallel prefix adder is used as the internal structure of this circuit. The figure of this is shown in below,

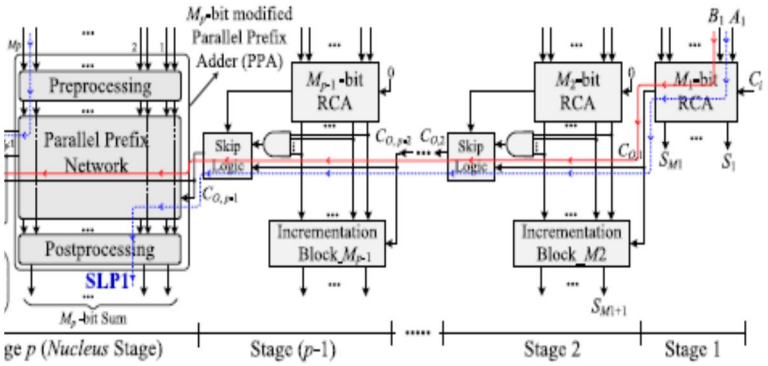

Figure 4: proposed hybrid variable latency CSKA structure

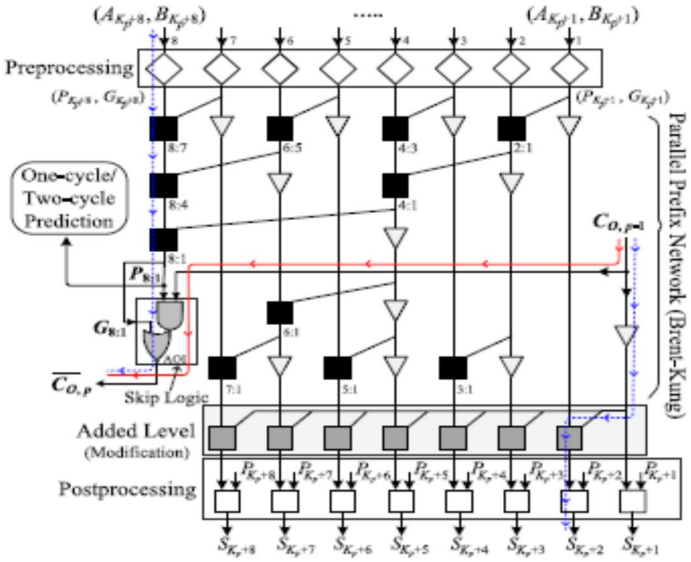

Figure 5: Internal structure of the Pth stage proposed hybrid variable latency CSKA structure

In the above figure every block having some block details, each block details can be explained in 6th diagram. Every block having some mathematical calculation; 1st stage is only buffer ; it stores 1st stage result and gives to p1.

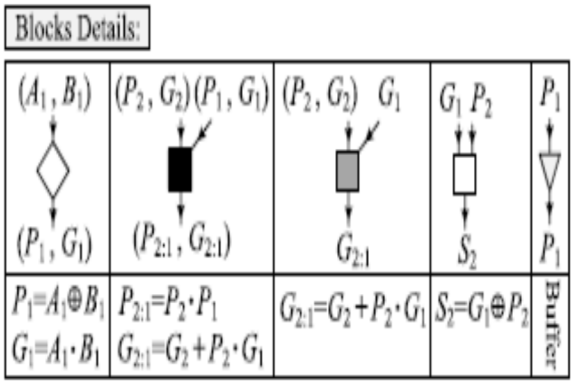

Figure 6: block details of intermediate stage

VI. EXPERIMENTAL RESULTS

It tells about the speed, area occurred and how much delay in the adder; and also tells about the which adder is better and speed wise which adder can be used. Delay also the main thing in the adder circuit; which adder having less delay in this experimental results.

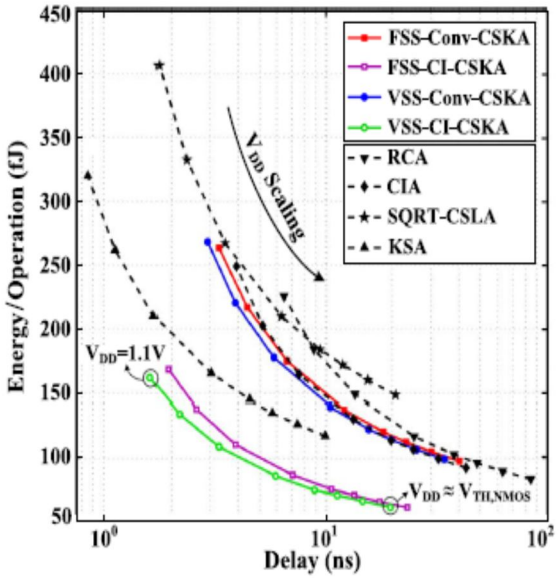

Figure 7: Energy Delay curves for different adders

Table contains the details about how much area occupied and how many gates can be utilized in adders. Table shows the details of this.

Adder Structure	Area (μm^2)	# of Transistors
RCA	151.3	896
CIA	230.0	1402
SQRT-CSLA	357.4	2096
KSA	403.2	2010
FSS-Conv-CSKA	254.2	1456
FSS-CI-CSKA	246.3	1370
VSS-Conv-CSKA	253.1	1464
VSS-CI-CSKA	241.5	1332

Table 1: areas usages and number of the gates in the adder

VII. CONCLUSION

In this paper compare to other adders the proposed hybrid structure exhibits higher speeds and lower energy. AOI and OAI compound gates were exploited for the carry skip logics. the results also suggested that the CSKA structure is a very good adder for the applications where both energy consumption and speed are critical. In addition the modified hybrid variable latency extension of the structure was proposed which reduces the delay and area without affecting the speed of the structures.

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